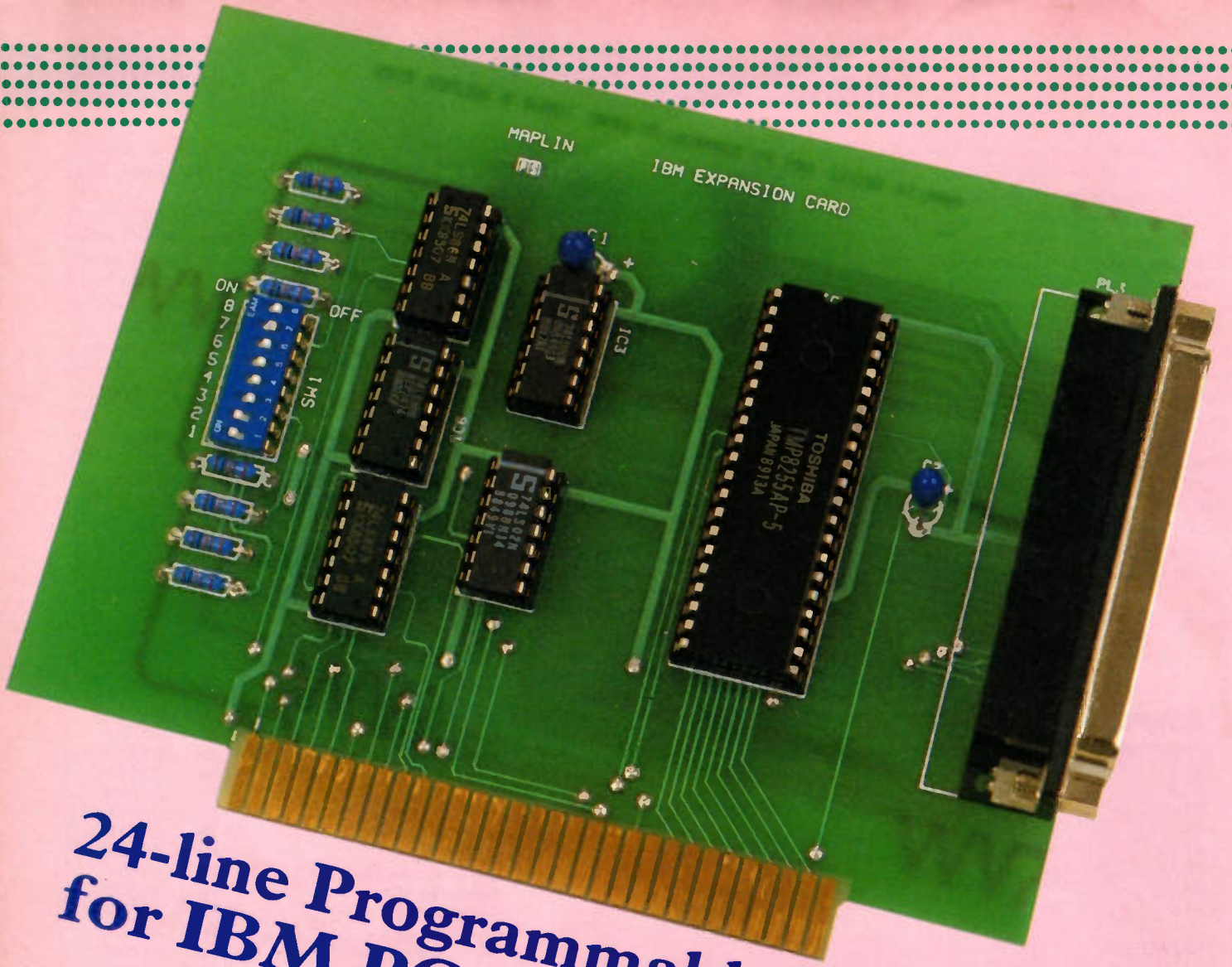


24-line Programmable I/O Card for IBM PC and Compatibles

Design by Peter Long
Text by Robert Ball AMIPRE

Features

- ★ *For use with IBM PC, PC-XT, PC-AT and Compatible Clones*
- ★ *24 Input/Output Lines*
- ★ *Fully Programmable from BASIC using INP and OUT*
- ★ *Base Address Selectable*
- ★ *Uses Industry Standard 8255 PPI IC*

Applications

★ *Data Logging* ★ *Robotics* ★ *Process Control*
★ *Interfacing to External Sensors*
★ *Controlling Lamps, Motors, Relays, Solenoids*
★ *Driving Non-Standard Peripherals*

Introduction

This project is a 24-line digital I/O (Input/Output) card for use with the IBM PC, PC-XT, PC-AT and compatible clones. The card is based around the industry standard 8255 PPI (Programmable Peripheral Interface) IC, which provides 24 I/O lines under user control. The card slots into any one of the vacant expansion slots provided on the host computer. Power, control, address and data signals are obtained from the computer's expansion bus. The 24 I/O lines and +5V and 0V are connected to a 37-way male D-type connector fitted to the rear edge of the board. The D-type connector protrudes through the expansion card slot to facilitate connection with the outside world.

Circuit Description

Figure 1 shows the circuit diagram of the I/O card and the following circuit description should help the constructor understand operation of the unit and assist in fault finding should this become necessary.

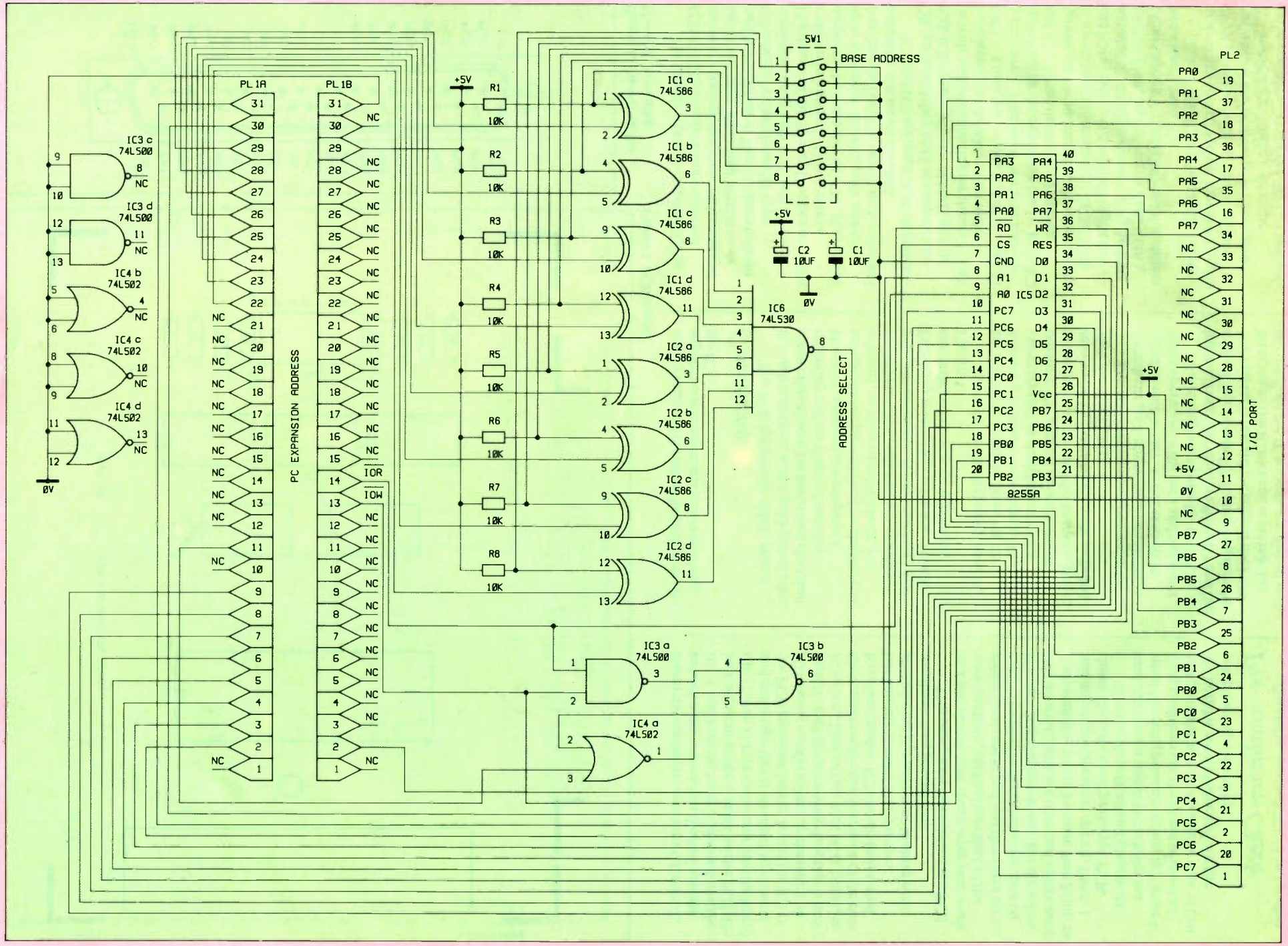


Figure 1. Circuit diagram of the PC I/O Card.

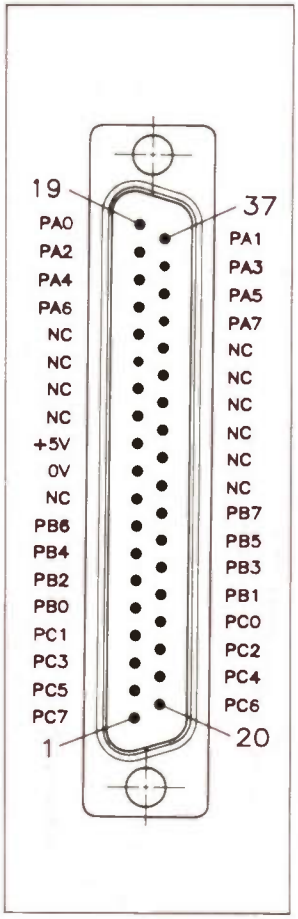


Figure 2. Pin-out of the 37-way D-type plug.

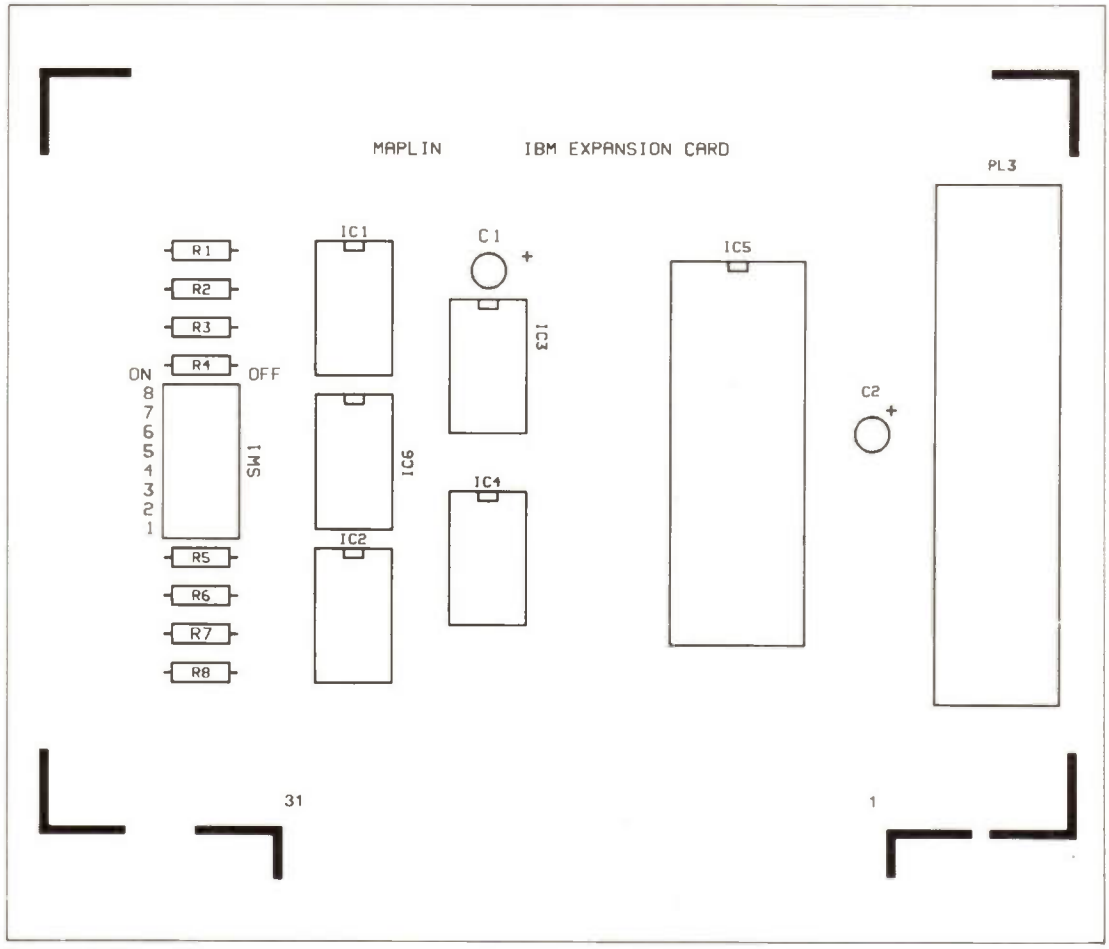


Figure 3. PCB legend.

The circuit is centred around IC5 an 8255 PPI IC, this device provides the necessary control, latching, buffering and handshaking of data being written to, or read from, the card. The I/O lines to/from IC5 connect to the 37-way D-type connector along with +5V and 0V lines. The pinout of the 37-way D-type connector is shown in Figure 2. This device is supported by a number of TTL ICs, which serve to provide the necessary address decoding and enable signals so that the host computer can access the card.

IC1 and IC2 are quad EOR (Exclusive OR) gates and they work in conjunction with IC6, an eight-input NAND gate to provide address decoding for the card. The complement of the address set up by SW1 – 1 to 8 ('on' = logic 0, 'off' = logic 1) is effectively 'compared' with the address appearing on the expansion bus by IC1, IC2 and IC6. When the required address appears on the address bus, the output from IC6 goes low (address select). IC3a, IC3b and IC4a provide IC5 with a Chip Select signal ($\overline{CS}$), which is derived from Address enable (Aen), Input/Output Read ($\overline{IOR}$), Input/Output Write ($\overline{IOW}$) and the address select signal from IC6.

IC3c, IC3d, IC4b, IC4c and IC4d are unused and therefore their inputs are tied to 0V. R1 to R8 are pull-up resistors, they ensure that the 'address select' inputs to IC1 and IC2 are at logic 1 when the corresponding switches of SW1 – 1 to 8 are open (off). C1 and C2 serve to decouple the supply rails and therefore help to prevent supply bourne noise and spikes reaching the ICs.

Construction

The PCB is a double-sided, plated-through hole type, with a gold-plated edge connector, chosen for maximum electrical reliability and mechanical stability. However, removal of a misplaced component is quite difficult with this type of board, so please double-check each component type, value and its polarity where appropriate, *before* soldering! The PCB has a printed legend to assist you in correctly positioning each item, see Figure 3.

The order in which the components are fitted is not critical, however the following instructions will make the assembly task as straightforward as possible. For general information on soldering and assembly techniques, please refer to the Constructors' Guide included with the Maplin kit.

During construction, be careful not to scratch the gold-plated edge connector or splash it with solder, as this is likely to affect operation of the card and computer.

Referring to the parts list and PCB legend, insert the resistors R1 to R8 and the dual-in-line switch SW1, ensuring that the 'on' end faces toward the edge of the PCB. Next insert the IC sockets, ensuring that the notch on the IC sockets are aligned with the corresponding marks on the legend. Insert the tantalum capacitors C1 and C2, in both cases ensure that the lead nearest the + mark on the body is inserted into the hole adjacent to the + mark on the PCB. Fit the 37-way D-type connector into the board and make sure that it is butted-up close to the PCB *before* soldering. Insert the IC1 to IC4, being careful to line up the notch on each IC with the corresponding notch in the IC socket. Ensure that each IC is located in the correct socket and that none of the pins have bent under. IC5 should be inserted last bearing in mind that it is static sensitive; so it is necessary to observe the usual handling precautions.

This completes assembly of the PCB and you should now check-over your work very carefully, making sure that all the solder joints are sound and that there are no solder splashes bridging adjacent pins on ICs, etc. It is also important that the solder side does not have any trimmed component leads standing proud by more than 2mm, as this may result in a short circuit. Photo 1 shows the completed prototype PCB.

If you wish to fit an end plate to the card, the easiest way is to cut holes in a spare blanking plate according to Figure 4. It is possible to use the board without an end plate but you must exercise care so that the board is not dislodged whilst the computer is powered up.

Pre-installation Check

Carefully operate SW1 – 1 to 8 so that they are set to 'on' i.e. the actuators are

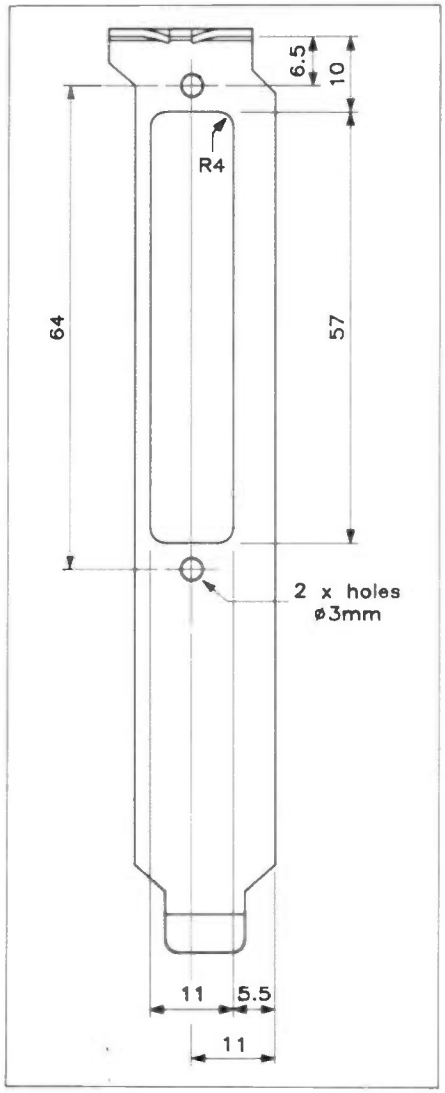


Figure 4. End plate cut-out.

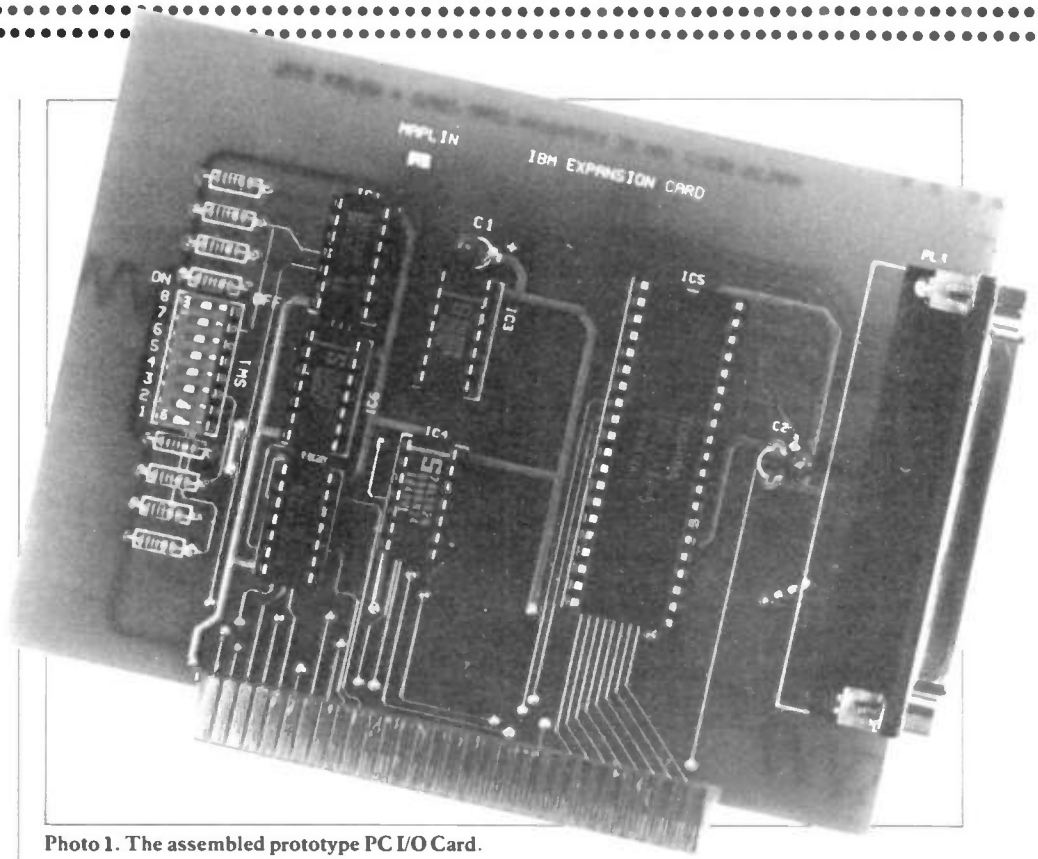


Photo 1. The assembled prototype PC I/O Card.

Description	Hex Address	
	PC PC – XT	PC – AT
DMA controller	000 – 00F	000 – 01F
Interrupt controller	020 – 021	020 – 03F
Timer	040 – 043	040 – 05F
PPI	060 – 063	n/i
Keyboard	n/i	060 – 06F
DMA page register	080 – 083	080 – 09F
NMI mask register	0A	070 – 07F
Interrupt controller	n/i	0A0 – 0BF
Sound generator	n/i	n/i
DMA controller 2	n/i	0C0 – 0DF
Clear/reset math co-processor	n/i	0F0 – 0F1
Math co-processor	n/i	0F8 – 0FF
Joystick	200 – 20F	200 – 207
Expansion unit	210 – 217	n/i
Parallel printer	n/i	278 – 27F
Serial port	3F8 – 3FF	3F8 – 3FF
Serial port	2F8 – 2FF	2F8 – 2FF
Prototype card	300 – 31F	300 – 31F
Fixed disk	320 – 32F	1F0 – 1F8
Parallel printer	378 – 37F	378 – 37F
SDLC	380 – 38F	380 – 38F
Bi-synchronous communications	n/i	3A0 – 3AF
Monochrome adapter/printer	3B0 – 3BF	3B0 – 3BF
Colour/graphics adaptor	3D0 – 3DF	3D0 – 3DF
Diskette controller	3F0 – 3F7	3F0 – 3F7

Note:
n/i = not implemented

Table 1. Designated I/O Addresses.

facing toward the edge of the PCB. Turn the PCB over so that the solder side is uppermost and the gold-plated edge connector is facing towards you, Pin 1 of the edge connector is on the left and Pin 31 is on the right. Using a multimeter, measure the resistance between Pin 29 (+5V) and Pin 31 (0V), be careful not to scratch the contact surface with the test probes, a reading of approximately 1·2kΩ should be obtained. A reading substantially higher than this indicates that SW1 is inserted incorrectly and a reading substantially lower than this indicates a short circuit.

Installation

The installation is broken down into a number of steps. These steps must be followed carefully to avoid problems.

1) Select an appropriate I/O base address, it is important to avoid those already used by existing cards otherwise a bus contention will occur and the computer will crash. Addresses already in use can be determined by consulting the installation instructions for the existing cards, alternatively the Table 1 gives the designated I/O addresses. It is suggested that address 0300 hex is used, unless of course this address is already occupied! This address is designated for prototyping cards.

The address is set up as follows: A9 to A2 select the base address, A1 and A0 select the appropriate register within the 8255 (see later). The settings of SW1 – 1 to 8 can be determined by converting the required address into binary and taking the 8 most significant bits (A9 to A2) as the settings for the switches. SW1 – 1 corresponds to bit A9 and SW1 – 8 corresponds to bit A2, a logic 1 = switch 'on' and a logic 0 = switch 'off'. An example of how to determine the switch settings is shown in Table 2. Photo 2 shows switch settings on the prototype corresponding to an I/O address of 0300 hex.

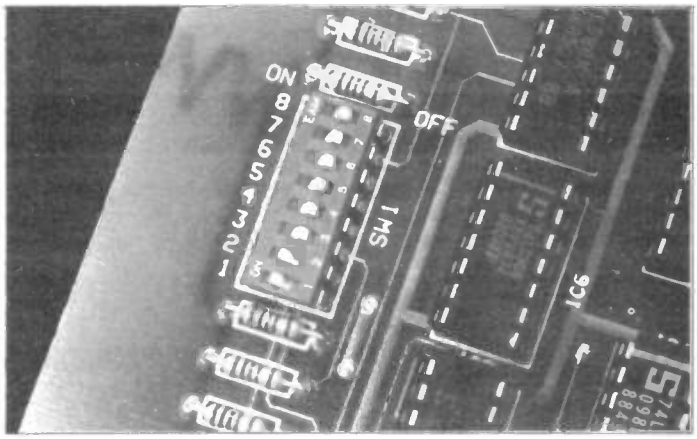


Photo 2. Close-up of the address selection switches (0300 hex).

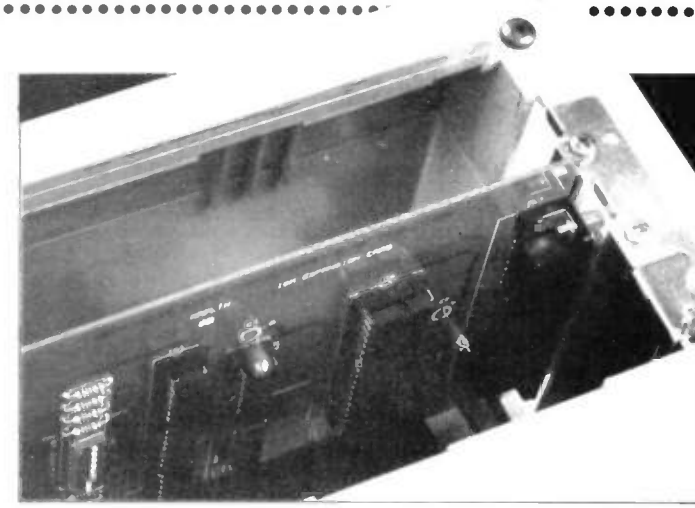


Photo 3. PC I/O Card installed in a computer.

Base address = 0300 hex

0300 hex = 11000000nn
A9 to A2 = 11000000xx
A1 to A0 = xxxxxxxxnn

where:

x = Don't care
n = register selection bit

Switch number:	SW1 – 1	SW1 – 2	SW1 – 3	SW1 – 4	SW1 – 5	SW1 – 6	SW1 – 7	SW1 – 8
Address line:	A9	A8	A7	A6	A5	A4	A3	A2
Binary Value:	1	1	0	0	0	0	0	0
Switch setting:	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF

Table 2. An example of how to determine switch settings.

```
10 BASEADD% = &H300          ' Set up base address for I/O card
20 OUT BASEADD% + 3,128      ' Set 8255 to Mode 0 control word 0
30 OUT BASEADD%,&HFF         ' Set all pins to logic 1
40 OUT BASEADD% + 1,&HFF
50 OUT BASEADD% + 2,&HFF
60 PRINT "LOGIC 1"
70 GOSUB 140                 ' Call delay subroutine
80 OUT BASEADD%,0            ' Set all pins to logic 0
90 OUT BASEADD% + 1,0
100 OUT BASEADD% + 2,0
110 PRINT "LOGIC 0"
120 GOSUB 140                ' Call delay subroutine
130 GOTO 30                  ' Repeat
140 FOR I = 1 TO 2000        ' Delay Subroutine
150 NEXT I
160 RETURN
```

Listing 1. A simple program to test the I/O card.

2) Turn off power and disconnect the computer from the mains supply. Failure to take these steps may expose potentially lethal mains voltage and installation of the card with the computer switched on may result in permanent damage to your computer and/or the card.

3) Remove the cover on the expansion card area of the computer or remove the computer case (dependent on model).

4) Locate an empty expansion slot and remove the metal cover plate fixing screw and cover.

5) Insert the card into the empty slot pushing it firmly home without forcing it. Photo 3 shows the prototype card installed in the authors' computer.

6) Replace the cover/case.

Testing

Switch on the computer, it should boot up in the normal way. If you have a system without a hard disk drive, you will need to insert a 'System Disk'. If the computer behaves in an abnormal way, turn off the computer immediately and remove the expansion card.

A simple program written in GWBASIC can be used to test the board, see Listing 1. The program sets all three ports to outputs and toggles them between logic 1 and logic 0 at short intervals, thus producing a square wave at each output pin. Each of the 24 output lines can be checked with a logic probe, oscilloscope, multimeter or the test circuit shown in Figure 5. Figure 6 shows a suggested strip board layout for the the test circuit. Photo 4 shows the test circuit assembled on a piece of strip board.

The delay may be adjusted to alter the period of the square wave output; this is achieved by altering the number in line 140, presently set at 2000. A lower number will decrease the periodic time and hence increase the frequency of the square wave. A higher number will have the opposite effect. A logic probe will show alternately logic 1 and logic 0. Whilst a scope will show a square wave (suggest delay in line 140 of 5, sweep speed of 20ms, attenuator set to 0·2V/cm, input DC coupled and the probe set to 'x 10'). With an analogue multimeter (set to 10V DC range) the needle will read alternately ≥2·4V and 0V. With a digital multimeter (set to 10V DC range) the display will read alternately ≥2·4V and 0V. With the test circuit shown in Figure 5 connected to each port in turn (A, B and C) the LEDs will flash on and off together.

8255 Operating Modes

As previously stated, the card utilises an 8255 PPI IC, which is a general purpose I/O device. The 8255 has 24 I/O lines

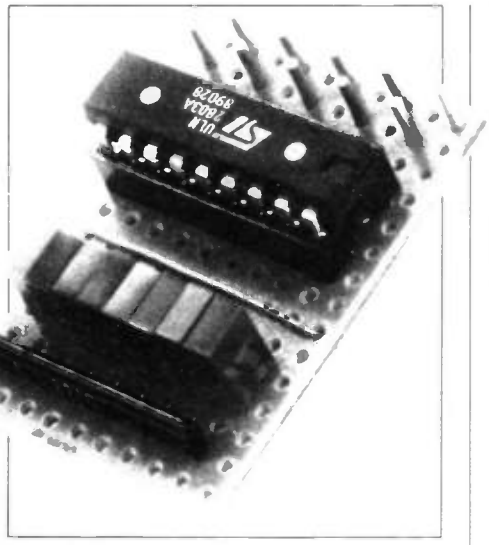


Photo 4. The suggested test circuit.

divided into three ports of 8-lines each; Port A, Port B and Port C. The three ports are configured in two groups of 12-lines, these are referred to as Group A and Group B. Group A comprises of all 8-lines of Port A (PA7 – 0) and the upper 4-lines of Port C (PA7 – 4). Group B comprises of all 8-lines of Port B (PB7 – 0) and the lower 4-lines of Port C (PC3 – 0). This is summarised in Table 3.

The way in which the function of each of the 24-lines is defined is determined by

Group A – Port A (PA7 – 0) and Port C (PC7 – 4)
Group B – Port B (PB7 – 0) and Port C (PC3 – 0)

Table 3. 8255 Grouping of Ports.

the Mode. There are three possible operating modes and these can be summarised as follows:

Mode 0; Each group of 12-lines can be configured, in a set of 8-lines and a set of 4-lines, to be either inputs or outputs.

Mode 1; Each group of 12-lines can be configured to have 8-lines of I/O. Three of the remaining lines in each group are used for handshaking and a further two lines are available for I/O.

Mode 2; Group A is configured to operate in a bi-directional bus mode using 8-lines from Group A for the bi-directional bus, and 4-lines from Group A and 1-line from Group B for handshaking. The remaining lines from Group B can be configured to operate in either Mode 0 or Mode 1.

The operating mode and definition of each port is defined by writing information to the Control Register located at three bytes above the (previously determined) base address in the I/O map. The control register can only be written to and not read from. Data may be written to and read from each of the three ports at the first three consecutive addresses starting from the base address. The arrangement of the 8255

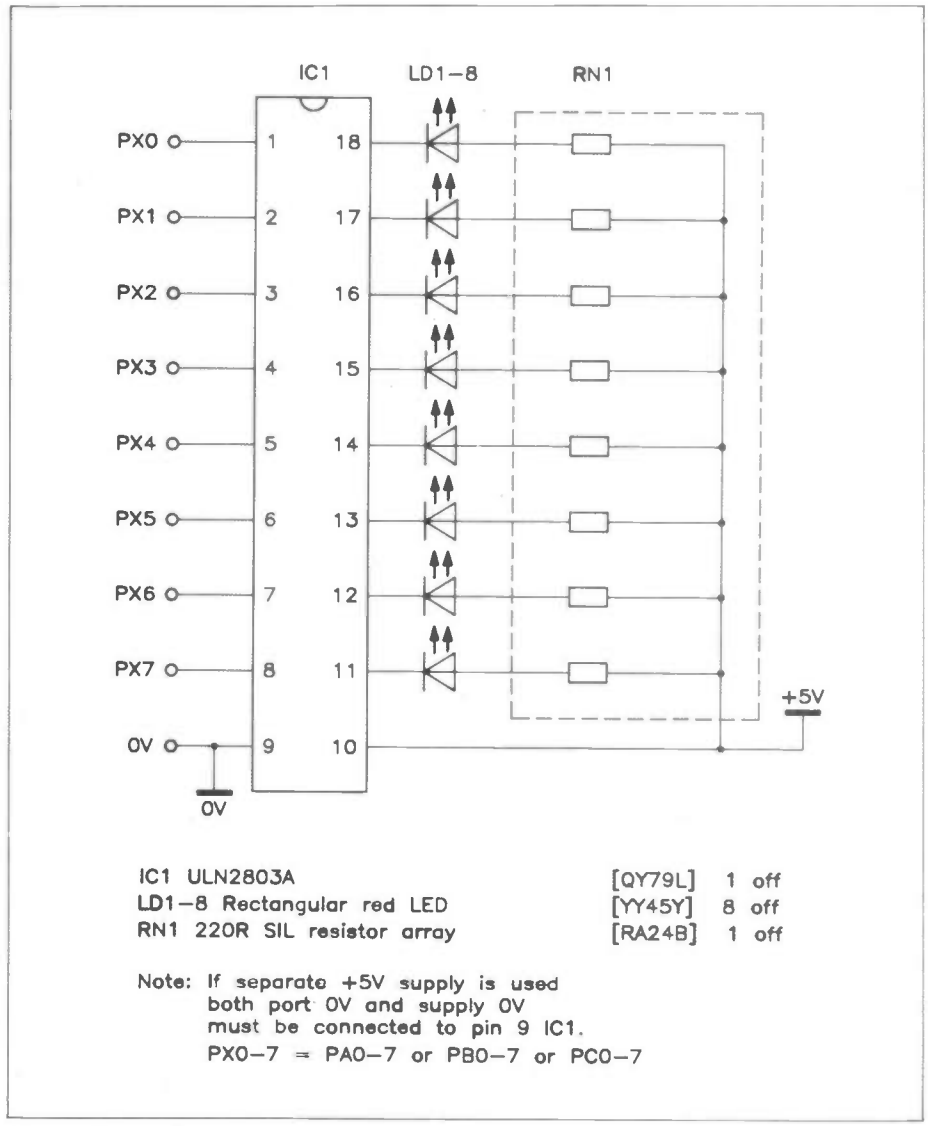


Figure 5. Circuit diagram of a suitable test circuit.

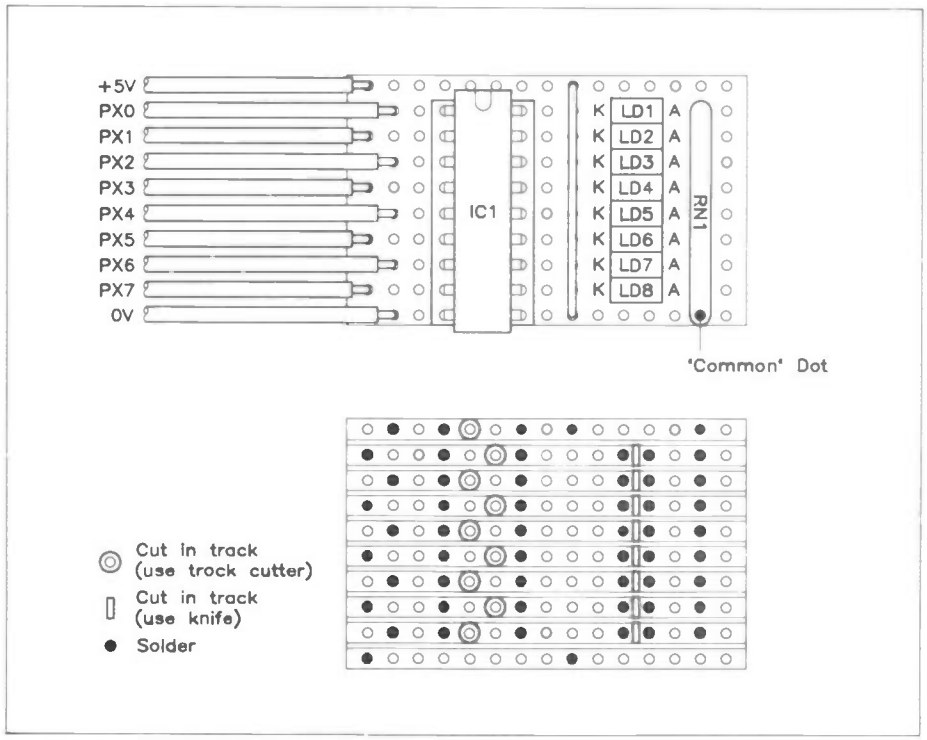


Figure 6. Suggested strip board layout for the test circuit.

Read Mode	
Offset from base address	Input operation
0	Port A → Data bus
1	Port B → Data bus
2	Port C → Data bus

Write Mode	
Offset from base address	Output Operation
0	Data Bus → Port A
1	Data Bus → Port B
2	Data Bus → Port C
3	Data Bus → Control Register

Table 4. Writing to and reading from the 8255 Registers.

D7			Mode/Bit Set/Reset Flag
1		=	Mode Set
0		=	Bit Set/Reset (see text)
Group A			
D6	D5		Mode selection
0	0	=	Mode 0
0	1	=	Mode 1
1	x	=	Mode 2
D4			Port A
1		=	Input
0		=	Output
D3			Port C (upper)
1		=	Input
0		=	Output
Group B			
D2			Mode selection
0		=	Mode 0
1		=	Mode 1
D1			Port B
1		=	Input
0		=	Output
D0			Port C (lower)
1		=	Input
0		=	Output

Table 5. The 8255 Control Register (Mode Selection).

Output line	=	Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
Decimal value	=	128	64	32	16	8	4	2	1

Where: x = port A, B or C

Example:

Output line	=	PB7	PB6	PB6	PB6	PB6	PB2	PB1	PB0
Decimal value	=	128	64	32	16	8	4	2	1
Binary value	=	1	0	0	0	0	1	0	0

= 128 + 4
= 84 hex
= 132 decimal

Table 7. Setting and resetting output lines.

registers is shown in Table 4. Table 5 shows the function of the 8 data bits within the control register, D7 is used to select the Mode/Bit Set/Reset, in most cases D7 will be set to logic 1. An example of how the 8255 can be set up by writing to the control register is shown in Table 6.

Accessing the I/O Card from GWBASIC

Defining the Base Address

The easiest way to define the base address for use in a BASIC program is to set an integer variable (% suffix) to the base address value. Then whenever the card needs to be accessed using the OUT or INP instructions the variable (plus offset where necessary) can be used instead of the actual address. This technique is good programming practice as the base address can be changed by modifying just one line of the program instead of tediously having to change every usage of the address. An example of this is shown in Listing 2.

Mode 0	
PA7 – PA0	IN
PC7 – PC4	OUT
PB7 – PB0	OUT
PC3 – PC0	IN
D7 = 1	Mode Set
D6 = 0 D5 = 0	Mode 0
D4 = 1	Input
D3 = 0	Output
D2 = 0	Mode 0
D1 = 0	Output
D0 = 1	Input

Control Byte = 10010001 binary
= 91 hex
= 145 decimal

Table 6. An example of setting 8255 Ports in Mode 0.

Setting the 8255 Operating Mode

The operating mode of the 8255 can be set by first determining the correct value of data that needs to be written to the 8255 control register (which was dealt with earlier), then writing the data using the OUT instruction. An example of this is shown in Listing 3.

Setting and Resetting Output Lines

To set and reset output lines, the appropriate port must be written to, using the OUT instruction, with data corresponding to the binary weighting of the output lines. Calculation of the data value can easily be achieved by using a number line and adding the values where a Logic 1 is required. Table 7 shows a binary weighted number line together with an example of how to calculate the data for setting Port B line PB7 and PB2 to logic 1 (the remaining lines will be set to logic 0).

Listing 4 shows an example of how to output the data to the Port B register.

Reading Data from Input Lines

Using the INP instruction, data from an input port can be read. The value of the data will be determined by the binary weighting of the logic levels on the input lines – the opposite process to calculating data to set and reset output lines. An example of how data can read from Port A is shown in Listing 5.

```
10 BASEADD% = &H0300
```

Listing 2. Example line of BASIC to set base address variable to 0300 hex.

```
In hex:
20 OUT BASEADD% + 3, &H91

In decimal:
20 OUT BASEADD% + 3, 145
```

Listing 3. Example line of BASIC to set 8255 to MODE 0 with Port A & Port C (lower) to input and Port B & Port C (upper) to output.

```
In hex:
30 OUT BASEADD% + 2, &H84

In decimal:
30 OUT BASEADD% + 2, 132
```

Listing 4. Example line of BASIC to set Port B lines PB7 and PB2 to Logic 1 and reset the other lines to Logic 0.

```
40 DAT% = INP (BASEADD%)
```

Listing 5. Example line of BASIC to read data from Port A.

Interfacing with the Outside World

The I/O lines on the 8255, when configured as outputs, are not capable of sourcing or sinking large amounts of current. Similarly the I/O lines, when configured as inputs, are not designed to accept voltages outside the range of the normal logic levels associated with 5V TTL and CMOS logic. It is necessary for outputs to be buffered according to the load that is to be driven and inputs be conditioned to conform to the correct logic levels. Flaunt these requirements at your (or rather the computer's and I/O card's) peril, you have been warned!

Figure 7 shows a number of output buffering circuits and Figure 8 shows a number of input conditioning circuits. These circuits must be considered as a basis for your own experimentation, no warranty is given for suitability in particular applications.

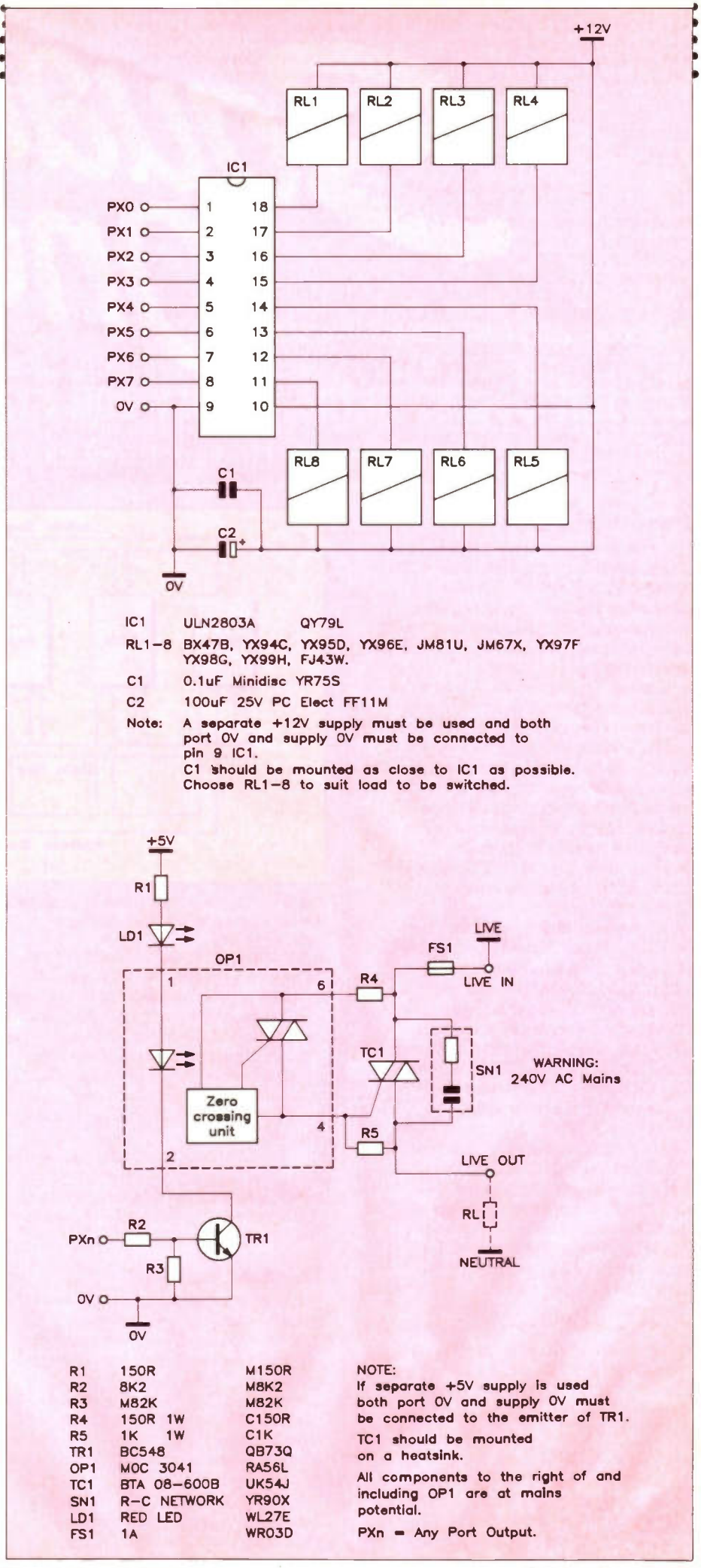
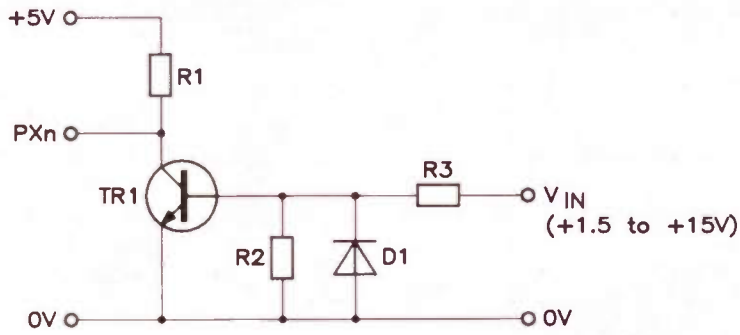


Figure 7. Output buffer circuits.

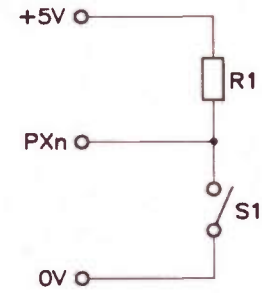
Continued on page 39.

PROGRAMMABLE I/O CARD Continued from page 31.

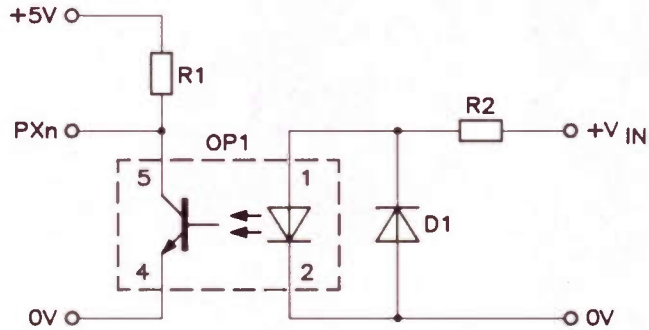


R1	= 2K7	M2K7
R2	= 220K	M220K
R3	= 22K	M22K
TR1	= BC548	QB73Q
D1	= 1N4148	QL80B

Note:
Input Voltage 0V must be connected to Port 0V.
Input is protected against negative voltage.



R1 = 2K7 M2K7
S1 = Switch



R1	= 2K7			M2K7
OP1	= Hi Sensitivity OPTO			RA57M
D1	= 1N4148			QL80B
V_{IN}	= +1.5V	R2	= 18R	M18R
V_{IN}	= +5V	R2	= 360R	M360R
V_{IN}	= +9V	R2	= 750R	M750R
V_{IN}	= +12V	R2	= 1K	M1K

Note:
Input is isolated from output.
Input is protected against negative voltage.

Further Information

As can be seen, the 8255 is an extremely flexible device, offering a wide range of operating configurations. For simplicity, only Mode 0 has been dealt with here, for readers wishing to utilise the other operating modes, a 24 page data book is available separately, order As (8255 Data Book) XK97F Price 75p. Numerous buffer ICs may be found in the semiconductor section of the current Maplin Buyers' Guide, data sheets for which may be obtained through the Maplin Mail Order Service, currently the price of data sheets is 40p (correct at time of going to press).

Figure 8. Input conditioning circuits.

IBM PC EXPANSION KIT PARTS LIST

RESISTORS: All 0·6W 1% Metal Film			
R1-8	10k	8	(M10K)
CAPACITORS			
C1,2	10μF 16V Tantalum	2	(WW68Y)
SEMICONDUCTORS			
IC1,2	74LS86	2	(YF36P)
IC3	74LS00	1	(YF00A)
IC4	74LS02	1	(YF02C)
IC5	8255A	1	(YH50E)
IC6	74LS30	1	(YF20W)
MISCELLANEOUS			
S1	Slimline 8W DIL Switch	1 Pkt	(QY70M)
PL2	RA D-Range 37-Way Plug	1	(JB37S)
	DIL Socket 14-pin	5	(BL18U)
	DIL Socket 40-pin	1	(HQ38R)
	PC Board	1	(GE31J)
	Constructors' Guide	1	(XH79L)
	IBM Exp. Leaflet	1	(XK29G)
OPTIONAL (Not in Kit)			
	D-Connector Jack Post	1 Pr	(FP31J)
	8255 Data Book	1	(XK97F)

The above items, except Optional are available as a kit:
Order As LP12N (IBM PC Expansion Kit) Price £17.95
The following items are also available separately:
IBM PC Expansion PCB Order As GE31J Price £11.95
8255 Data Book **Order As XK97F Price 75p** *NV*