

CHIP SIZE SELECT HEADERS.
SEE PAGE 2 FOR DETAILS.
J20 IS FOR BANK 1, J22 IS
FOR BANK 2.

STANDBY POWER
BATTERY BACKUP
SELECT HEADER.
SEE DIAGRAM.

BASE ADDRESS SELECT
SEE PAGE 3 FOR DETAILS.

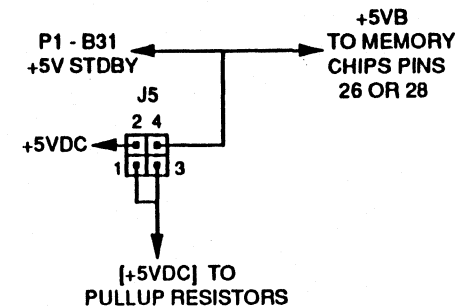
J21 AND J23 ARE ACCESS TIME
JUMPERS. SEE PAGE 3 FOR DETAILS.

PART NUMBERS:

MVME211 01-W3295B01 76432569

SEE CURRENT REVISION LEVEL (CRL)
FOR CURRENT REVISION INFORMATION.

STANDBY POWER BATTERY BACKUP SELECT

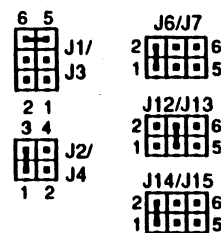


NOTE 1: THE BASE ADDRESS IS DEPENDANT ON THE SIZE OF MEMORY
DEVICES BEING INSTALLED IN EACH BLOCK.

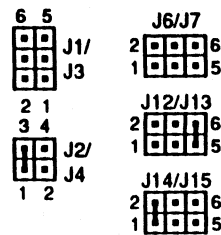
NOTE 2: MEMORY ARRAY IS SEPARATED INTO 2 BANKS. BANK 1
CONSISTS OF JUMPERS J1, J2, J6, J12 AND J14. BANK 2
CONSISTS OF JUMPERS J3, J4, J7, J13 AND J15. SEE PAGE 2
FOR CONFIGURATIONS AND SIGNAL NOMENCLATURE.

09/12/89

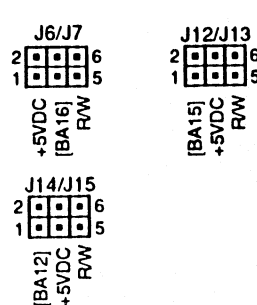
09/12/89



**16K X 8 EPROM
INTEL 27128**



**4K X 8 RAM
INDUSTRY STANDARD**



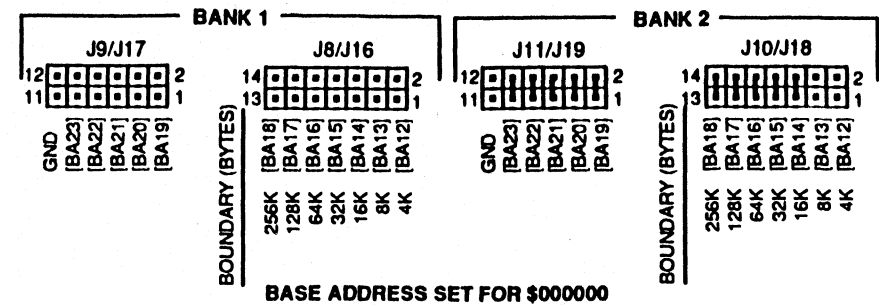
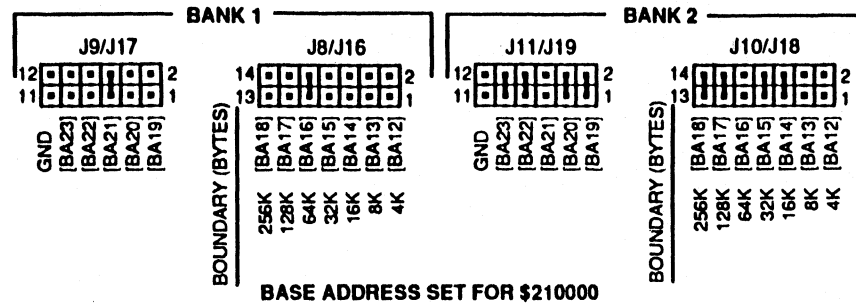
8K X 8 NMOS RAM
INTEL 2186-25

J20/J22

6	5
■	■
■	■
■	■
2	1

LOGICAL
EQUIVALENT
NUMBER 7
DO NOT USE
THIS OPTION

BASE ADDRESS SELECT HEADERS



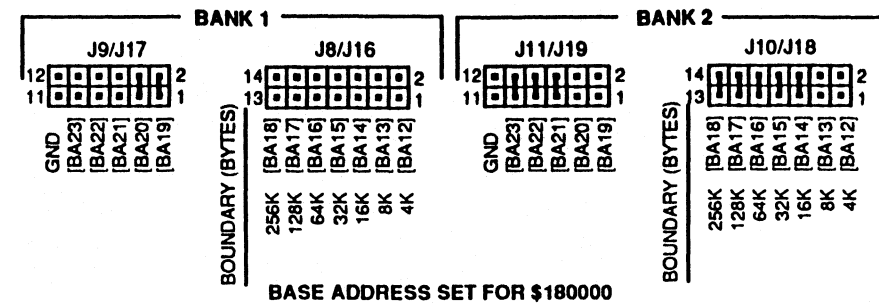
MEMORY DEVICE CAPACITY	ADDRESS LINE FUNCTION						
	A12	A13	A14	A15	A16	A17	A18
2K X 8	S	S	X	X	X	X	X
4K X 8	A	S	S	X	X	X	X
8K X 8	A	A	S	X	X	X	X
16K X 8	A	A	A	S	S	X	X
32K X 8	A	A	A	A	S	S	X
64K X 8	A	A	A	A	A	S	S

WHERE: A = USED FOR INTERNAL ADDRESSING
 S = USED FOR SOCKET PAIR SELECTION
 X = AVAILABLE FOR BLOCK ADDRESS DECODING

NOTES: ADDRESS LINE A01 - A11 ARE ALWAYS USED FOR INTERNAL ADDRESSING.

ADDRESS LINES A19 - A23 ARE ALWAYS USED FOR BLOCK ADDRESS DECODING, AND ARE ALWAYS JUMPED EXCEPT WHEN THE BLOCK IS DISABLED.

THE "SOCKET PAIR SELECTION" (S) ADDRESS(ES) MAY BE JUMPED, BUT THIS WILL DISABLE PART OF THE MEMORY BLOCK SELECTED. SUCH DISABLING IS NOT RECOMMENDED BY MOTOROLA.



ACCESS TIME SELECT (NOMINAL ACCESS TIME IN NANoseconds)

