

Overview

The Digital Video Board is a single-slot PCI Bus or SBus board that implements a high-speed DMA channel between an external digital video camera and the host computer. The device interface side of the board consists of thirty-five RS-422-compatible driver/receivers connected to a Xilinx RAM-based programmable gate array. These driver/receivers can be assigned as inputs or outputs in groups of four. The Xilinx device can be programmed to implement arbitrary interface protocols by executing a program that downloads a bit pattern from a file to the PCI DV or SDV board.

This document describes the PCI DV or SDV hardware and software specific to the Amber Radiance Camera. The Amber Radiance 1 is an infrared camera with several different data interfaces. The PCI DV or SDV is connected to the HSVB Interface. This manual lists the camera-specific files included with the software, provides a connector pinout for the camera end of the cable, and includes information on the registers implemented in the Xilinx gate array.

For complete information on using the Digital Video board, see the *PCI DV User's Guide for Solaris* (part number 008-00966), *PCI DV User's Guide for Windows NT* (part number 008-01075), or the *SDV User's Guide* (part number 008-00411), for which you can contact Engineering Design Team, Inc.

Included Files

In addition to the files shipped with the PCI DV or SDV, the following files are shipped with the SDV for the Amber Radiance 1 camera:

camera_config/rad1.bit

Firmware for Amber Radiance 1 camera.

NOTE: For SBus hosts, this file is named rad1.rbt.

camera_config/ar*.cfg

Configuration file chosen when you select the camera model in the setup dialog.

Connector Pinout

The Digital Video Board uses a high-density 80-pin I/O connector. The Amber Radiance 1 camera HSVB interface uses a high-density 50-pin connector. The cable provided by EDT adapts the PCI DV or SDV board to the camera.

The 50-pin male cable connector is AMP part number 749621-5, with a shielded backshell (AMP part number 749193-2).

The following pinout diagram describes the connection from the cable to the camera. The connection from the SDV board to the cable is described in the user's guides listed above.

Pin	Radiance Signal	PCI DV or SDV Signal	Pin	Radiance Signal	PCI DV or SDV Signal
1	Ground	Ground	26	Ground	Ground
2	DATA0 +	MSB0 +	27	DATA0 –	MSB0 –
3	DATA1 +	MSB1 +	28	DATA1 –	MSB1 –
4	DATA2 +	MSB2 +	29	DATA2 –	MSB2 –
5	DATA3 +	MSB3 +	30	DATA3 –	MSB3 –
6	DATA4 +	MSB4 +	31	DATA4 –	MSB4 –
7	DATA5 +	MSB5 +	32	DATA5 –	MSB5 –
8	DATA6 +	MSB6 +	33	DATA6 –	MSB6 –
9	DATA7 +	MSB7 +	34	DATA7 –	MSB7 –
10	DATA8 +	MSB8 +	35	DATA8 –	MSB8 –
11	DATA9 +	MSB9 +	36	DATA9 –	MSB9 –
12	DATA10 +	MSB10 +	37	DATA10 –	MSB10 –
13	DATA11 +	MSB11 +	38	DATA11 –	MSB11 –
14	DATA12 +	MSB12 +	39	DATA12 –	MSB12 –
15	DATA13 +	MSB13 +	40	DATA13 –	MSB13 –
16	DATA14 +	MSB14 +	41	DATA14 –	MSB14 –
17	DATA15 +	MSB15 +	42	DATA15 –	MSB15 –
18	PIXELCLK +	PSTRB +	43	PIXELCLK –	PSTRB –
19	HS_LS +	LINE+	44	HS_LS –	LINE –
20	HS_FS +	FRAME +	45	HS_FS –	FRAME –
21	GATE	FRMRST / EXP +	46	GATE	FRMRST / EXP –
22	unused		47	unused	
23	unused		48	unused	
24	unused		49	unused	
25	unused		50	unused	

Table 1. Connector Pinout

Xilinx Programmable Gate Array Registers

The Xilinx programmable gate array contains four registers: command, status, configuration and data path. Each is described below.

Command Register

The command register is an 8-bit write-only register at address 0x00 (0x0000.8080 for SBus hosts).

Bit	Name	Description
7-3		not used
2	AQ_CLR	Setting this bit resets the acquisition done interrupt.
1	ENABLE_GRAB	Enable acquisition of the next complete frame. If enabled in the configuration register, the shutter timer is started. If the continuous acquisition bit is set in the data path register, then ENABLE_GRAB starts acquisition. Acquisition continues until the continuous bit is reset.
0	RESET_INTFC	Setting this bit resets the PCI DV or SDV interface board.

Table 2. Xilinx Programmable Gate Array Command Register

Status Register

The status register is an 8-bit read-only register at address 0x01 (0x0000.8081 for SBus hosts). The executable `watchstat` (included with the PCI DV or SDV software) reads and displays this register symbolically.

Bit	Name	Description
7	AQUIRE_IP	When set, the camera is presently acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued and the camera is waiting for a valid beginning of a frame.
5-2	not used	
1	FRAME_VALID	When set, the camera shutter has closed and valid data is being transmitted.
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting. Therefore the data has been corrupted.

Table 3. Xilinx Programmable Gate Array Status Register

Configuration Register

The configuration register is an 8-bit read-write register at address 0x02 (0x0000.8082 for SBus hosts).

Bit	Name	Description
7	INT_ENAQ	Setting this bit enables acquisition interrupt. This interrupt is asserted when the next acquisition is complete. Reset the interrupt with the AQ_CLR bit in the command register.
6	SHFT2	Setting this bit shifts the HSVB data bits down by two, ignoring the DATA0 and DATA1 bits. The Amber Radiance 1 sends gain and offset information on these bits and pixel data on DATA[2-13]. If pixel information only is required, set this bit and acquire data as a 12-bit camera. If gain and offset is required, clear this bit and acquire data as a 14-bit camera. See Data Path register to set bit depth of pixels.
5	FILTER_00_ON	Setting this bit turns on a filter that maps all bits from 00–10 such that 00–07 are not used. This saves the lowest eight color palette indexes for use by the window manager. This bit is ignored unless the data path is set to clip the camera resolution to 8 bits.
4	FILTER_F0_ON	Setting this bit turns on a filter that maps all bits from F0–FF such that F8–FF are not used. This saves the highest eight color palette indexes for use by the window manager. This bit is ignored unless the data path is set to clip the camera resolution to 8 bits.
3	FIFO_RESET	Set and clear this bit to reset the PCI DV or SDV input FIFOs.
2-0	not used	

Table 4. Xilinx Programmable Gate Array Configuration Register

Data Path Register

The data path register is an 8-bit read-write register at address 0x06 (0x0000.8086 for SBus hosts).

Bit	Name	Description																				
7-5	not used																					
4	CONTINUOUS	Set if PCI DV or SDV is to acquire successive frames of data. ENABLE_GRAB in the command register must be set to start acquisition. After CONTINUOUS has been cleared, acquisition continues until the end of a complete frame.																				
3	not used	Reserved																				
2-1	RES[1-0]	Set for maximum depth resolution of the camera—the number of shades of gray it can display. <table><tr><td>RES1</td><td>RES0</td><td>Resolution</td><td>Shades of Gray</td></tr><tr><td>0</td><td>0</td><td>12-bit</td><td>4096</td></tr><tr><td>0</td><td>1</td><td>10-bit</td><td>1024</td></tr><tr><td>1</td><td>0</td><td>16-bit</td><td>65,536</td></tr><tr><td>1</td><td>1</td><td>14-bit</td><td>13,384</td></tr></table>	RES1	RES0	Resolution	Shades of Gray	0	0	12-bit	4096	0	1	10-bit	1024	1	0	16-bit	65,536	1	1	14-bit	13,384
RES1	RES0	Resolution	Shades of Gray																			
0	0	12-bit	4096																			
0	1	10-bit	1024																			
1	0	16-bit	65,536																			
1	1	14-bit	13,384																			
0	EXT_DEPTH	Set when operating the camera in the maximum depth resolution. Cleared when operating in 8-bit mode. In 8-bit mode, the most significant 8 bits of data are extracted from each pixel and packed in bytes. Always clear for 8-bit cameras.																				

Table 5. Xilinx Programmable Gate Array Data Path Register

Utility Register (PCI Bus only)

The utility register is an 8-bit read-write register at address 0x0F.

Bit	Name	Description															
7		not used															
6		reserved															
5-3		not used															
2-1	HWPAD	Add pixels to each row for use with Windows NT library functions that require word-aligned data, as follows:															
		<table> <tr> <th>Bit 2</th><th>Bit 1</th><th>Pixels Added</th></tr> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>2</td></tr> <tr> <td>1</td><td>1</td><td>3</td></tr> </table>	Bit 2	Bit 1	Pixels Added	0	0	0	0	1	1	1	0	2	1	1	3
Bit 2	Bit 1	Pixels Added															
0	0	0															
0	1	1															
1	0	2															
1	1	3															
0	BSWAP	A value of 1 swaps the order of bytes in a 16-bit word of data coming in from the camera, to accommodate Intel byte order.															

Table 6. Xilinx Programmable Gate Array Utility Register

Use bits 1 and 2 of the Utility register to pad each line in an image with additional pixels, extending the native camera line length. This may be desirable for use with certain Windows NT library functions used to draw to the display, because certain of these functions require word-aligned data.

If you set either of these bits, the hardware will pad the image rows, but the software will be unaware of the change. To ensure that the software remains compatible with the hardware, edit the camera configuration file:

- Set the `width` parameter to the new number—the native line length, in pixels, plus the pad.
- Set the `hwpad` parameter to the number of pixels you're adding.

For example, the Kodak MegaPLUS 1.6 10-bit camera has a native width of 1534 pixels. To use images from this camera with library functions requiring word-aligned data:

1. Set bit 2 of the Utility register.
2. Edit the configuration file so that the corresponding lines read:

```
width: 1536  
hwpad: 2
```