PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/12/7341
Dated 20 Aug 2012

M24128, 128 Kbit Serial I2C Bus EEPROM / Industrial range Redesign and upgrade to the CMOSF8H process technology

Table 1. Change Implementation Schedule

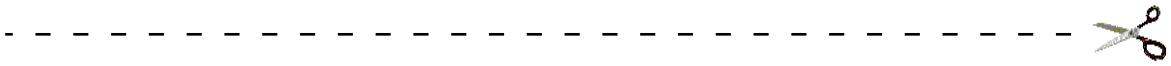
Forecasted implementation date for change	13-Aug-2012
Forecasted availability date of samples for customer	13-Aug-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	13-Aug-2012
Estimated date of changed product first shipment	09-Nov-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24128 products family
Type of change	Waferfab technology change
Reason for change	Line up to state-of-the-art of design
Description of the change	Redesign and upgrade to the new CMOSF8H Process technology.
Change Product Identification	Process Technology identifier "K" for F8H
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/12/7341**
Please sign and return to STMicroelectronics Sales Office	**Dated 20 Aug 2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
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Candela, Jean-Philippe	Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M24128, 128 Kbit Serial I2C Bus EEPROM / Industrial range
Redesign and upgrade to the CMOSF8H process technology

What is the change?
The **M24128**, 128 Kbit serial I²C bus EEPROM product's family, currently produced using the CMOSF8L process technology at ST Rousset (France) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at the same wafer diffusion plant.

This upgraded version in CMOSF8H allows us to offer:
- **1.7 V** / 5.5 V ("-D**F**") Vcc range
- Lockable Identification Page ("-**D**")
- Frequency up to 1 MHz
- Write cycles up to 4 millions
- Data retention up to 200 years

The new M24128 in CMOSF8H version is functionally compatible with the current CMOSF8L version (as detailed in datasheet rev. 20 - November 2011, attached).

Following parameters are updated in the revised datasheet (rev. 21):

- tCLQX(min) = 100 ns at 400 kHz (200 ns for F8L version)
- tNS = 80 ns at 400 kHz (100 ns for F8L version)

AC timings concerning the signal applied on /WC input are now specified:
- tWLDL (/WC set up time before a START condition) : 0 µs (min)
- tDHWH (/WC hold time after a STOP condition) : 1 µs (min)

Concurrent to this change, the following production rationalization will follow:

- SO8N (Narrow, 150 mils) assembled on SHD line at ST Shenzhen will use 0.8 mil Copper wire (as introduced in PCN MMS-MMY/11/6929).
- MLP 2x3 (UFDFPN) will change from small exposed pad (package code "MB") to large exposed pad (package code "MC"), PTN will be released in 2h/2012.
- WLCSP (Wafer Level Chip scale Package): Commercial Part Number will change from M24128-BFCS6TP/A to M24128-DFCS6TP/K (with smaller dimensions), PTN will be released in 2h/2012.

Why?
The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24128 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?
The production of the upgraded M24128 with the new CMOSF8H will ramp up from end of August 2012 and shipments can start from Week 45 / 2012 onward (or earlier upon customer approval).

How will the change be qualified?
The new version of the M24128 was qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.
The CMOSF8H process technology is already qualified for this product family.
The intermediate **Qualification Report QRMMY1202** is available and included inside this document.

What is the impact of the change?

- Form: marking change (see **Device marking** paragraph)

- Fit: product dimension change for WLCSP

- Function:
- change on **DC characteristics** (updated in datasheet rev. 21)
- change on **AC performances** (updated in datasheet rev. 21)

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "**K**" for the **upgraded version** in **CMOSF8H**, this identifier being "A" for the current version in CMOSF8L.

➔ *Example for M24128-BRMN6TP*

How can the change be seen?

- DEVICE MARKING

For the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **process technology** identifier is "**K**" for the **upgraded version** in **CMOSF8H**, this identifier being "A" for the current version in CMOSF8L:

	Upgraded M24128 CMOSF8H	Current M24128 CMOSF8L
SO8N Example: M24128-BRMN6TP	4128BRP PYWW**K**	4128BRP PYWW**A**

For the TSSOP8 package, the difference is visible inside the product name where the last digit is "**K**" for the **upgraded version** in **CMOSF8H**, this identifier being "P" for the current version in CMOSF8L:

	Upgraded M24128 CMOSF8H	Current M24128 CMOSF8L
TSSOP8 Example: M24128-BRDW6TP	428R**K** PYWW	428R**P** PYWW

For the MLP8 package, the product name is "4**GFK**" for the **upgraded version** in **CMOSF8H**, while the current version in CMOSF8L is "4**28F**":

	Upgraded M24128 CMOSF8H	Current M24128 CMOSF8L
MLP8 2x3 Example: M24128-BFMC6TG	4**GFK** PYWW	4**28F** PYWW

P = Assembly plant / country
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process technology code/ Wafer Fab ID

Appendix A- Product Change Information

Product family / Commercial products:	M24128 products family
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of design
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: (Notification to customer)	Week 33 / 2012
Forecast date of Qualification samples availability for customer(s):	See details on next page
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The intermediate **Qualification Report QRMMY1202** is available and included inside this document.
Marking to identify the changed product:	Process Technology identifier "**K"** for F8H
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 45 / 2012

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M24128-BRMN6P (*)	SO8N	No sample in tube
M24128-BRMN6TP (*)	SO8N	Available
M24128-BWMN6P	SO8N	No sample in tube
M24128-BWMN6TP	SO8N	Available
M24128-BRDW6TP (*)	TSSOP8	Available
M24128-BWDW6TP	TSSOP8	Available
M24128-BFMC6TG	MLP8 2x3	Available

(*) Following product line rationalization, we recommend customer to use **–R** version (1.8 V – 5.5 V) when –W (2.5 V – 5.5 V) is used.
For instance, **M24128-BRMN6TP should be preferred** to M24128-BWMN6TP.

- The following part number will not be kept in production, replacement part number is:

Current Commercial Part Numbers	Replacement Commercial Part Numbers	Package	Samples availability
M24128-BFM**B**6TG	M24128-BFM**C**6TG	MLP8 2x3	Available
M24128-**B**FCS6TP/**A**	M24128-**D**FCS6TP/**K**	WLCSP	November 2012

Appendix C: Qualification Report:

See following pages

QRMMY1202
Qualification report

New design / M24128-BR M24128-BW M24128-BF M24128-DF using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24128-BRMN6P M24128-BRMN6TP M24128-BWMN6P M24128-BWMN6TP M24128-BRDW6TP M24128-BWDW6TP M24128-BFMC6TG M24128-DFMC6TG M24128-DFCS6TP/K
Product description	128 Kbit serial I²C bus EEPROM
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
WLCSP	Subcon Stats ChipPac, Singapore	Subcon Stats ChipPac, Singapore

Reliability assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M24128 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for -BW devices
- 1.8 to 5.5 V at –40 to 85 °C for -BR devices
- 1.7 to 5.5 V at –40 to 85 °C for -BF and -DF devices

The CMOSF8H is a new advanced silicon process technology that is already qualified in the STMicroelectronics Rousset 8” diffusion plant, and is in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24C64/M95640 and M24C32/M95320 EEPROM products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The new design M24128 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed all reliability requirements.

Refer to *Section 3: Reliability test results* for details on the test results.

2 Device characteristics

Device description

The M24128-x devices are I²C-compatible electrically erasable programmable memories (EEPROM). They are organized as 16Kb × 8 bits.

The M24128-D also offers an additional page, named the Identification Page (128 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as it can be used to store unique identification parameters and/or parameters specific to the production line.

The device behaves as a slave in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and a Read/Write bit (RW) terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicles used for the die qualification are presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24128	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)
M95128 (2)	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. Die-oriented reliability tests mainly based on M95128 product (same silicon process technology, same design core between 128Kbit SPI and 128Kbit I2C, metal mask option for bus control).

The package qualifications were mainly obtained by similarity. The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95M02 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / Subcon Amkor
M24M01 (2)	CMOSF8H	ST Rousset 8”	TSSOP8	ST Shenzhen / Subcon Amkor
M24512	CMOSF8H	ST Rousset 8”	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / Subcon Amkor
M95M02 / M24512	CMOSF8H	ST Rousset 8”	WLCSP	Subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable to M24128.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable to M24128.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description						
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size	
						M95128	M24128
						Lot 1	Lot 2
EDR	High temperature operating life after endurance						
	AEC-Q100-005	400 000 E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	1	504 hrs	0/80	-
					1008 hrs	Results FC W30	
	Data retention after endurance						
	AEC-Q100-005	400 000 E/W cycles at 150 °C then: HTSL at 150 °C	80	1	504 hrs	0/80	-
					1008 hrs	Results FC W30	
LTOL	Low temperature operating life						
	JESD22-A108	–40 °C, 6 V	80	1	504 hrs	0/80	-
					1008 hrs	Results FC W30	
HTSL	High temperature storage life						
	JESD22-A103	Retention bake at 200 °C	80	1	504 hrs	0/80	-
					1008 hrs	Results FC W30	
WEB	Program/erase endurance cycling + bake						
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	5 Million cycles / 48 hrs	0/80	-
ESD HBM	Electrostatic discharge (human body model)						
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)						
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)						
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A	Class II - Level A

1. See *Table 8: List of terms* for a definition of abbreviations.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95M02 (2)			M24128
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable.
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24M01 (2)			M24128
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	400	3	N/A	0/400	0/400	0/400	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-Jul-2012	1	Initial release.

Document Revision History

Date	Rev.	Description of the Revision
July 11, 2012	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

M24128-BW
M24128-BR M24128-BF

128 Kbit serial I²C bus EEPROM

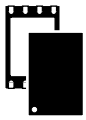
Features

- Supports the I²C bus modes:
  - 400 kHz Fast-mode
  - 100 kHz Standard-mode
- Single supply voltages:
  - 2.5 V to 5.5 V (M24128-BW)
  - 1.8 V to 5.5 V (M24128-BR)
  - 1.7 V to 5.5 V (M24128-BF)
- Write Control input
- Byte and Page Write
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 Million write cycles
- More than 40-year data retention
- Packages
  - ECOPACK2® (RoHS-compliant and Halogen-free)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

WLCSP (CS)



UFDFPN8
(MB, MC)

Contents

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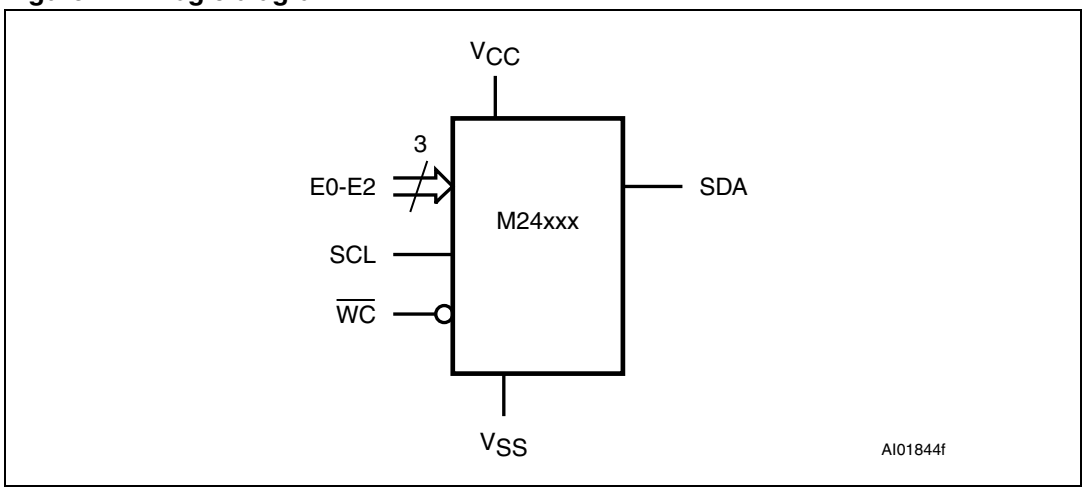
1 Description

The M24128-BW, M24128-BR and M24128-BF devices are I^{2}C-compatible electrically erasable programmable memories (EEPROM). They are organized as 16384 × 8 bits.

Figure 1. Logic diagram



I^{2}C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^{2}C bus definition.

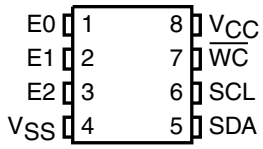
The device behaves as a slave in the I^{2}C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$) (as described in *Table 2*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 1. Signal names

Signal name	Function	Direction
E0, E1, E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections



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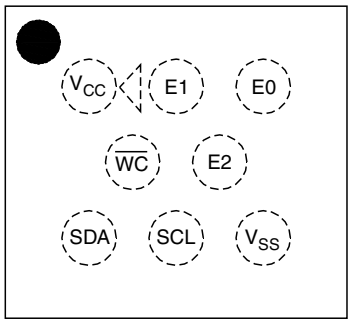
1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)



ai14799

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

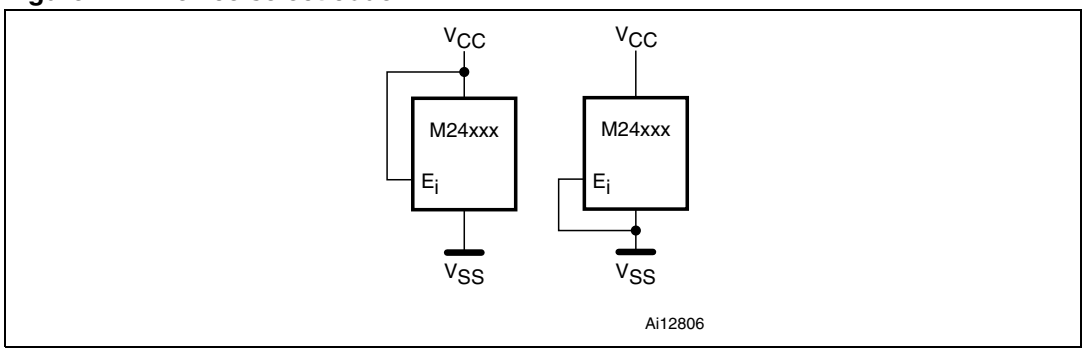
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 4*. When not connected (left floating), these inputs are read as low (0,0,0).

Figure 4. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven high, device select and Address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 7*, *Table 8* and *Table 9*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 7*, *Table 8* and *Table 9*. The rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8* and *Table 9*). Until V_{CC} passes over the POR threshold, the device is reset and in Standby Power mode.

In a similar way, during power-down (continuous decay of V_{CC}), as soon as V_{CC} drops below the POR threshold voltage, the device is reset and stops responding to any instruction sent to it.

2.6.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal Write cycle in progress).

Figure 5. Maximum R_P value versus bus parasitic capacitance (C) for an I^2C bus

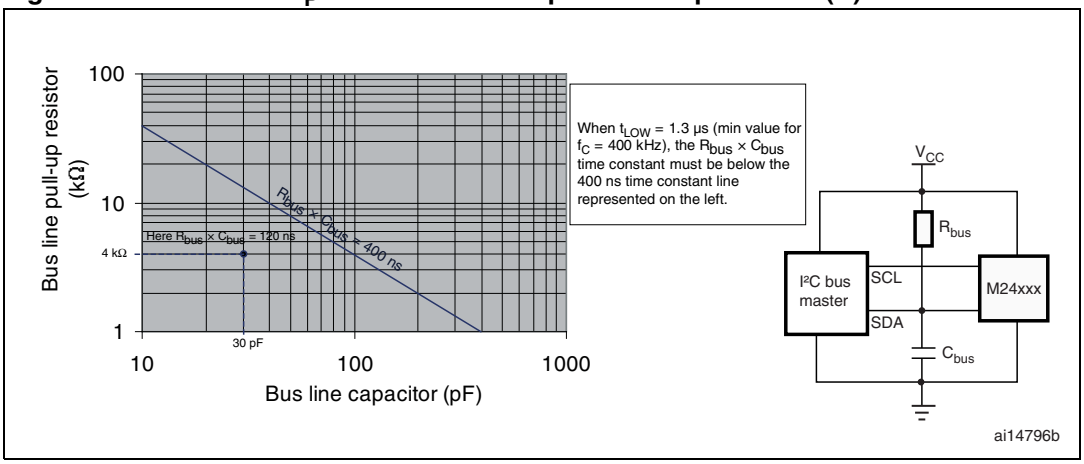


Figure 6. I^2C bus protocol

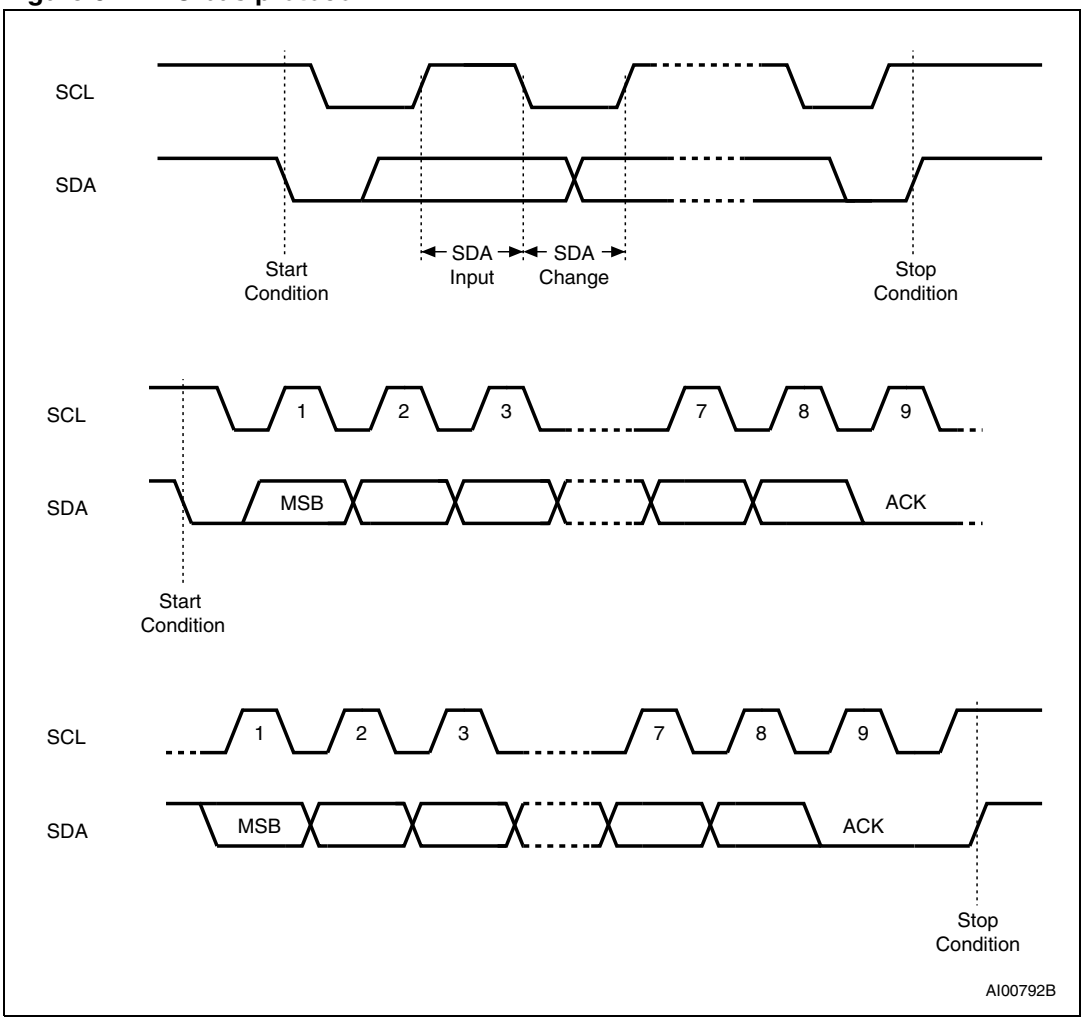


Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

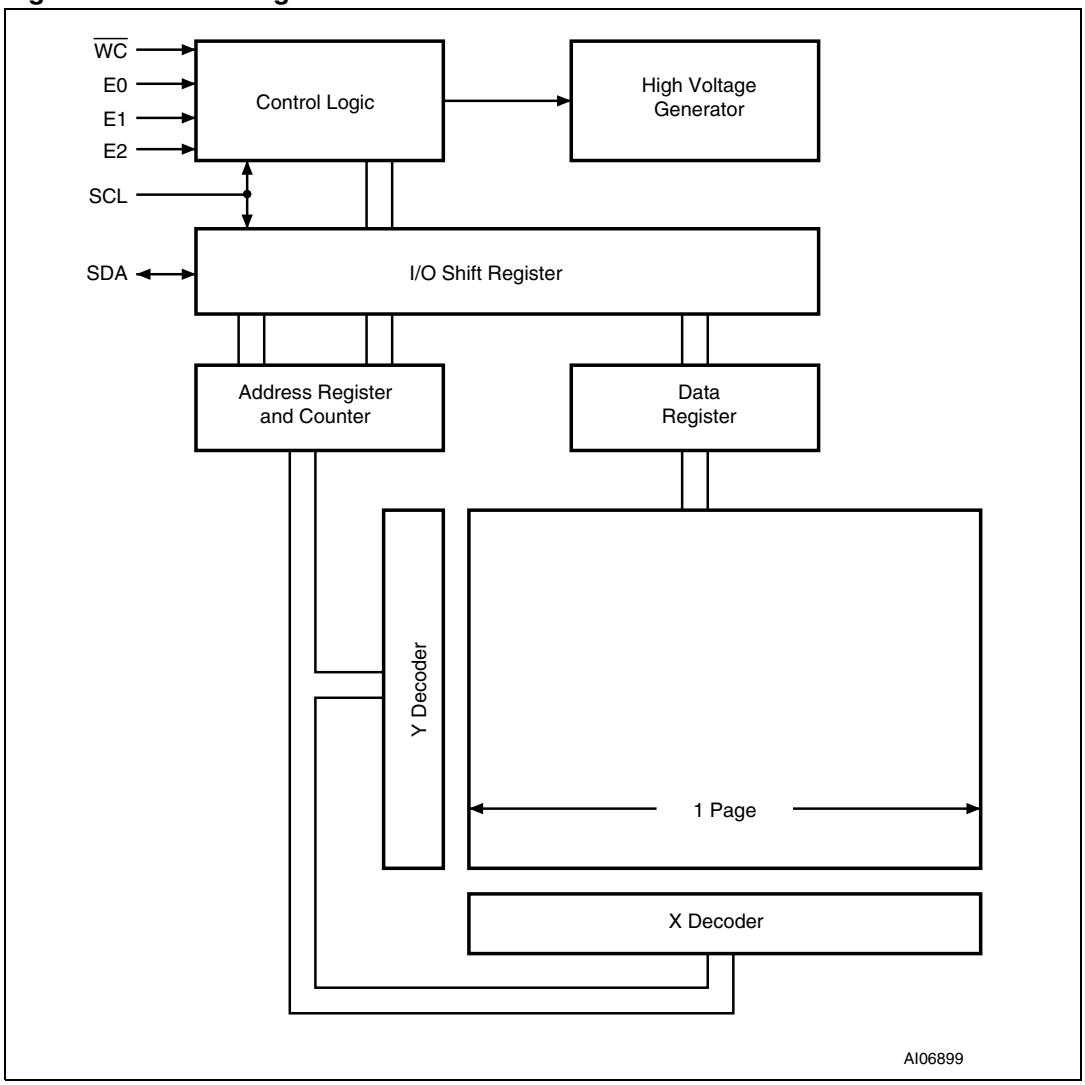
Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Memory organization

The memory is organized as shown in *Figure 7*.

Figure 7. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 6*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

4.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.4 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit device type identifier is 1010b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

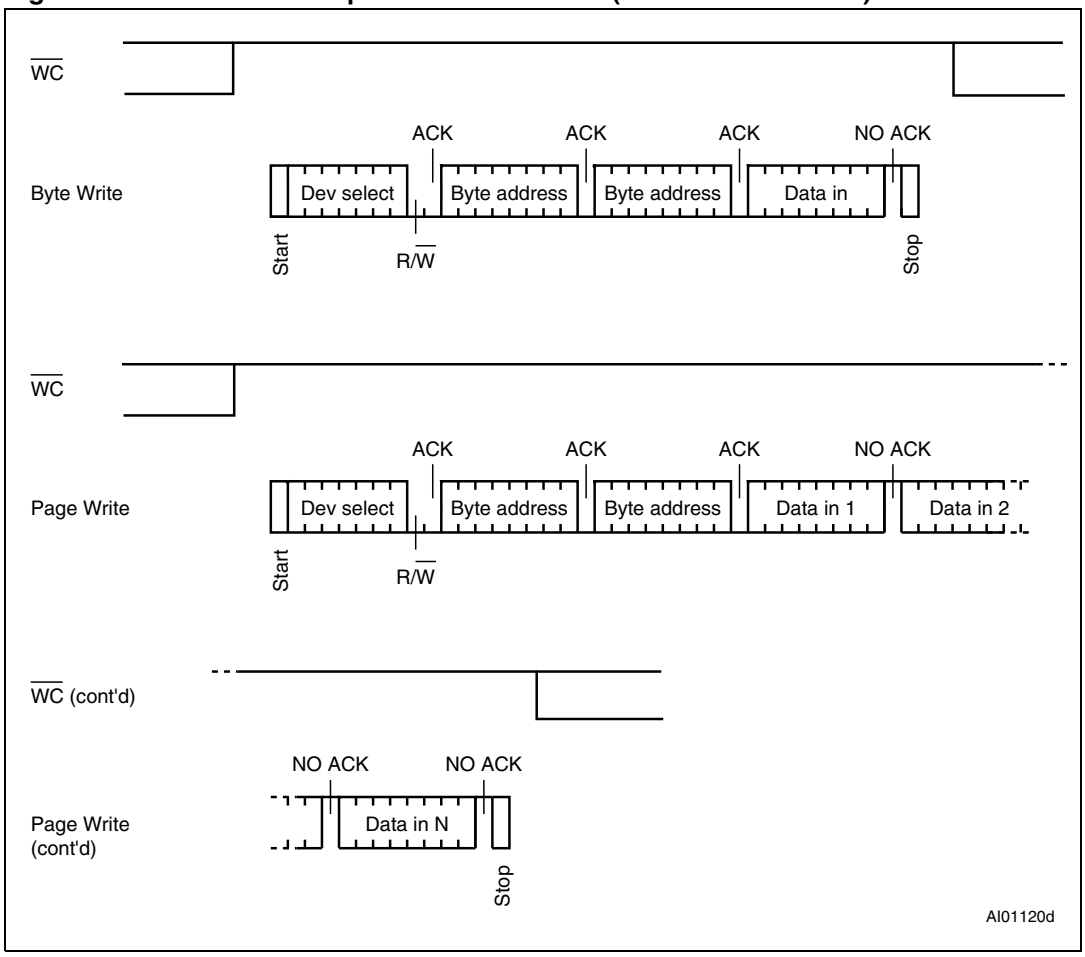
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 5. Operating modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$(1)	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	Start, device select, $\overline{\text{RW}}$ = 0, Address
	1	X		reStart, device select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤ 64	Start, device select, $\overline{\text{RW}}$ = 0

1. X = V_{IH} or V_{IL}.

Figure 8. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



4.6 Write operations

Following a Start condition the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit ($\text{R}\overline{\text{W}}$) reset to 0. The device acknowledges this, as shown in *Figure 9*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data Byte.

Writing to the memory may be inhibited if Write Control ($\overline{\text{WC}}$) is driven high. Any Write instruction with Write Control ($\overline{\text{WC}}$) driven high (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 8*.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 3*) is sent first, followed by the Least Significant Byte (*Table 4*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

4.7 Byte Write

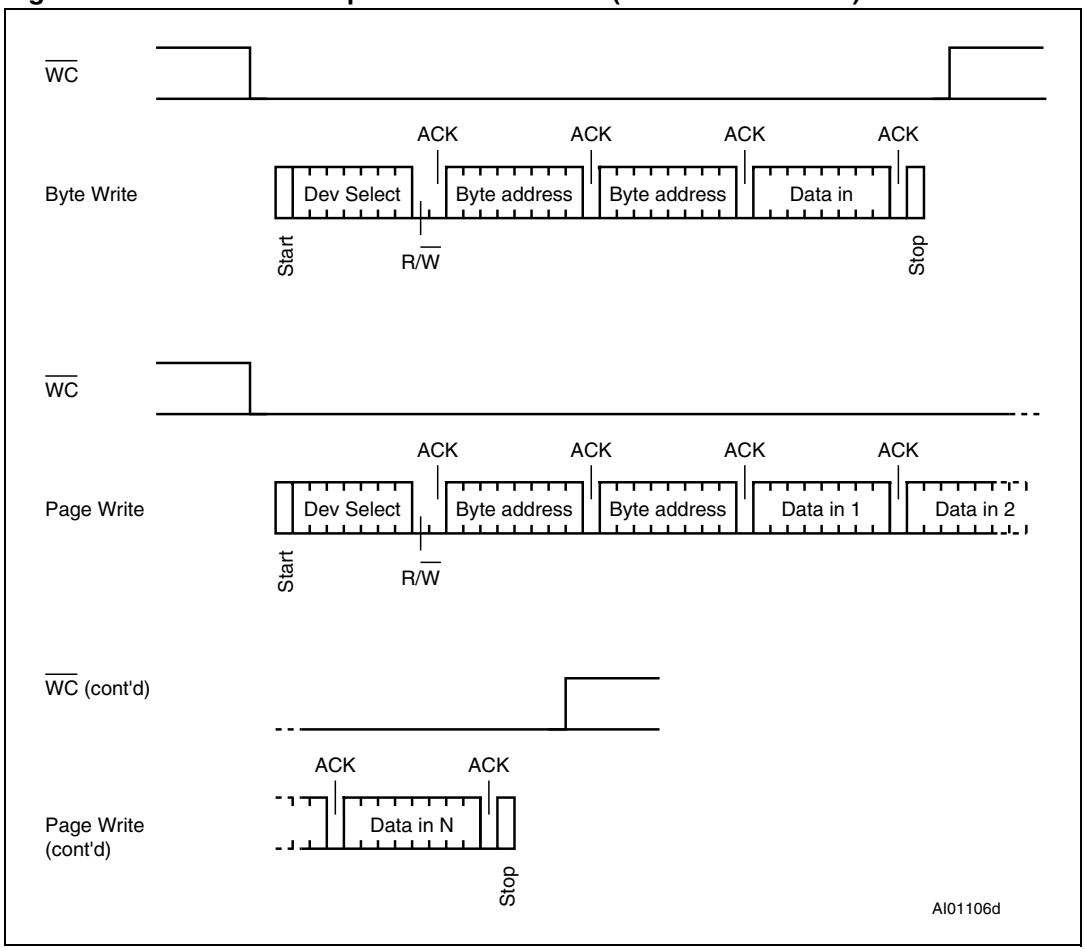
After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{\text{WC}}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 9*.

4.8 Page Write

The Page Write mode allows up to 64 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b13-b6) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 64 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{\text{WC}}$) is low. If Write Control ($\overline{\text{WC}}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (inside the page) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 9. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



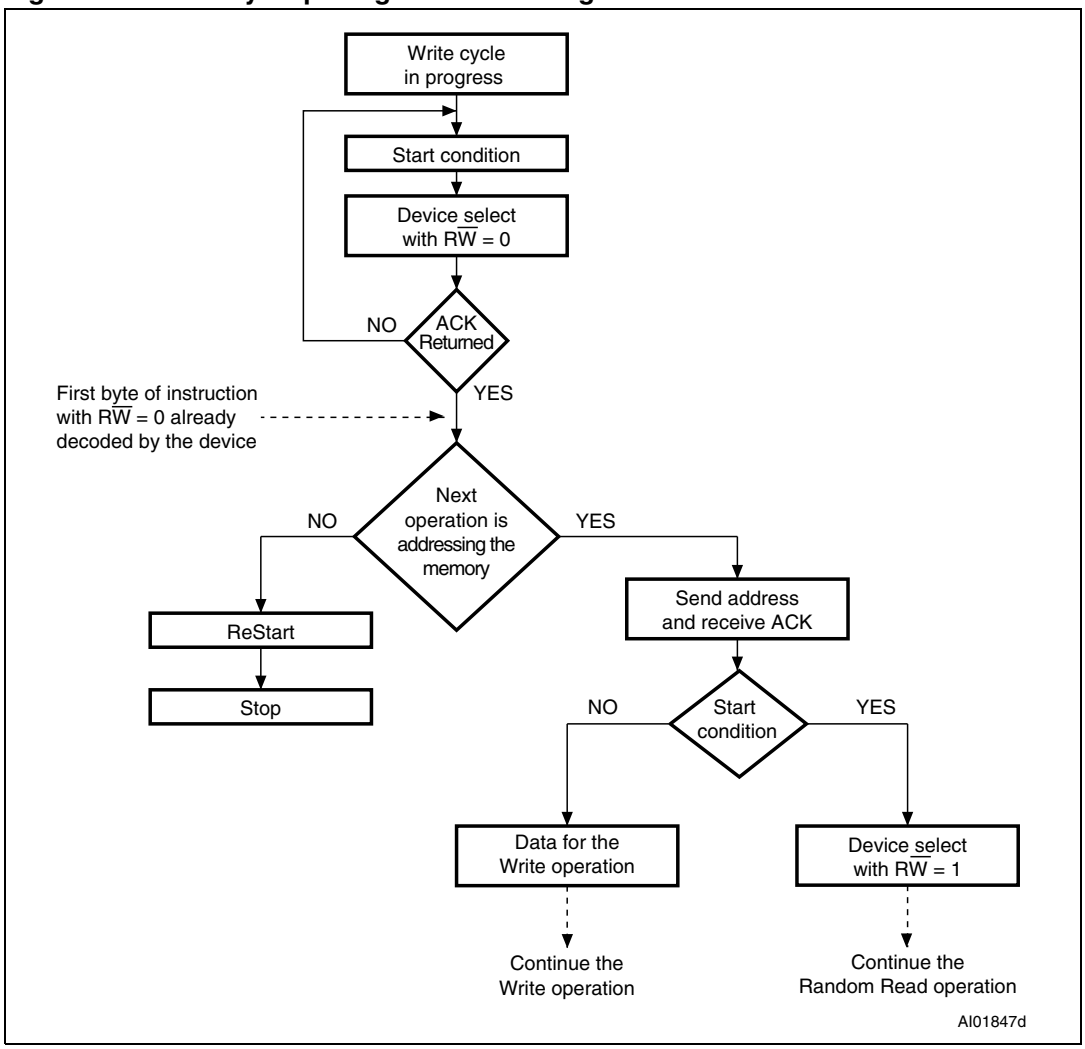
4.9 ECC (error correction code) and write cycling

The new M24128 devices offer an ECC (error correction code) logic which compares each 4-byte word with its six associated EEPROM ECC bits. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC word), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by packets of 4 bytes in order to benefit from the larger amount of write cycles.

All M24128 devices are qualified at 1 million (1 000 000) write cycles; the new M24128 devices offering the ECC improvement are qualified using a cycling routine that writes to the device by multiples of 4-byte words.

Figure 10. Write cycle polling flowchart using ACK



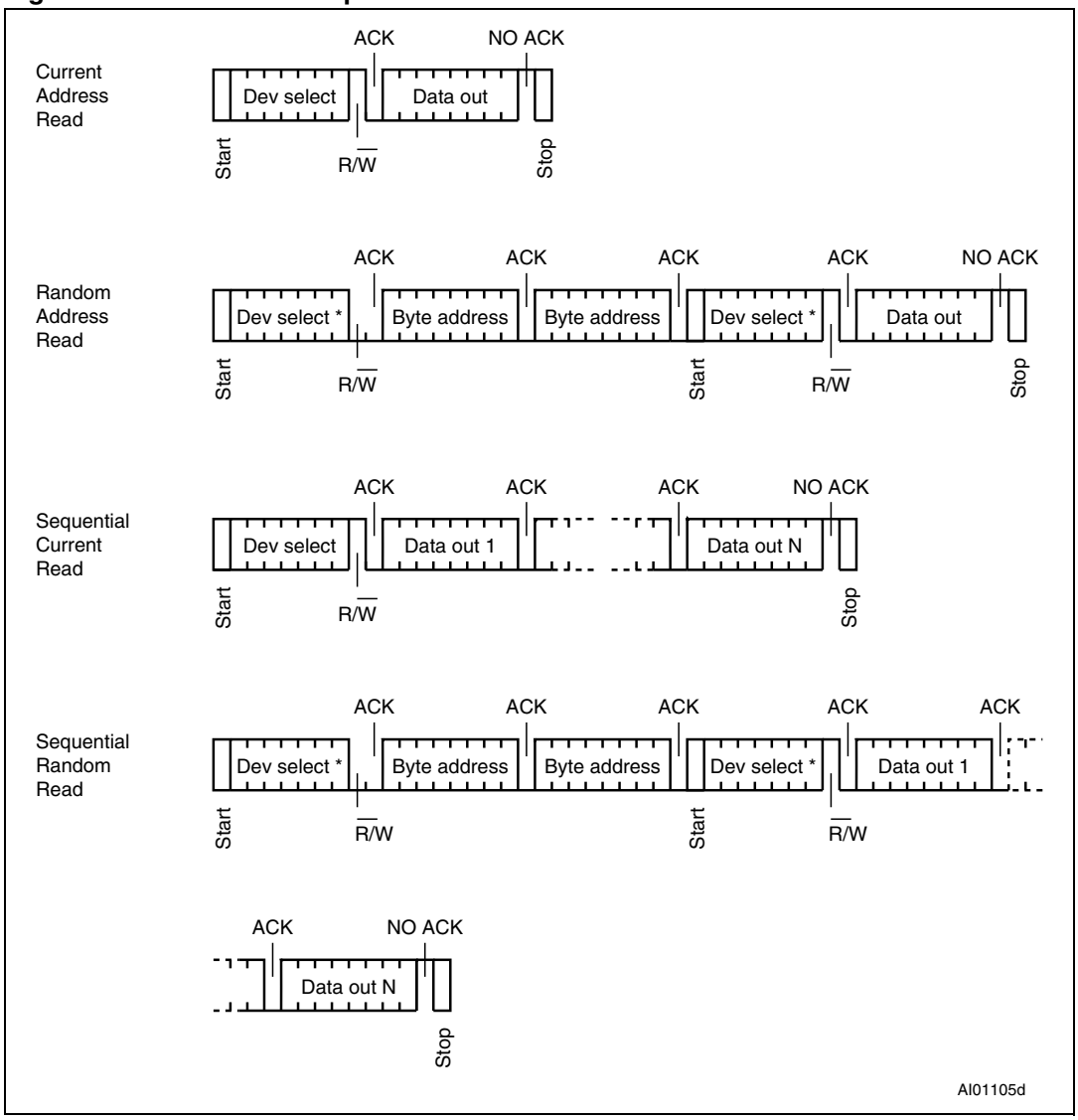
4.10 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 16*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

1. Initial condition: a Write cycle is in progress.
2. Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
3. Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 11. Read mode sequences



1. The seven most significant bits of the device select code of a Random Read (in the 1st and 4th bytes) must be identical.

4.11 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

4.12 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/$\overline{Write}$ bit (R$\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

4.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/$\overline{Write}$ bit (R$\overline{W}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the Byte.

4.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

4.15 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

5 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

6 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_{IO}	Input or output range	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500 Ω, R2=500 Ω)

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating conditions (M24xxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 8. Operating conditions (M24xxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. Operating conditions (M24xxx-F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 5)	–20	85	°C

Table 10. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 12. AC test measurement I/O waveform

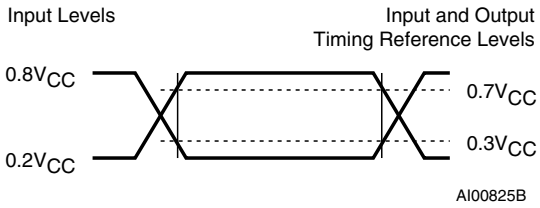


Table 11. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_{WCL}(1)	$\overline{WC}$ input impedance	$V_{IN} < 0.3V_{CC}$	50	200	kΩ
Z_{WCH}(1)	$\overline{WC}$ input impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}(1)	Pulse width ignored (Input filter on SCL and SDA)			100	ns

1. Characterized only.

Table 12. DC characteristics (M24xxx-W, device grade 6)

Symbol	Parameter	Test condition (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz		2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(1)	mA
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		5	µA
	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA)		$0.7V_{CC}$	6.5	V
	Input high voltage ($\overline{WC}$, E0, E1, E2)		$0.7V_{CC}$	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a Read command (after the Stop condition) or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write command).

Table 13. DC characteristics (M24xxx-W, device grade 3)

Symbol	Parameter	Test condition (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz		2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(1)	mA
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, 2.5 V < V_{CC} < 5.5 V		10	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA)		$0.7V_{CC}$	6.5	V
	Input high voltage ($\overline{WC}$, E0, E1, E2)		$0.7V_{CC}$	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a Read command (after the Stop condition) or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write command).

Table 14. DC characteristics (M24xxx-R - device grade 6)

Symbol	Parameter	Test condition (in addition to those in *Table 8*)(1)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c = 400 kHz		0.8	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V < V_{CC} < 2.5 V		3(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)		$0.7V_{CC}$	6.5	V
	Input high voltage ($\overline{WC}$, E0, E1, E2)		$0.7V_{CC}$	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V

1. If the application uses the M24128-BR at 2.5 V < V_{CC} < 5.5 V and –40 °C < T_A < +85 °C, please refer to *Table 12: DC characteristics (M24xxx-W, device grade 6)* instead of the above table.
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read command (after the Stop condition) or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write command).

Table 15. DC characteristics (M24xxx-F)

Symbol	Parameter	Test condition (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} =1.7 V, f_c = 400 kHz		0.8	mA
I_{CC0}	Supply current (Write)	During t_W, 1.7 V < V_{CC} < 2.5 V		3(1)	mA
I_{CC1}	Standby supply current	Device not selected(2), V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.7 V		1	µA
V_{IL}	Input low voltage (SDA, SCL, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)		0.7V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E0, E1, E2)		0.7V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} = 1.7 V		0.2	V

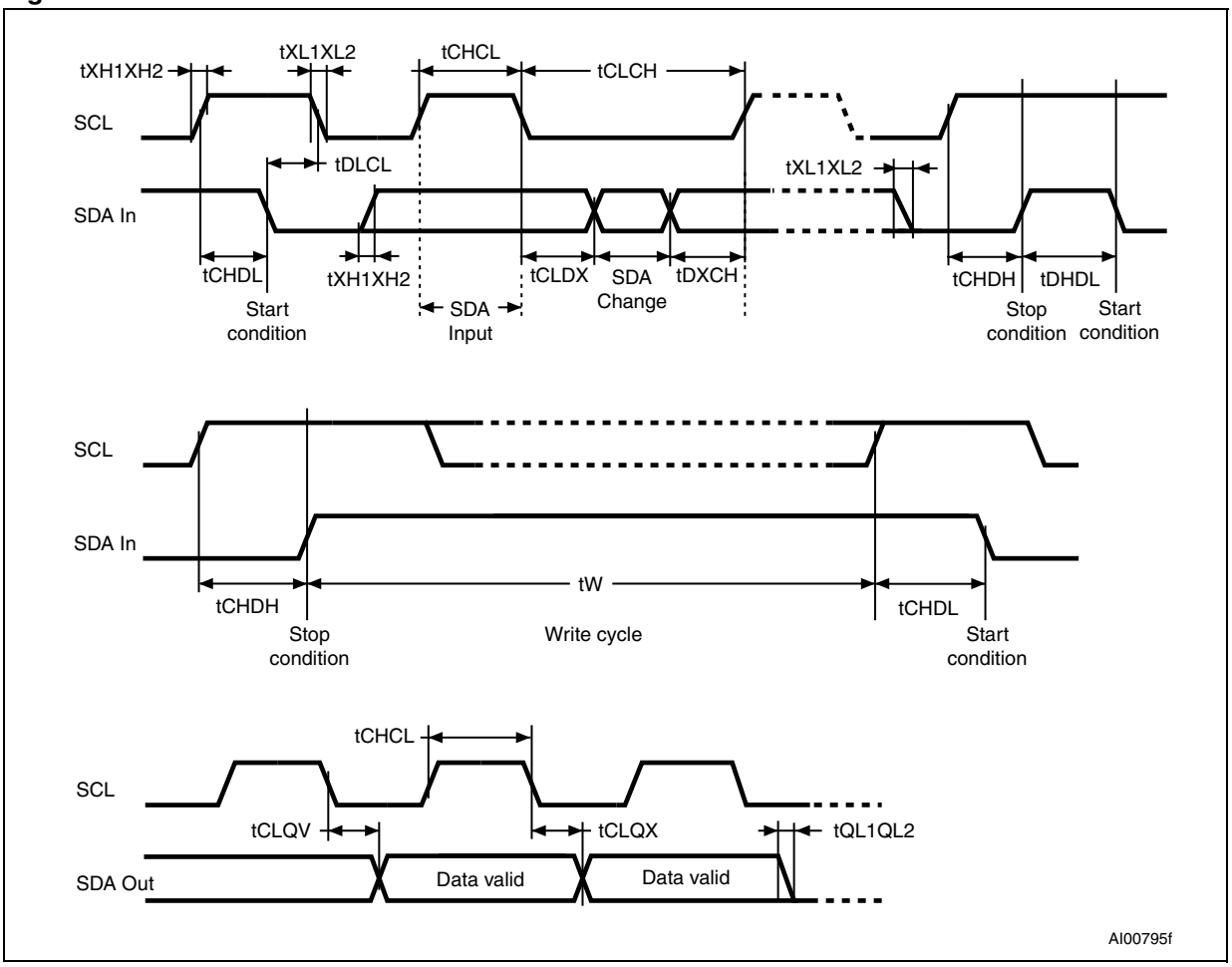
1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a Read command (after the Stop condition) or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write command).

Table 16. AC characteristics

Test conditions specified in *Table 7*, *Table 8* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	120	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}(4)(5)	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W	t_{WR}	Write time		5	ms

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 5*.

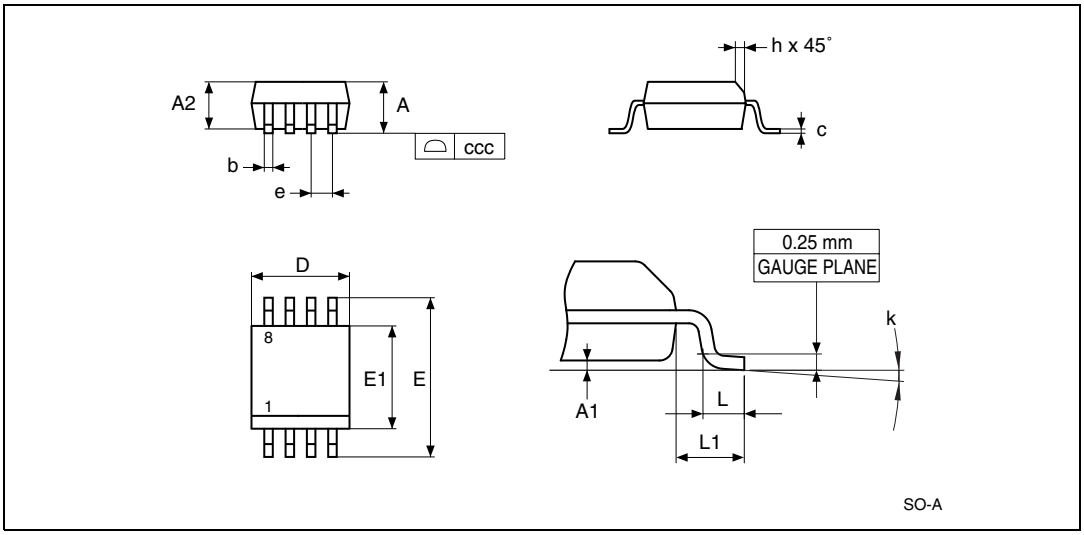
Figure 13. AC waveforms



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 17. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data

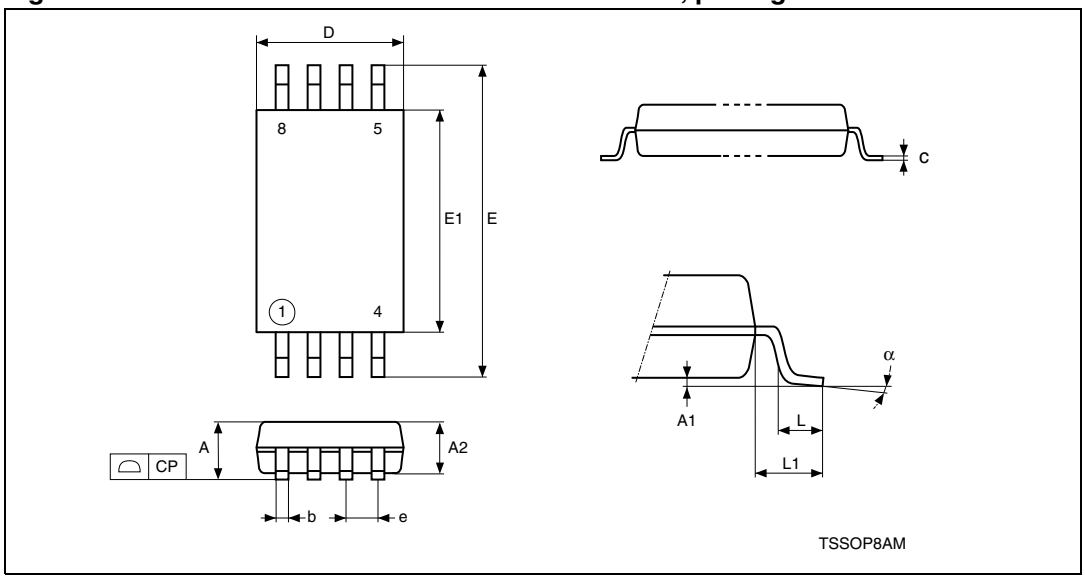
Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.10	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.0110	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.10			0.0039
D	4.90	4.80	5.00	0.1929	0.1890	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	–	–	0.0500	–	–
h		0.25	0.50			
k		0°	8°		0°	8°

Table 17. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
L		0.40	1.27		0.0157	0.0500
L1	1.04			0.0410		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 15. TSSOP8 – 8 lead thin shrink small outline, package outline



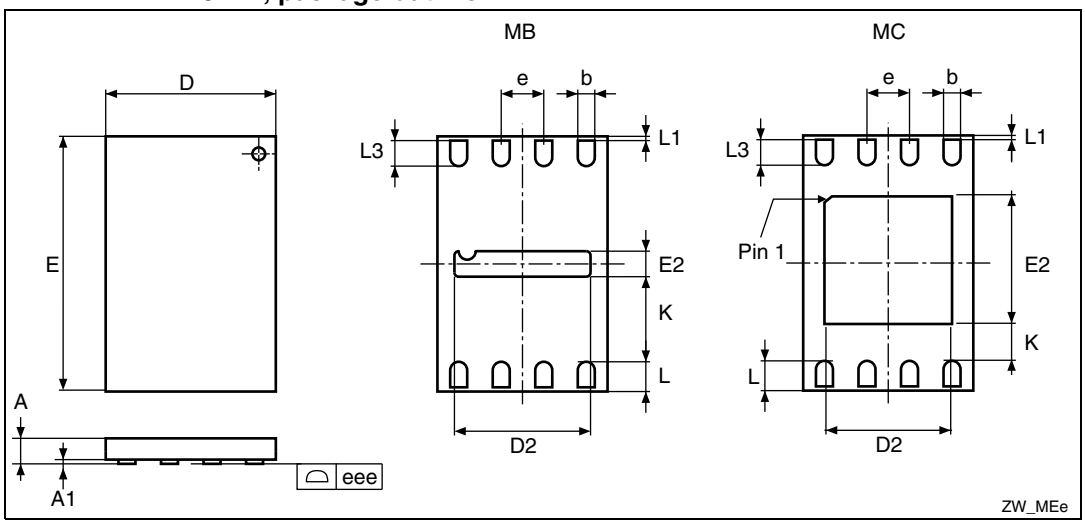
1. Drawing is not to scale.

Table 18. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 16. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package outline



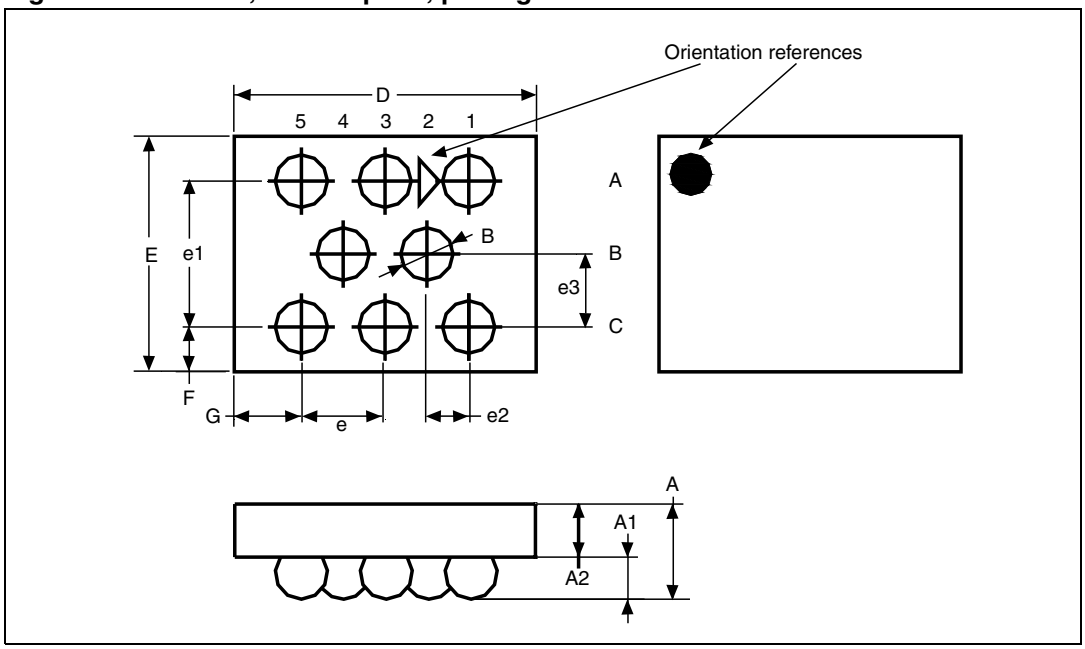
1. Drawing is not to scale.
2. The central pad (E2 × D2 area in the above illustration) is internally pulled to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

Table 19. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 17. WLCSP, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 20. WLCSP, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.585	0.535	0.635	0.0230	0.0211	0.0250
A1	0.230	0.205	0.255	0.0091	0.0081	0.0100
A2	0.355	0.330	0.380	0.0140	0.0130	0.0150
B	0.320	0.290	0.350	0.0126	0.0114	0.0138
D	1.805	1.785	1.825	0.0711	0.0703	0.0719
E	1.400	1.380	1.420	0.0551	0.0543	0.0559
e	0.5			0.0197		
e1	0.886			0.0349		
e2	0.250			0.0098		
e3	0.443			0.0174		
F	0.257			0.0101		
G	0.4025			0.0158		
N[2]	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. N is the total number of terminals.

9 Part numbering

Table 21. Ordering information scheme

Example: M24128–B W MN 6 T P /P

Device type

M24 = I^2C serial access EEPROM

Device function

128–B = 128 Kbit (16384 x 8)

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

R = V_{CC} = 1.8 V to 5.5 V

F = V_{CC} = 1.7 V to 5.5 V

Package

MN = SO8 (150 mil width)(1)

DW = TSSOP8 (169 mil width)(1)

MB or MC = UFDFPN8 (MLP8)(1)

CS = WLCSP(1)

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

3 = Automotive: device tested with high reliability certified flow(2) over –40 to 125°C.

Option

blank = standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(3)

P = F6DP26% Chartered

A = F8L Rousset (only for the WLCSP package)

1. ECOPACK2® (RoHS-compliant and Halogen-free).
2. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
3. Used only for device grade 3 and WLCSP packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

10 Revision history

Table 22. Document revision history

Date	Revision	Changes
22-Dec-1999	2.3	TSSOP8 package in place of TSSOP14 (pp 1, 2, OrderingInfo, PackageMechData).
28-Jun-2000	2.4	TSSOP8 package data corrected
31-Oct-2000	2.5	References to Temperature Range 3 removed from Ordering Information Voltage range -S added, and range -R removed from text and tables throughout.
20-Apr-2001	2.6	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated
16-Jan-2002	2.7	Test condition for I_{LI} made more precise, and value of I_{LI} for E2-E0 and $\overline{WC}$ added -R voltage range added
02-Aug-2002	2.8	Document reformatted using new template. TSSOP8 (3x3mm² body size) package (MSOP8) added. 5ms write time offered for 5V and 2.5V devices
04-Feb-2003	2.9	SO8W package removed. -S voltage range removed
27-May-2003	2.10	TSSOP8 (3x3mm² body size) package (MSOP8) removed
22-Oct-2003	3.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. V_{IL}(min) improved to -0.45V.
01-Jun-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade clarified
04-Nov-2004	5.0	Product List summary table added. Device Grade 3 added. 4.5-5.5V range is Not for New Design. Some minor wording changes. AEC-Q100-002 compliance. t_{NS}(max) changed. V_{IL}(min) is the same on all input pins of the device. Z_{WCL} changed.
05-Jan-2005	6.0	UFDFPN8 package added. Small text changes.

Table 22. Document revision history (continued)

Date	Revision	Changes
29-Jun-2006	7	Document converted to new ST template. M24C32 and M24C64 products (4.5 to 5.5V supply voltage) removed. M24C64 and M24C32 products (1.7 to 5.5V supply voltage) added. *Section 2.3: Chip Enable (E0, E1, E2)* and *Section 2.4: Write Control (WC)* modified, *Section 2.6: Supply voltage (V_{CC})* added and replaces *Power On Reset: VCC Lock-Out Write Protect* section. T_A added, *Note 1* updated and T_{LEAD} specified for PDIP packages in *Table 6: Absolute maximum ratings*. I_{CC0} added, I_{CC} voltage conditions changed and I_{CC1} specified over the whole voltage range in *Table 12: DC characteristics (M24xxx-W, device grade 6)*. I_{CC0} added, I_{CC} frequency conditions changed and I_{CC1} specified over the whole voltage range in *Table 14: DC characteristics (M24xxx-R - device grade 6)*. t_W modified in *Table 16: AC characteristics*. SO8N package specifications updated (see *Figure 14* and *Table 17*). Device grade 5 added, B and P Process letters added to *Table 21: Ordering information scheme*. Small text changes.
03-Jul-2006	8	I_{CC1} modified in *Table 12: DC characteristics (M24xxx-W, device grade 6)*. *Note 1* added to *Table 15: DC characteristics (M24xxx-F)* and table title modified.
17-Oct-2006	9	UFDFPN8 package specifications updated (see *Table 19*). M24128-BW- and M24128-BR part numbers added. Generic part number corrected in *Features on page 1*. I_{CC0} corrected in *Table 13* and *Table 12*. Packages are ECOPACK® compliant.
27-Apr-2007	10	Available packages and temperature ranges by product specified in *Table 22*, *Table 24* and *Table 25*. Notes modified below *Table 11: Input parameters*. V_{IH} max modified in DC characteristics tables (see *Table 12*, *Table 13*, *Table 14* and *Table 15*). C process code added to *Table 21: Ordering information scheme*. For M24xxx-R (1.8 V to 5.5 V range) products assembled from July 2007 on, t_W will be 5 ms (see *Table 16: AC characteristics*.
27-Nov-2007	11	Small text changes. *Section 2.5: V_{SS} ground* and *Section 4.9: ECC (error correction code) and write cycling* added. V_{IL} and V_{IH} modified in *Table 14: DC characteristics (M24xxx-R - device grade 6)*. JEDEC standard reference updated below *Table 6: Absolute maximum ratings*. Package mechanical data inch values calculated from mm and rounded to 4 decimal digits (see *Section 8: Package mechanical data*).

Table 22. Document revision history (continued)

Date	Revision	Changes
18-Dec-2007	12	Added *Section 2.6.2: Power-up conditions*, updated *Section 2.6.3: Device reset*, and *Section 2.6.4: Power-down conditions* in *Section 2.6: Supply voltage (V_{CC})*. Updated *Figure 5: Maximum R_P value versus bus parasitic capacitance (C) for an I^2C bus*. Replace M24128 and M24C64 by M24128-BFMB6 and M24C64-FMB6, respectively, in *Section 4.9: ECC (error correction code) and write cycling*. Added temperature grade 6 in *Table 9: Operating conditions (M24xxx-F)*. Updated test conditions for I_{LO} and V_{LO} in *Table 12: DC characteristics (M24xxx-W, device grade 6)*, *Table 13: DC characteristics (M24xxx-W, device grade 3)*, and *Table 14: DC characteristics (M24xxx-R - device grade 6)*. Test condition updated for I_{LO}, and V_{IH} and V_{IL} differentiate for 1.8 V ≤ V_{CC} < 2.5 V and 2.5 V ≤ V_{CC} < 5.5 V in *Table 15: DC characteristics (M24xxx-F)*. Updated *Table 16: AC characteristics*, and *Table 17: AC characteristics (M24xxx-F)*. Updated *Figure 13: AC waveforms*. Added M24128-BF in *Table 25: Available M24C32 products (package, voltage range, temperature grade)*. Process B removed from *Table 21: Ordering information scheme*.
30-May-2008	13	Small text changes. C *Process* option and Blank *Plating technology* option removed from *Table 21: Ordering information scheme*.
15-Jul-2008	14	WLCSP package added (see *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* and *Section 8: Package mechanical data*). *Section 4.9: ECC (error correction code) and write cycling* updated.
16-Sep-2008	15	I_{OL} added to *Table 6: Absolute maximum ratings*. *Table 24: Available M24C32 products (package, voltage range, temperature grade)* and *Table 25: Available M24C32 products (package, voltage range, temperature grade)* updated.
05-Jan-2009	16	I2C modes supported specified in *Features on page 1*. Note removed from *Table 15: DC characteristics (M24xxx-F)*. Small text changes.

Table 22. Document revision history (continued)

Date	Revision	Changes
10-Dec-2009	17	32 and 64 Kbit densities removed. ECOPACK status of packages specified *on page 1* and in *Table 21: Ordering information scheme*. *Section 2.6.2: Power-up conditions* updated. *Figure 5: Maximum R_P value versus bus parasitic capacitance (C) for an I^2C bus* updated. t_{NS} modified in *Table 11: Input parameters*. I_{CC1} and V_{IH} updated in *Table 12: DC characteristics (M24xxx-W, device grade 6)*, *Table 13: DC characteristics (M24xxx-W, device grade 3)*, *Table 14: DC characteristics (M24xxx-R - device grade 6)* and *Table 15: DC characteristics (M24xxx-F)*. Note added to *Table 14: DC characteristics (M24xxx-R - device grade 6)*. *Table 16: AC characteristics* modified. *Figure 13: AC waveforms* modified. Note added below *Figure 16: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3mm, package outline*. Small text changes.
12-Jan-2010	18	*Section 4.9: ECC (error correction code) and write cycling* modified.
23-Mar-2010	19	Removed PDIP package.
24-Nov-2011	20	Updated UFDFPN8 silhouette on cover page, *Figure 16: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3mm, package outline* and *Table 19: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data* to add MC version. Renamed *Figure 2: 8-pin package connections*. Removed “Available M24128 products“ table. Updated disclaimer on last page.

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