New patent specification

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First, the new name: (Chinese / English)

Peak capture and correction circuit

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Fourth, STATED

□ advocates of the Patent Law Article 22, item □ first paragraph or □ the fact that the provisions of the second paragraph, the date of its facts: date

□ before application to the following countries (regions) Patent Application:

[Please follow the format: receiving countries (regions), the filing date, docket number, sequence annotation]

□ assertive Patent Law Article 27 of the first international priority:

□ No advocate of the Patent Law Article 27 of the first international priority:

□ advocates of the Patent Law Article 29 The first domestic priority:

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□ Article 30 of the Patent Law advocated biological materials:

□ shall be deposited biological material by:

Domestic biomaterials [Please follow the format: depositary institution, date, number, sequence annotation]

foreign biological material [Please follow the format: Storage countries, institutions, dates, numbers, sequence annotation]

□ do not need to register the biological material by: Those skilled person having knowledge usually readily available, you do not need to register.

Fifth, the Chinese invention summary:

The creative department has about a peak capture and correction circuit, mainly as a digital meter peak in the signal acquisition and correction circuit that utilizes an integrated circuit and a capacitor embodiment, the external circuit

amplifier and a switch circuit, the input terminal of the operational amplifier are connected to a fed back into the first voltage and said operational amplifier is connected to the output terminal of said switching circuit, said a second switching circuit output voltage, and is connected to the capacitor; fewer parts used in this creation, the production of low cost, value for money, to avoid the conventional peak capture circuit using the diode is not easy to obtain, and the slow speed, Lack large power consumption.

Six English invention summary:

Seven designated representative figure:

(A) case designated representative Pictured:

(B) The symbol element representative diagram of a simple explanation:

Eight new instructions:

Description:

(a) Technical Field Creation: The creation relates to a peak capture (peak hold) and correction circuit, in particular, relates to a use of VLSI (verylarge scale integration; VLSI) implementation of digital meter peak signal capture and measurement circuit calibration (calibration) circuit.

(B) Background Art Creation: Press, For an electronic circuit system, the peak capture circuit (peakhold circuit) is used to measure the analog input signal voltage maxima and the voltage minima, which was prepared using the peak maximum value (the Peak max.) circuit and a minimum peak (Peak min.) circuit. See Figure 1 below, the input signal line painted define the maximum and minimum values are shown. Current measuring input analog signal voltage peak maximum and minimum values of the capture circuit is implemented utilizing discrete components (discretecomponents).

See further shown in Figure 2, which illustrates the general line of the peak capture circuit for measuring maximum and minimum values of the input signal voltage, wherein Figure II A system for the peak maxima circuit 10, and Figure II B line is the minimum value of the peak circuit 20.

II A, the maximum peak value circuit 10 comprises an operational amplifier 12, a diode 14 and a capacitor 16. Input terminal IN from the non-inverting input terminal of the operational amplifier 12 into the inverting input is connected to the feed-back, and the output terminal of the operational amplifier 12 is connected to the positive terminal of diode 14.

When the input voltage VIN is greater than the output voltage VOUT, the output of the operational amplifier 12 is "high" logic state, diode 14 turns on, the output voltage V_{OUT} will follow (follow) the input voltage $V_{the\ IN}$, that is, the output voltage V_{OUT} will be equal to the input voltage $V_{the\ IN}$.

And, when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is low, the output of the operational amplifier 12 is "low" logic state, diode 14 is not turned on, the capacitor 14 the output voltage V_{OUT} voltage sustain; just type voltage $V_{the\ IN}$ again higher than the output voltage V_{OUT} , the output voltage V_{OUT} will again follow the input voltage $V_{the\ IN}$.

Again, the minimum value of two peaks in Figure B circuit 20 includes an operational amplifier 22, a diode 24 and a capacitor 26. Input terminal IN from the non-inverting input terminal of the operational amplifier 22 into the inverting input is connected to the feed-back, and the output terminal of the operational amplifier 22 is connected to the negative terminal 24 of the diode.

When the input voltage $V_{the\ IN}$ less than the output voltage V_{OUT} , the output of the operational amplifier 22 is "low" logic state, diode 24 turns on, the output voltage V_{OUT} will follow (follow) the input voltage $V_{the\ IN}$, that is, the output voltage V_{OUT} It will be equal to the input voltage $V_{the\ IN}$.

And, when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is high, the output of the operational amplifier 22 is "high" logic state, diode 24 is not turned on, the output voltage V_{OUT} is maintained live; as long as the input voltage $V_{the\ IN}$ again lower than the output voltage V_{OUT} , the output voltage V_{OUT} will again follow the input voltage $V_{the\ IN}$.

However, since the peak of conventional capture circuit for diode characteristics demanding diodes used must be turned on / off (turn on / off) speed, small parasitic capacitance, leakage current, it is not easy to obtain . In addition, with this capacitance diodes used, it generally takes a larger holding (holding) capacitor, it is usually not easy to capture the signal speed work fast, and power consumption are relatively large.

Peak of the implementation of the above-described circuits using discrete components to capture, an operational amplifier, diode capacitance and a combination of parts used in the more, in addition to the high cost of production, the less cost-effective than, diode also not easy to obtain, and the slower, power consumption is large.

(C) the creation of a brief description: In view of the deletion of the above conventional art, the creator is made the peak having a number Multimeter in the signal of the capture and correction circuit, which can effectively solve the above conventional technique deletion of this creation, namely: The Creation an object

conventional discrete components to implement it, and may cause diode is not easy to obtain, and the slower, power consumption is a big problem, but may reduce production of the costs.

To achieve the above purpose, the creation of the Department of one kind of digital signal meter peak capture circuit that takes advantage of an integrated circuit and a capacitor embodiment, the external circuit of the capacitor product, the integrated circuit comprises an operational amplifier, a capacitor and a switch circuit, the input terminal of the operational amplifier are connected to a fed back into the first voltage and said operational amplifier is connected to the output terminal of the switching circuit, the switching circuit outputs a second voltage, and is connected to the capacitor; fewer parts used in this creation, the production of low cost, value for money, to avoid the conventional diode is not easy to obtain, and the slower the speed, the power consumption of large deletions.

Preferably by the switching circuit comprises a transistor, can provide enough current to charge the capacitor.

Preferably by the digital signal meter peak capture circuit may further comprises a resistor, the resistance of the transistor connected to the second voltage will avoid exceeding (overshouting) phenomenon.

Preferably by the electrical system as a crystalline N-channel transistors, the operation of the non-inverting input of the amplifier into the first voltage, the operational amplifier and the inverting input terminal connected to the feed back, and said gate output of the operational amplifier is connected to the N-channel transistor pole.

Are preferred, the drain terminals of N-channel transistors connected to the highest potential of the circuit, a source connected to one end of said resistor, said resistor and the other end connected to said capacitor, said capacitor into the circuit of a low heteroatom News DC voltage.

It is preferred, before entering the measuring said second voltage is set to be lower than the minimum of the effective potential of the potential measurement range.

Preferably those in the first voltage is greater than the second voltage, the output of the operational amplifier is "high" logic state, the N-channel transistor turns on, the second voltage follower (follow) the first voltage.

Preferably person, when comparing the first voltage and the second voltage is low, the output of the operational amplifier is "low" logic state, the N-channel transistor is turned off, the voltage of the second capacitor sustain.

It is preferred, and then when the first voltage is higher than the second voltage, the second voltage will be the first voltage follower.

Preferably by the electrical system of a crystalline P-channel transistor, the operational amplifier non-inverting input voltage into the first, the operation inverting input terminal connected to an amplifier and fed back, and said the output terminal of the operational amplifier is connected to the P-channel transistor gate.

Are preferred, drain terminals of the P-channel transistor is connected to the lowest potential of the circuit, a source connected to one end of said resistor, said resistor and the other end connected to said capacitor, said capacitor into the circuit of a low heteroatom News DC voltage.

Are preferred, before entering the measuring said second voltage is set to a potential higher than the maximum effective range of measurement of the potential.

Preferably those in the first voltage is less than the second voltage, the output of the operational amplifier is " ,, a low logic state, the P-channel transistor turns on, the second voltage follower (the Follow) of said first voltage.

Preferably person, when comparing the first voltage and the second voltage is high, the output of the operational amplifier is "high" logic state, the P-channel transistor is turned off, the second voltage sustain.

It is preferred, and then when the first voltage is lower than said second voltage, the second voltage will be the first voltage follower.

Preferably by the electrical system of a crystalline P-channel transistor, the operational amplifier inverting input terminal into said first voltage, the operational amplifier non-inverting input is connected with the feed-back, and the the output terminal of the operational amplifier is connected to the P-channel transistor gate.

Preferably person, the source terminal of the P-channel transistor is connected to the highest potential of the circuit, the drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitor to the circuit in a low miscellaneous News DC voltage.

It is preferred, before entering the measuring said second voltage is set to be lower than the minimum of the effective potential of the potential measurement range.

Who preferred, when the first voltage is greater than the second voltage, the operational amplifier output is "low" logic state, the P-channel transistor turns on, the second voltage may be fast to keep up with the said first voltage.

Are preferred when said first voltage is lower than said second voltage, the output of the operational amplifier is logic "high" state, the P-channel transistor is turned off, the voltage of the second capacitor voltage sustain.

It is preferred, and then when the first voltage is higher than the second voltage, the second voltage will be the first voltage follower.

Are preferred, the electrical system for the crystalline N-channel transistor, the inverting input terminal of the operational amplifier enters the first voltage, the operational amplifier is fed back to the non-inverting input terminal is

N-channel transistor pole.
Preferably person, the source terminal of the N-channel transistor is connected to the lowest potential of the circuit, the drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitor to the circuit in a low miscellaneous News DC voltage.
Are preferred, before entering the measuring said second voltage is set to a potential higher than the maximum effective range of measurement of the potential.
Who preferred substrate of the N-channel transistor (substrate) circuit connected to the lowest potential.
Preferably those in the first voltage is less than the second voltage, the output of the operational amplifier is "high" logic state, the N-channel transistor turns on, the second voltage can quickly follow (follow) of said first voltage.
Preferably person, when comparing the first voltage and the second voltage is high, the output of the operational amplifier is "low" logic state, the N-channel transistor is turned off, the second voltage sustain.
It is preferred, and then when the first voltage is lower than said second voltage, the second voltage will be the first voltage follower.
The creation of the peak meter digital signals capture and correction circuit, takes advantage of an integrated circuit and a capacitor embodiment, the external circuit of the capacitor product, the integrated circuit comprises an operational amplifier, a transistor and a resistance, the operational amplifier is connected to the inverting input of the circuit in a low noise dc voltage, the non-inverting input terminal is connected with the feed-back, and the gate of the operational amplifier connected to the output electrode of the transistor, the transistor can supply enough current to charge the capacitor, the resistor is connected between the transistor and the capacitor, to avoid a second output voltage of the phenomenon will be over.
Preferably by the electrical system of crystal P-channel transistor, the source of the P-channel transistor terminal connected to the highest potential of the circuit, the drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitance to the circuit in a low-noise DC voltage.
Preferably who, because of the operational amplifier circuit connected to the inverting input of a low noise dc voltage (GND), a non-inverting input terminal is connected with the feed-back, so is the output voltage of the op amp's input offset voltage (input offset voltage).
Preferably by the electrical system of crystal N-channel transistor, the source of the N-channel transistor terminal connected to the lowest potential of the circuit, the drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitance to the circuit in a low-noise DC voltage.
Who preferred substrate of the N-channel transistor (substrate) circuit connected to the lowest potential.
Preferably who, because of the operational amplifier circuit connected to the inverting input of a low noise dc voltage (GND), a non-inverting input terminal is connected with the feed-back, so is the output voltage of the op amp's input offset voltage (input offset voltage).
To give you a review committee for the creation of features of the case, the purpose and effect can have a better understanding and awareness of, hereby drawings with details such as the rear:
drawings Brief Description of
view of a system maximum and minimum values of the input signal depicted the definition.
Detailed circuit diagram of the peak capture circuit peak maxima circuit of Figure II A of the conventional system depicted.
Detailed circuit diagram of the peak minimum circuits Figure II B system depicted conventional peak capture circuit.
Figure III Series A detailed circuit diagram depicts the creation of the first preferred embodiment of the digital signal meter measuring the peak capture circuit peak maxima circuits.
Detailed circuit diagram of Figure III B line depicts the creation of the first preferred digital signal meter peak capture measurement circuit of the embodiment of the peak minimum circuits.
A detailed circuit diagram of Figure IV line depicts the creation of the second preferred digital signal meter peak capture measurement circuit of the embodiment of the peak maxima circuits.
Detailed circuit diagram of Figure IV B line depicts the creation of the second preferred digital signal meter peak capture measurement circuit of the embodiment of the peak minimum circuits.
Figure V Series A detailed circuit diagram depicts the creation of the third preferred digital meter calibration signal peak capture circuit peak maxima of the embodiment of the circuit.
Figure V B based detailed circuit diagram of the peak value of the minimum circuits depicted in this digital creation of a third preferred embodiment of the meter peak signal to retrieve the calibration circuit.
Figure VI line depicts the creation of the third preferred digital meter calibration circuit calibration signal peak retrieve a timing diagram of the embodiment.
Symbol Description The main element
10. . . Circuit peak maxima
14. . . Diode

24. . . Diode
30. . . Circuit peak maxima
34N. . . Channel transistor
38. . . Resistor
42. . . Operational amplifier
46. . . Capacitance
50. . . Circuit peak maxima
54P. . . Channel transistor
58. . . Resistor
62. . . Operational amplifier
66. . . Capacitance
12. . . Operational amplifier
16. . . Capacitance
22. . . An operational amplifier
26. . . Capacitance
32. . . The operational amplifier
36. . . Capacitance
40. . . Circuit peak minima
44P. . . Channel transistor
48. . . Resistor
52. . . Operational amplifier
56. . . Capacitance
60. . . Circuit peak minimum of
64N. . . Channel transistor
86. . . Resistor
70. . . Circuit peak maxima
74P. . . Channel transistor
78. . . Resistor
82. . . Operational amplifier
86. . . Capacitance
72. . . Operational amplifier
76. . . Capacitance
80. . . Circuit peak minimum of
84N. . . Channel transistor
88. . . Resistance

(v) Creation Description: The creation mainly as a peak capture and correction circuit, especially a digital signal meter peak in the capture and correction circuit, which takes advantage of an integrated circuit and an electrical capacity of the facilities the integrated circuit external capacitor, the integrated circuit comprises an operational amplifier and a switching circuit of the operational amplifier's inputs are connected to and fed back into the a first voltage, the output of the operational amplifier is connected to the end said switching circuit, the switching circuit outputs a second voltage, and is connected to the capacitor. Digital signal meter peak of the creation of the capture and correction circuit, the use of fewer parts, lower cost of production, is cost-effective, avoid conventional peak capture circuit using the diode is not easy to obtain, and the slower the speed, power consumption Lack. Hereinafter, with reference to the drawings a detailed description of the creation of the digital signal meter peak capture measurement circuit and calibration circuit of the preferred embodiment.

[] The first preferred embodiment of

a circuit diagram of the digital signal meter peak capture measurement and correction circuit of a first preferred embodiment of the present creation, see depicted in Figure III, the Department of VLSI circuits in order to make the peak capture circuit, only capacitors do outside the wafer. Wherein Figure III A line circuit 30 is the peak maxima, and Figure III B line is the minimum value of the peak circuit 40.

Triple-A shown in FIG. 30 circuit peak maxima using an integrated circuit, and a capacitor 36 embodiment, the integrated circuit of the external capacitor 36, the integrated circuit includes an operational amplifier 32, an N-channel power crystal 34, and a resistor 38. IN input from the non-inverting input terminal of the operational amplifier 32 into the inverting input terminal is connected to the feed-back, and the output terminal of the operational amplifier 32 is connected N-channel transistor gate electrode 34.

N-channel transistor 34, the drain electrode (Drain) high-voltage source connected to the VDD terminal, i.e. the highest potential of the circuit, a source connected to one end of resistor 38, resistor 38 connected to the other end of the capacitor 36, the capacitor 36 connected to GND, GND is circuit in a low noise dc voltage (low noise DC voltage).

Configuring resistor 38 between 36 and N-channel transistor 34 in capacitor, so that the output voltage V_{OUT} will exceed (overshooting) phenomenon. Prior to measuring the peak maxima, it must first output voltage the $V_{the\ OUT}$ is set to a potential lower than the minimum of the effective potential of the measurement range.

When the input voltage $V_{the\ IN}$ is greater than the output voltage V_{OUT} , the output of the operational amplifier 32 is "high" logic state, N channel transistor 34 turns on, the output voltage V_{OUT} will follow (follow) the input voltage $V_{the\ IN}$, the output voltage V_{OUT} It will be equal to the input voltage $V_{the\ IN}$. And, when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is low, the output of the operational amplifier 32 is "low" logic state, N channel transistor 34 is closed, the capacitor 34 the output voltage V_{OUT} voltage sustain; as long as the input voltage V [illegible] again higher than the output voltage V

the output voltage V_{OUT} will again follow the input voltage $V_{the\ IN}$.
Then the circuit shown, the peak value of the minimum three-B in Figure 40 utilizes an integrated circuit and a capacitor 46 embodiment, the integrated circuit of the external capacitor 46, the integrated circuit includes an operational amplifier 42, a P-channel transistor 44 and a resistor 48. Input terminal IN from the non-inverting input terminal of the operational amplifier 42 into the inverting input is connected to the feed-back, and the output terminal of the operational amplifier 42 is connected with the P-channel transistor 44 of the gate electrode. P-channel transistor 44 of the drain electrode (Drain) low-voltage source connected to the VSS terminal, i.e. the lowest potential of the circuit, a source connected to one end of resistor 48, resistor 48 and the other end connected to the capacitor 46, the capacitor 46 connected to GND. GND is a circuit of a low-noise DC voltage (low noise DC voltage).
Configuring resistor 48 between the capacitor 44 and P-channel transistor 46, to avoid the output voltage V_{OUT} will exceed (overshooting) phenomenon. Before entering the minimum peak measure 'must first output voltage V_{OUT} is set to be even higher than the highest potential of the effective measurement range of potential.
When the input voltage $V_{the\ IN}$ less than the output voltage V_{OUT} , the output of the operational amplifier 42 is "low" logic state, P-channel transistor 44 turns on, the output voltage V_{OUT} will follow (follow) the input voltage $V_{the\ IN}$, the output voltage V_{OUT} It will be equal to the input voltage $V_{the\ IN}$.
And 'when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is high, the output of the operational amplifier 42 is "high" logic state, P-channel transistor 44 is not turned on' output voltage V_{OUT} is maintained live; as long as the input voltage V_{IN} again lower than the output voltage V_{OUT} , the output voltage V_{OUT} will again follow the input voltage V_{IN} .
[] The second preferred embodiment
of the creation of the second preferred embodiment of the digital signal meter peak capture measurement and correction circuit schematic, and then refer to Figure IV depicted, the Department of VLSI circuits in order to make the peak capture circuit only the capacitor do outside of the wafer. Wherein Figure IV A system of circuit peak maxima 50 and Figure IV B line to a minimum value circuit 60 peak.
A four shown in FIG peak maxima circuit 50 uses an integrated circuit and a capacitor 56 embodiment, the integrated circuit of the external capacitor 56, the integrated circuit includes an operational amplifier 52, a P-channel power crystal 54, and a resistor 58. The inverting input terminal IN from the input terminal of the operational amplifier 52 into the non-inverting input terminal is connected to the feed-back, and the output terminal of the operational amplifier 52 is connected with the P-channel transistor 54 of the gate.
Source terminal P-channel transistor 54 is connected to the high voltage source VDD, that is the highest potential of the circuit, the drain (drain) connected to one end of the resistor 58, the other end of the resistor 58 is connected to the capacitor 56, the capacitor 56 connected to GND, GND is a circuit a low noise dc voltage (low noise DC voltage).
When the input voltage $V_{the\ IN}$ is greater than the output voltage V_{OUT} , the output of the operational amplifier 52 is "low" logic state, P-channel transistor 54 turns on, V_{GS} = high voltage source VDD- low voltage source VSS. Since the P-channel transistor 54 will not have body effect problems, can provide enough current to charge the capacitor 56, the output voltage V_{OUT} can be fast to keep the input voltage $V_{the\ IN}$, the output voltage V_{OUT} is equal to the input voltage $V_{the\ IN}$.
And, when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is low, the output of the operational amplifier 52 is "high" logic state, P-channel transistor 54 is closed, the capacitor 56 the output voltage V_{OUT} voltage sustain; as long as the input voltage $V_{the\ IN}$ again higher than the output voltage V_{OUT} , the output voltage V_{OUT} will again follow the input voltage $V_{the\ IN}$.
Since Figure IV A using P-channel transistors, so the output swing compared with Figure III A of outputswing large.
Then IV B, the minimum value of the peak circuit 60 as shown in the use of an integrated circuit, and a capacitor 66 embodiment, the integrated circuit of the external capacitor 66, the integrated circuit includes an operational amplifier 62, an N-channel transistor 64 and a resistor 68. The inverting input terminal IN from the input terminal of the operational amplifier 62 into the non-inverting input terminal is connected to the feed-back, and the output terminal of the operational amplifier 62 is connected to the N-channel transistor 64 gate.
The source terminal of N-channel transistor 64 is connected to a low voltage source VSS, that is, the lowest potential of the circuit, the drain (drain) connected to one end of the resistor 68, the resistor 68 and the other end connected to the capacitor 66, the capacitor 66 connected to GND, GND is a circuit a low noise dc voltage (low noise DC voltage).
When the input voltage $V_{the\ IN}$ less than the output voltage V_{OUT} , the output of the operational amplifier 62 is "high" logic state, the N-channel transistor 64 will be turned on, since the N-channel transistor 64 of the substrate (substrate) is also connected to a low voltage source VSS , so there is no body effect problems, can provide enough current to charge the capacitor 66, the output voltage V_{OUT} can be fast to keep the input voltage $V_{the\ iN}$, the output voltage V_{OUT} will be equal

And 'when the input voltage $V_{the\ IN}$ comparing the output voltage V_{OUT} is high, the output of the operational amplifier 62 is "low" logic state, N channel transistor 64 is not turned on' output voltage V_{OUT} is maintained live; as long as the input voltage V_{IN} again lower than the output voltage V_{OUT} , the output voltage V_{OUT} will again follow the input voltage V_{IN} . Since Figure IV B using N-channel transistors, so the output swing compared with Figure IV B of the large output swing.

Between the capacitor 56 and the P-channel transistor 54 is disposed resistor 58, the capacitor 66 and N-channel transistor configuration resistance between 64 and 68 prevents output voltage V_{OUT} will exceed (overshooting) phenomenon.

It is noteworthy that, in the preferred embodiment, the circuit peak maxima of 50 lines to replace the P-channel transistor N-channel transistors to avoid when the output voltage is high, because V_{GS} = high voltage source output voltage V VDD- $_{OUT}$, so that V_{GS} is small and may not provide enough current to charge the capacitor, and N-channel transistors have a substrate effect (body effect) problems resulting V_T becomes large, the impact to the operating element.

Since the substrate effect of N-channel transistors (body effect) caused by the deterioration of the circuit characteristics, so that when the supply voltage is low, N-channel transistors can not provide enough current to charge the capacitor, the output voltage V_{OUT} can not keep up with rapidly the input voltage $V_{the\ IN}$.

When the supply voltage is low, the use of N-channel transistors situation is likely to occur when the input voltage $V_{the\ IN}$ time to rise to the highest point since the N-channel transistor V_{GS} -V_T is too small to provide enough current to charge the capacitor The output voltage V_{OUT} can not keep up with the input voltage $V_{the\ IN}$, the output voltage V_{OUT} is not equal to the input voltage $V_{the\ IN}$, than the input voltage $V_{the\ IN}$ lower.

Next, the input voltage $V_{the\ IN}$ time to fall down, just lower than the output voltage V_{OUT} , the output voltage V_{OUT} will sustain will never change, but this time may occur output voltage V_{OUT} is lower than the input voltage $V_{the\ IN}$ maxima situation.

Instead, the minimum value of the peak circuit 40, although there will be no effect of the substrate (bodyeffect) problems, but when the power supply voltage is low, may also occur not provide enough current to charge the capacitor, the output voltage V_{OUT} will not be able to quickly to keep up with the input voltage $V_{the\ IN}$, the output voltage V_{OUT} is not equal to the input voltage $V_{the\ IN}$.

[Third Embodiment]

Referring again to Figure V, depicted in Figure V-based authoring system of the second embodiment, the digital signal meter peak capture circuit diagram of a calibration and correction circuit of the time. Wherein Figure V Series A peak maxima for the circuit 70, and Figure V B-based minimum peak for the circuit 80.

Since the operational amplifier typically have tens mV input offset voltage (input offset voltage), which causes an error on the measurement, so the digital signal meter peak before the peak capture circuit to capture measurements, this must be an error correction , ie before measuring to do first calibration (calibration) operation.

In a dual slope analog-to-digital converter (dual slope A / D), if 0.1mV equals one count, then there is 100counts 10mV error. The present embodiment is the use of calibration (calibration) way, this peak capture circuit offset voltage (offset voltage), error compensation includes operational amplifier input offset voltage generating back.

Since the circuit circuit 70 and the peak minimum peak maxima 80 respectively with different op amp OPH72 and OPL82, and therefore the operational amplifier OPH72 respectively OPL82 who must do the calibration (calibration), and subtracting the operational amplifier measured peak maxima OPH72 offset by subtracting the offset of the operational amplifier OPL82 when measured peak minimum.

A five circuit shown in FIG. 70 peak maxima integrated circuit using a capacitor and a 76 embodiment, the integrated circuit of the external capacitor 76, the integrated circuit includes an operational amplifier 72, a P-channel power crystal 74, and a resistor 78, capacitor 76 made in the outside of the wafer. The inverting input terminal IN from the input terminal of the operational amplifier 72 into the non-inverting input terminal is connected to the feed-back, and the output terminal of the operational amplifier 72 is connected with the P-channel transistor 74 of the gate electrode.

Source terminal P-channel transistor 74 is connected to the high voltage source VDD, that is the highest potential of the circuit, the drain (drain) connected to one end of the resistor 78, the resistor 78 and the other end connected to the capacitor 76, the capacitor 76 connected to GND, GND is a circuit a low noise dc voltage (low noise DC voltage).

Before entering the calibration mode, you must first circuit peak maximum output voltage of 70 V_{OUT} is set to lower than the offset voltage (offset vo1tage) potential. After entering the calibration mode, the input connected to GND, until stable output, the output voltage V_{OUT} is the value of the op amp input offset voltage of 72.

Again, the op amp input offset voltage 72 via a dual slope analog-to-digital converter (dual slope A / D) converted into a digital signal after temporarily stored in digital electronics, after each peak capture measurement results reset

Five more B circuit shown in Figure 80 peak minimum use of an integrated circuit, and a capacitor 86 embodiment, the integrated circuit of the external capacitor 86, the integrated circuit includes an operational amplifier 82, a P-channel transistor 84 and a resistor 88. The inverting input terminal IN from the input terminal of the operational amplifier 82 into the non-inverting input terminal is connected to the feed-back, and the output terminal of the operational amplifier 82 is connected to the N-channel transistor 84 gate.

The source terminal of N-channel transistor 84 is connected to a low voltage source VSS, that is, the lowest potential of the circuit, the drain (drain) connected to one end of the resistor 88, the resistor 88 and the other end connected to the capacitor 86, the capacitor 86 connected to GND, GND is a circuit a low noise dc voltage (low noise DC voltage).

Before entering the calibration mode, you must first circuit minimum peak output voltage of 80 V_{OUT} is set to higher than the offset voltage (offset voltage) potential. After entering the calibration mode, the input connected to GND, until stable output, the output voltage V_{OUT} is the value of the op amp input offset voltage of 82.

Again, the op amp input offset voltage 82 via a dual slope analog-to-digital converter (dual slope A / D) converted into a digital signal after temporarily stored in digital electronics, after each peak capture measurement results reuse digital electronics offset value is subtracted.

See Figure VI again depicted, which illustrates a timing diagram calibration. When entering calibration (calibration) measurements, circuits, circuit peak maxima of five A-70, the minimum value of the peak is shown in figure V 80 B, dual slope analog-to-digital converter (dual slope A / D) again interactively calculated peak maxima and minima n peak times, soon after the end of the n-th calibration automatically leave the calibration measurements.

The number of measurements at the time of the end of the circuit may be required to stabilize, the last calculation result is converted into digital signals are stored in digital electronics have the scratchpad. When measured at the peak maxima, the use of digital electronics store register minus the offset value of the operational amplifier 72. When measuring peak minimum, the use of digital electronics subtract another register stored offset value of the operational amplifier 82.

The creative use of VLSI circuits can be easily calibrated to do, to avoid the conventional peak capture circuit, since the combination of discrete components, the use of more parts, so the error correction prior to capture peak measurement, cost and have a high degree of difficulty of the missing.

In the present used in the creation of an operational amplifier, must provide sufficient drive current output capacity better, the output voltage V_{OUT} to rapidly keep up with the input voltage $V_{the\ IN}$. In addition, the speed gain (gain) large, the output voltage V_{OUT} and the input voltage $V_{the\ IN}$ error will be small.

The creation of a digital signal meter peak capture measurement circuit, a simple VLSI circuit design, suitable for use in digital meter to reduce the cost of production, the more cost-effective, and fast, big gain, small power consumption , more power.

He said digital signal meter peak capture circuit measurements clearly showing the progress of the purpose and effect of the Creation are deep rich embodiment, the use of great industrial value of the 'new creation for the current and unprecedented surface of the towel completely in line with the creation of patent requirements, Yuan law to apply.

Only those described above, only the preferred embodiments of the Creation only, when it is not to limit the creation of the implementation of the range. That is almost all under these modifications and alterations made by the scope of patent creation, all should still fall within the scope of the patent covers the creation, the committee would like to ask you to review Yao Mingjian, and pray prospective benefits, it is Suozhi prayer.

Nine, the patent application scope:

A peak value capture and correction circuit system is a digital meter peak signal acquisition and calibration of the circuit, which takes advantage of an integrated circuit and a circuit external capacitor embodiment of the capacitor of the product, the integrated circuits includes an operational amplifier and a switch circuit, the operational amplifier's inputs are connected to and fed back into the a first voltage, the operational amplifier is connected to the output terminal of the switching circuit, the switching circuit outputs a second voltage, and is connected to the capacitor.

2. The scope of the patent application peak of paragraph 1 capture and correction circuit, wherein the switching circuit comprises a transistor, can provide enough current to charge the capacitor.

3. The scope of the patent application peak of paragraph 2 capture and correction circuitry further comprises a resistor, the resistance of the transistor connected to the second voltage will avoid exceeding the phenomenon.

4. The capture range of the patent as the peak of the correction circuit and Item 3, wherein the electrical system as a crystalline N-channel transistor, the operational amplifier non-inverting input voltage into the first, the said operational amplifier and fed back to the inverting input terminal is connected, and the operational amplifier output terminal connected to the gate electrode of the N-channel transistors

the item 4, wherein said drain terminal of N-channel transistors connected to the highest potential of the circuit, a source connected to one end of said resistor, the other end of the resistor connected to the capacitor, the capacitor to the circuit in a low-noise DC voltage.

6. The scope of the patent application peak in item 5 capture and correction circuit, wherein, before entering the measure, the second voltage is set to be lower than the minimum potential of the effective measurement range of potential.

7. The scope of the patent application for the peak of the item capture and correction circuit 6, wherein said first voltage is greater than the second voltage, the output of the operational amplifier is "high" logic state, the N-channel transistor turns on, the second voltage follower (follow) the first voltage.

8. The scope of the patent application peak in item 7 capture and correction circuit, wherein when the first voltage and the second voltage is relatively low, the output of the operational amplifier is "low" logic state, the N-channel transistor is turned off, the capacitor voltage of the second sustain.

9. The application range of the peak of the patent item capture and correction circuit 8, wherein when said first voltage is then higher than the second voltage, the second voltage will then follow the first voltage .

10. The scope of the patent application peak of paragraph 3 capture and correction circuit, wherein the electrical system as a crystalline P-channel transistor, the operational amplifier non-inverting input voltage into the first, the inverting input terminal of the operational amplifier and fed back to the connection, and the operational amplifier output terminal connected to the P-channel transistor gate.

11. The scope of the patent application for the peak of the item capture and correction circuit 10, wherein said P-channel transistor drain terminal connected to the lowest potential of the circuit, a source connected to one end of the resistance, the resistance of the other connect one end of the capacitance of the capacitor to the circuit in a low-noise DC voltage.

12. The scope of the patent application for the peak of the item capture and correction circuit 11, which, before entering the measure, the second voltage is set to be higher than the highest potential effective measurement range of potential.

13. The scope of the patent application for the peak of the item capture and correction circuit 12, wherein said first voltage is less than the second voltage, the output of the operational amplifier is "low" logic state, the P-channel transistor turns on, the second voltage follower (follow) the first voltage.

14. The scope of patent No. 13, the peak of the capture and correction circuit, wherein when said first voltage representing the second voltage is high, the output of the operational amplifier is "high" logic state, the P-channel transistor is turned off, the second voltage sustain.

15. The peak of the patent application scope of article 14, item capture and correction circuit, wherein when said first voltage is again lower than the second voltage, the second voltage will then follow the first voltage .

16. The peak of the patent application scope of paragraph 3 capture and correction circuit, wherein the electrical system as a crystalline P-channel transistor, the operational amplifier inverting input terminal into said first voltage, the said operational amplifier non-inverting input terminal is connected with the feed-back, and the operational amplifier output terminal connected to the P-channel transistor gate.

17. The range of the peak of the patent item capture and correction circuit 16, wherein the source terminal of the P-channel transistor is connected to the highest potential of the circuit, the drain connected to one terminal of resistor, the resistance of the other connect one end of the capacitance of the capacitor to the circuit in a low-noise DC voltage.

18. The scope of patent applications in item 17 of the peak value capture and correction circuit, wherein when said first voltage is greater than the second voltage, the output of the operational amplifier is "low" logic state, the P-channel transistor turns on, the second voltage quickly to keep up with the first voltage.

19. The scope of the patent application for the peak of the item capture and correction circuit 18, which, when compared with the first voltage and the second voltage is low, the output of the operational amplifier is "high" logic state, the P-channel transistor is turned off, the capacitor voltage of the second sustain voltage.

20. The scope of the patent application for the peak of the item capture and correction circuit 19, wherein when said first voltage is then higher than the second voltage, the second voltage will then follow the first voltage .

21. The scope of the patent application peak of paragraph 3 capture and correction circuit, wherein the electrical system for the crystal N-channel transistors, the operational amplifier inverting input terminal into said first voltage, the the non-inverting input terminal of the operational amplifier is fed back and connected, and the operational amplifier output terminal connected to the gate electrode of the N-channel transistors.

22. The scope of the patent application for the peak of the item capture and correction circuit 21, wherein the source terminal of the N-channel transistor is connected to the lowest potential of the circuit, the drain connected to one end of the resistance, the resistance of the other connect one end of the capacitance of the capacitor to the circuit in a low-noise DC voltage.

23. The patent scope of Article 22 of the peak value capture and correction circuit, wherein the substrate of the N-channel transistor (substrate) circuit

24. The scope of the patent application for the peak of the item capture and correction circuit 23, wherein said first voltage is less than the second voltage, the output of the operational amplifier is "high" logic state, the N-channel transistor turns on, the second voltage will quickly follow (follow) the first voltage.

25. The patent scope of Article 24 of the peak value capture and correction circuit, wherein when said first voltage representing the second voltage is high, the output of the operational amplifier is "low" logic state, the N-channel transistor is turned off, the second voltage sustain.

26. The scope of the patent application for the peak of the first 25 capture and correction circuit, wherein when said first voltage is again lower than the second voltage, the second voltage will then follow the first voltage .

27. A digital meter calibration signal peak capture circuit that takes advantage of an integrated circuit and a capacitor embodiment, the external circuit of the capacitor product, the integrated circuit comprises an operational amplifier, a transistor and a resistor , the operational amplifier circuit connected to the inverting input of a low noise dc voltage, the non-inverting input terminal is connected with the feed-back, and the operational amplifier output terminal connected to the gate of the transistor, the said transistors to provide enough current to charge the capacitor, the resistor is connected between the transistor and the capacitor, to avoid a second output voltage of the phenomenon will be over.

28. The patent context of Article 27 of the digital signal meter peak capture calibration circuit, wherein the electrical system for the crystal P-channel transistor, a source terminal of the P-channel transistor is connected to the highest potential of the circuit , drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitor to the circuit in a low-noise DC voltage.

29. The scope of the patent in item 28 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is greater than the second voltage, the output of the operational amplifier is "low" logic state, the P-channel transistor turns on, the second voltage quickly to keep up with the first voltage.

30. The scope of the patent in item 29 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is lower than the second voltage, the operational amplifier output is "high" logic state, the P-channel transistor is turned off, the capacitor voltage of the second sustain voltage.

31. The scope of the patent in item 30 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is then higher than the second voltage, the second voltage follower will be the first a voltage.

32. The scope of the patent Article 27 of the digital signal meter peak capture calibration circuit, wherein the electrical system for the crystal N-channel transistors, the source terminal of the N-channel transistor is connected to the lowest potential of the circuit , drain connected to one end of the resistor, the other end of the resistor connected to the capacitor, the capacitor to the circuit in a low-noise DC voltage.

33. The scope of the patent in item 32 of the digital signal meter peak capture calibration circuit, wherein the substrate of the N-channel transistor (substrate) circuit connected to the lowest potential.

34. The scope of the patent in item 33 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is less than the second voltage, the output of the operational amplifier is "high" logic state, the N-channel transistor turns on, the second voltage can quickly follow (follow) the first voltage.

35. The scope of the patent in item 34 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is higher than the second voltage, the operational amplifier output is "low" logic state, the N-channel transistor is turned off, the second voltage sustain.

36. The scope of the patent Article 35 of the digital signal meter peak capture calibration circuit, wherein when said first voltage is again lower than the second voltage, the second voltage follower will be the first a voltage.

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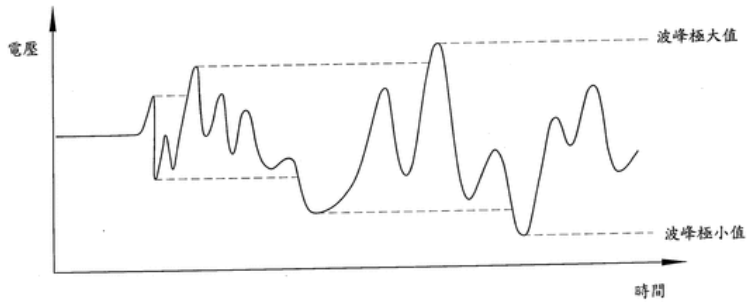

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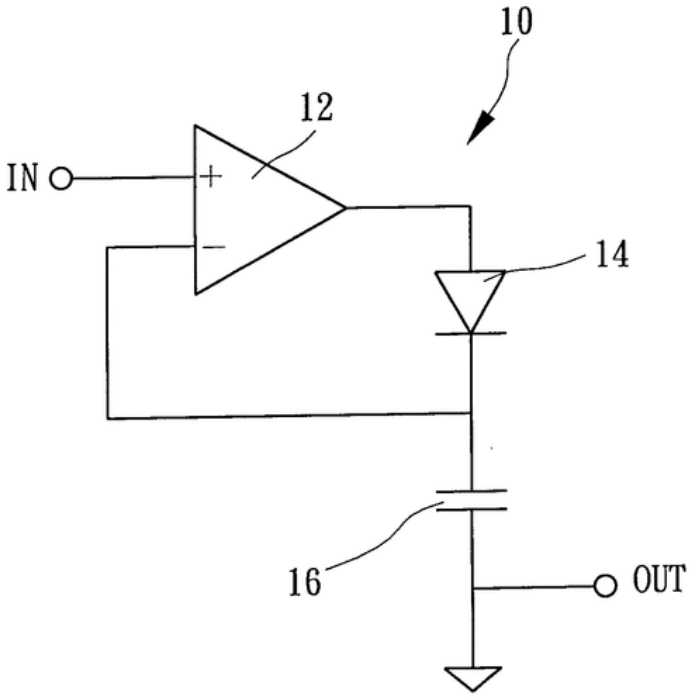

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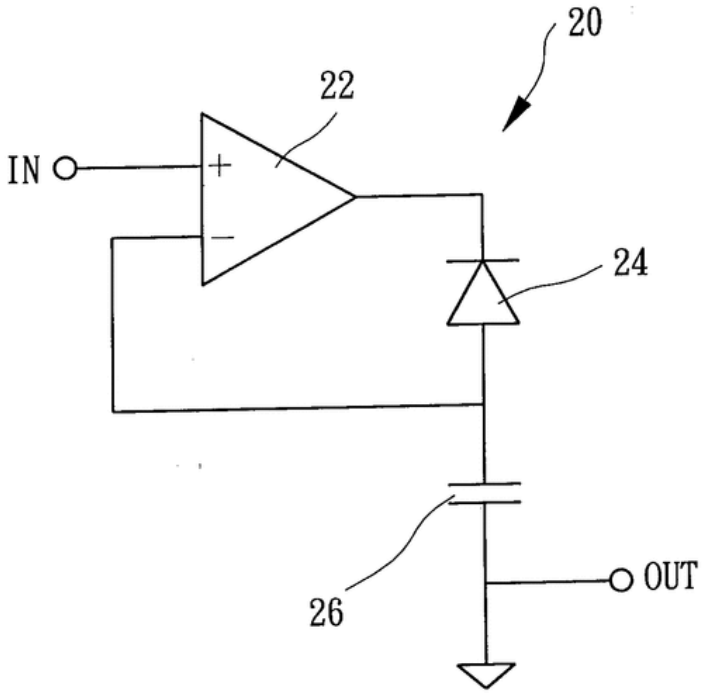

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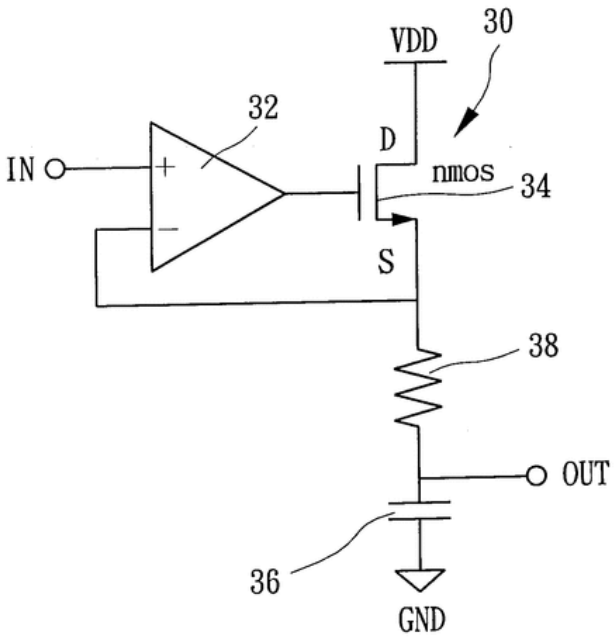

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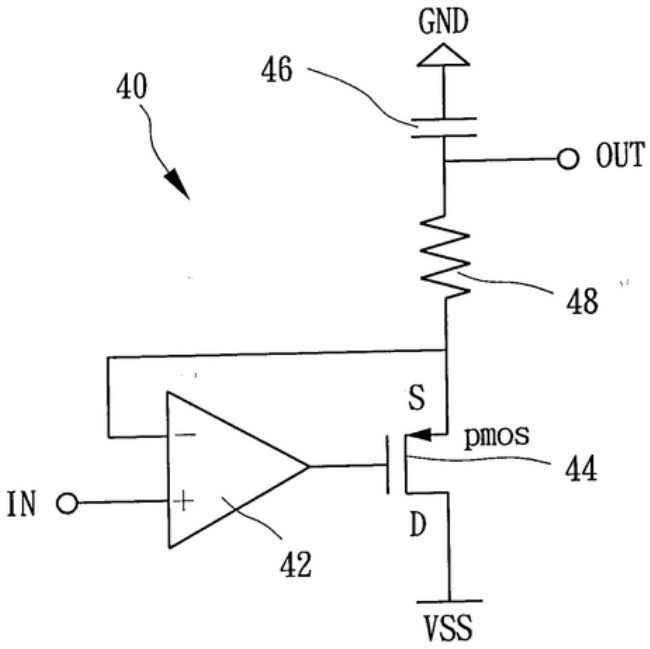

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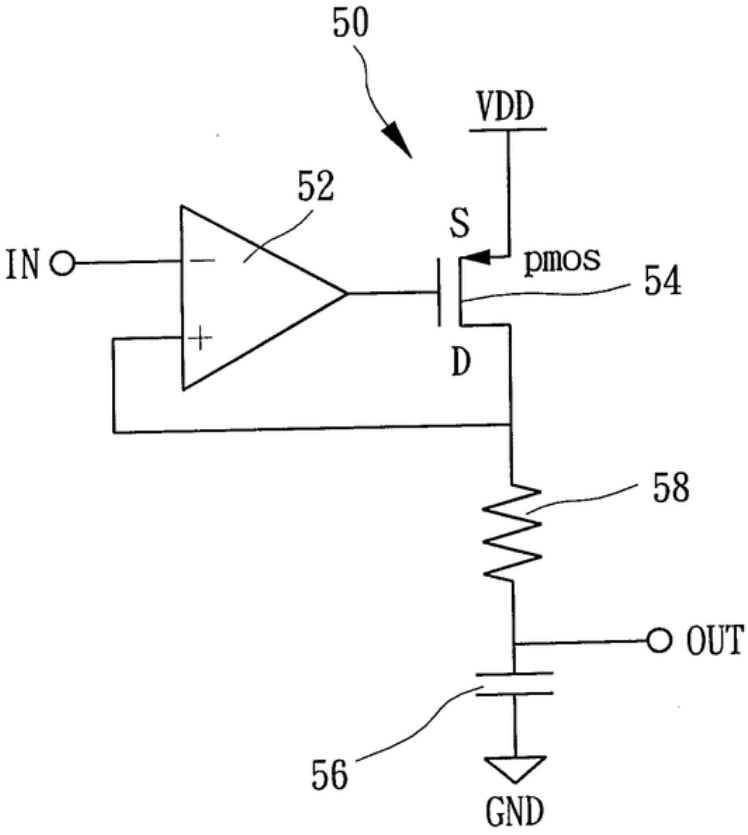

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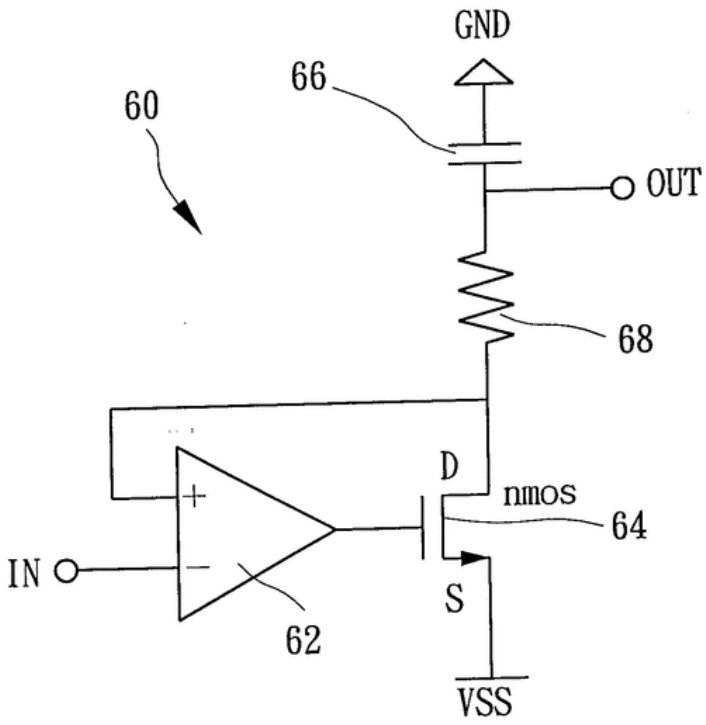

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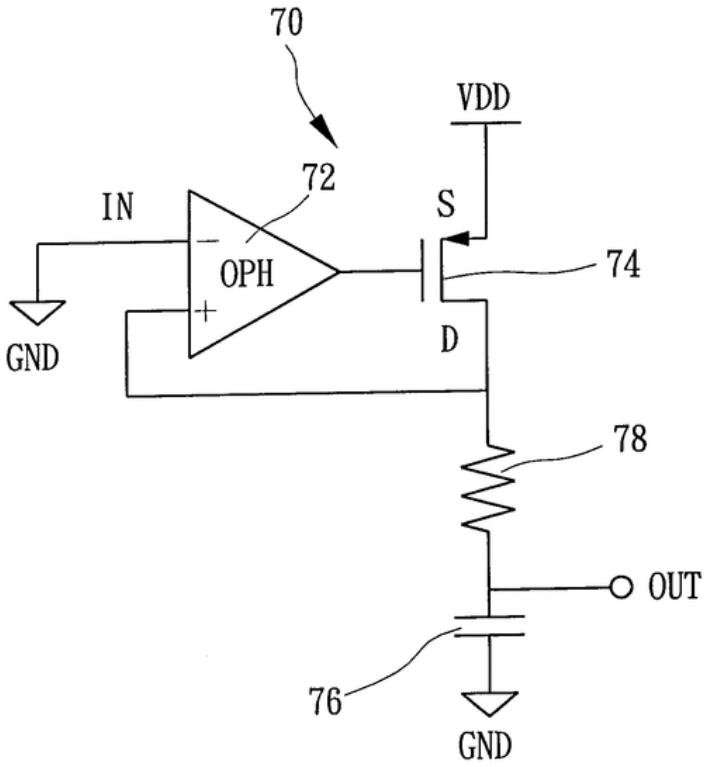

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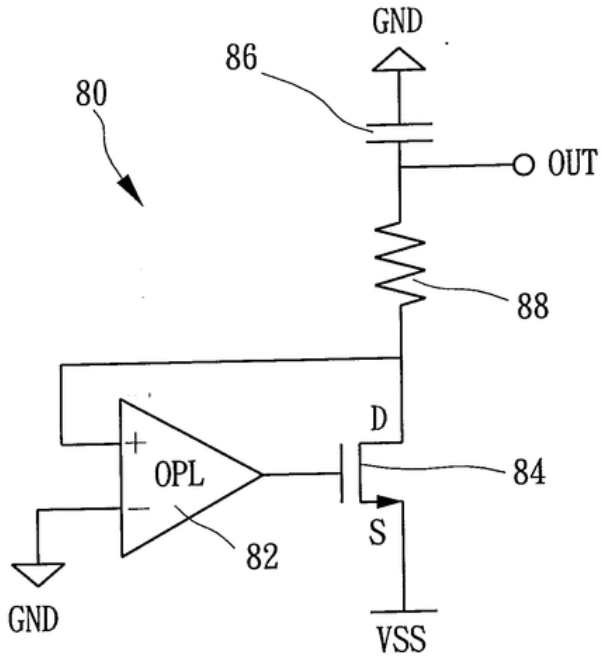
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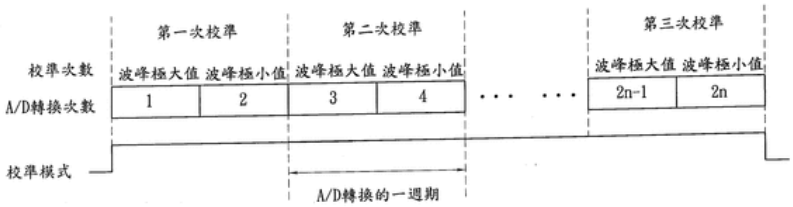
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圖 六