Endura AB915GM Product Manual

RadiSys
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Preface

Notational Conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.

Notes indicate important information about the product.

Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.

The globe indicates a World Wide Web address.

The book indicates a book or file.

ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).

Cautions indicate potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.

Warnings indicate potentially hazardous situations, which, if not avoided, can result in death or serious injury.

Danger indicates imminently hazardous situations, which, if not avoided, will result in death or serious injury.

Installation Notes

When installing this motherboard into a suitable chassis, refer to the following notes:

- Read and save all instructions.
- Always disconnect Cord/Plug before installation or upgrade. Parts of the motherboard can remain powered even when the power supply is switched off unless the cord is disconnected.
- Pay attention to the safety warnings included in this document.
- When installing expansion cards, pay attention to the maximum loads detailed in this document. Use only UL approved peripheral cards.
- Route wiring away from sharp edges, heat sources and cooling fans.
- Pay attention to the thermal issues described in this document. The motherboard requires suitable airflow to maintain an ambient temperature within its operating range.

Where to get more product information

You can find out more about Endura products from these sources:

- World Wide Web: RadiSys maintains an active Web site at www.radisys.com. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, software updates, manuals, and technical support information.
- RadiSys sales representative: If you purchased your product from RadiSys, contact your sales representative via email or phone.
- Other: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

Safety and Approval Notices

Table 1. Safety and approval notices

Item	Description
Battery	This product contains a lithium cell. • When removing or replacing the lithium cell, do not use a conductive instrument as a short-circuit may cause the cell to explode. Always replace the cell with one of the same type. This product uses a CR2032 cell. Dispose of a spent cell promptly – do not recharge, disassemble or incinerate. Keep cells away from children. • **CAUTION!** Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of batteries according to the manufacturer's instructions.
LAN (Local Area Network) Connector	This product may include an RJ45 LAN connector (see product options). Do not connect to anything other than an Ethernet LAN.
Thermal Interface Material	This product may contain thermal interface material between devices and heatsinks. This can cause irritation and can stain clothing. Avoid prolonged or repeated contact with the skin and wash thoroughly with soap and water after handling. Avoid contact with eyes and inhalation of fumes. Do not ingest.
Anti-static Precautions	This product contains static-sensitive components and should be handled with care. It is recommended that the product be handled in a Special Handling Area (SHA) as defined in EN100015-1:1992. Such an area has working surfaces, floor coverings and chairs connected to a common earth reference point. An earthed wrist strap should be worn whilst handling. Other examples of static-sensitive devices are the memory modules and the processor. Failure to employ adequate anti-static measures can cause irreparable damage to components on the motherboard.
Electromagnetic Compatibility	This product is designed to meet the following EMC standards when installed in a suitable chassis. • FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B) • EN55022:1998 Class B • EN55024:1998
Safety	This product complies with the American Safety Standard UL60950 when installed in a suitable chassis.
Legal Directives	This product complies with the relevant clauses of the following European Directives. Low Voltage Directive 73/23/EEC EMC Directive 89/336/EEC

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1. Overview

The AB915GM is a MicroATX form factor motherboard designed around an Intel® Celeron® or Pentium® M processor and an Intel 915GM family chipset. It integrates video, audio, system monitoring and an Ethernet controller on a 9.0 x 7.5 inch board.

Table 2. Features

Item	Description
Form Factor	MicroATX and FlexATX, 9.0 x 7.5-inches, 4 expansion slots
Processor	Intel Mobile Celeron M and Pentium M processor support 479-pin PGA socket for µFC-PGA processor package 479-ball BGA processor package support – contact RadiSys 400/533MHz processor bus speed
Chipset	Intel 915GM GMCH and Intel ICH6-M I/O hub
Memory	Two 200-pin SO-DIMM sockets for DDR2-400/533 (PC2-3200/4200) modules, each on independent memory channels Maximum 2GB (Gbit technology), minimum 128MB No support for ECC or parity Optional on-board Multimedia/Secure Digital (MM/SD) card slot
Video	Intel Graphics Media Accelerator 900 video controller integrated within chipset Dual independent displays On-board 18-bit dual channel LVDS flat panel interface Two on-board DVI interfaces, one DVI interface supports the analog VGA port Maximum VGA resolution 1600x1200 at 75Hz.
Audio	Optional Multi-stream digital audio controller integrated within chipset and Intel High Definition Audio compatible CODEC MIC, Line-out and Line-in (optional) jacks on I/O panel CD input, AUX input and Line output ATAPI internal connectors On-board PC speaker (beep)
Expansion	Two PCI Express x1 slots Two PCI 2.3 32-bit 33MHz bus-master slots One PCI Express Mini Card slot option
Power Management	ACPI 2.0 supporting states S0, S4, S5, and C0, C1, C2, C3
System Management	Voltage, temperature and fan monitoring (3 fans) Lithium cell voltage monitoring Automatic fan speed control (3 fans) Programmable watchdog timer SMBus header
BIOS	Based on Phoenix FirstBIOS™ Notebook Pro Customizable system configuration and startup logo 8Mb device includes video BIOS and network boot

Table 2. Features

Item	Description
	Optionally socketed ROM with write-protect feature
I/O	Eight USB 2.0 ports - four on I/O panel and four on locking headers, two shared with PCI Express Mini Card and MM/SD Card controller IEEE 1394b controller with single port on I/O panel General purpose I/O lines (13) with LCD character display support
Network	Intel-based 10/100Mbps or Gbit Ethernet port
Disks	Two SATA ports with locking headers Single Ultra ATA/100 interface supporting hard disks and ATAPI drives Optional on-board MM/SD card slot

1.1 Motherboard Layout

The following figure shows the layout of the AB915GM motherboard with the major components identified.

Figure 1. Motherboard layout

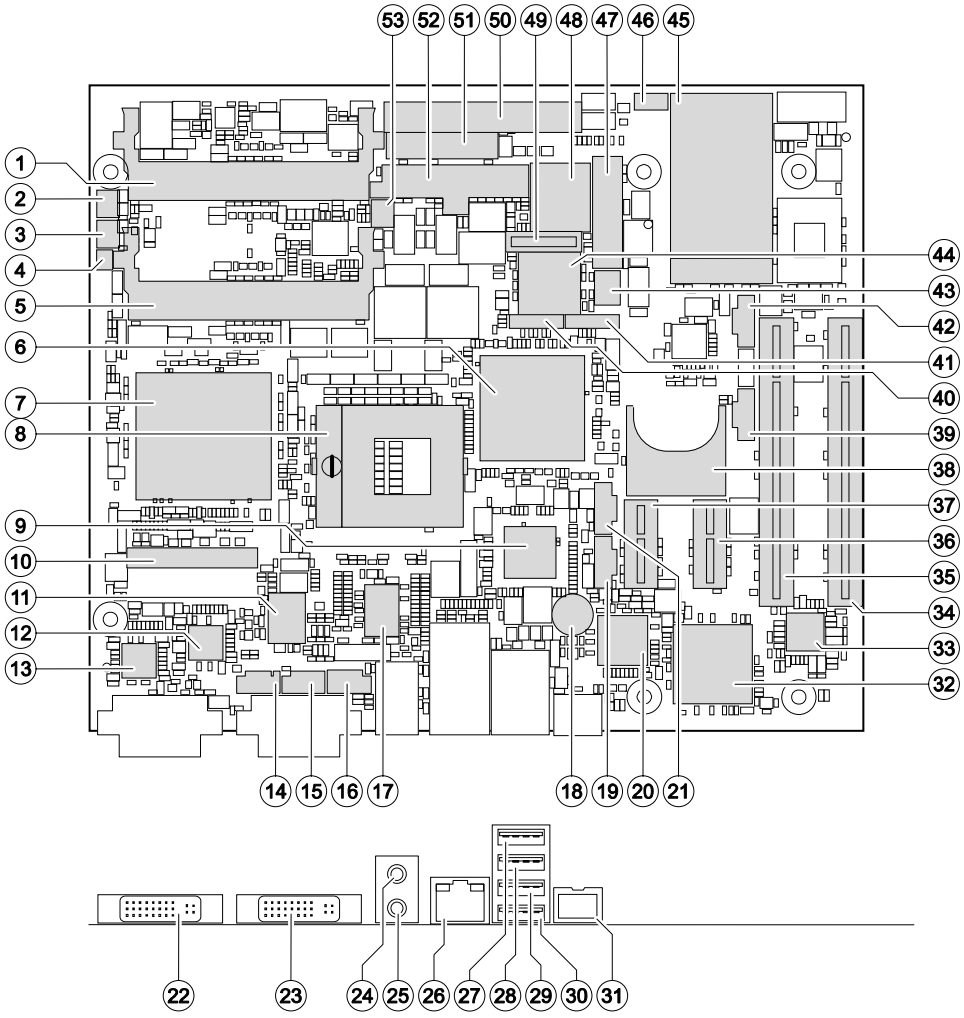


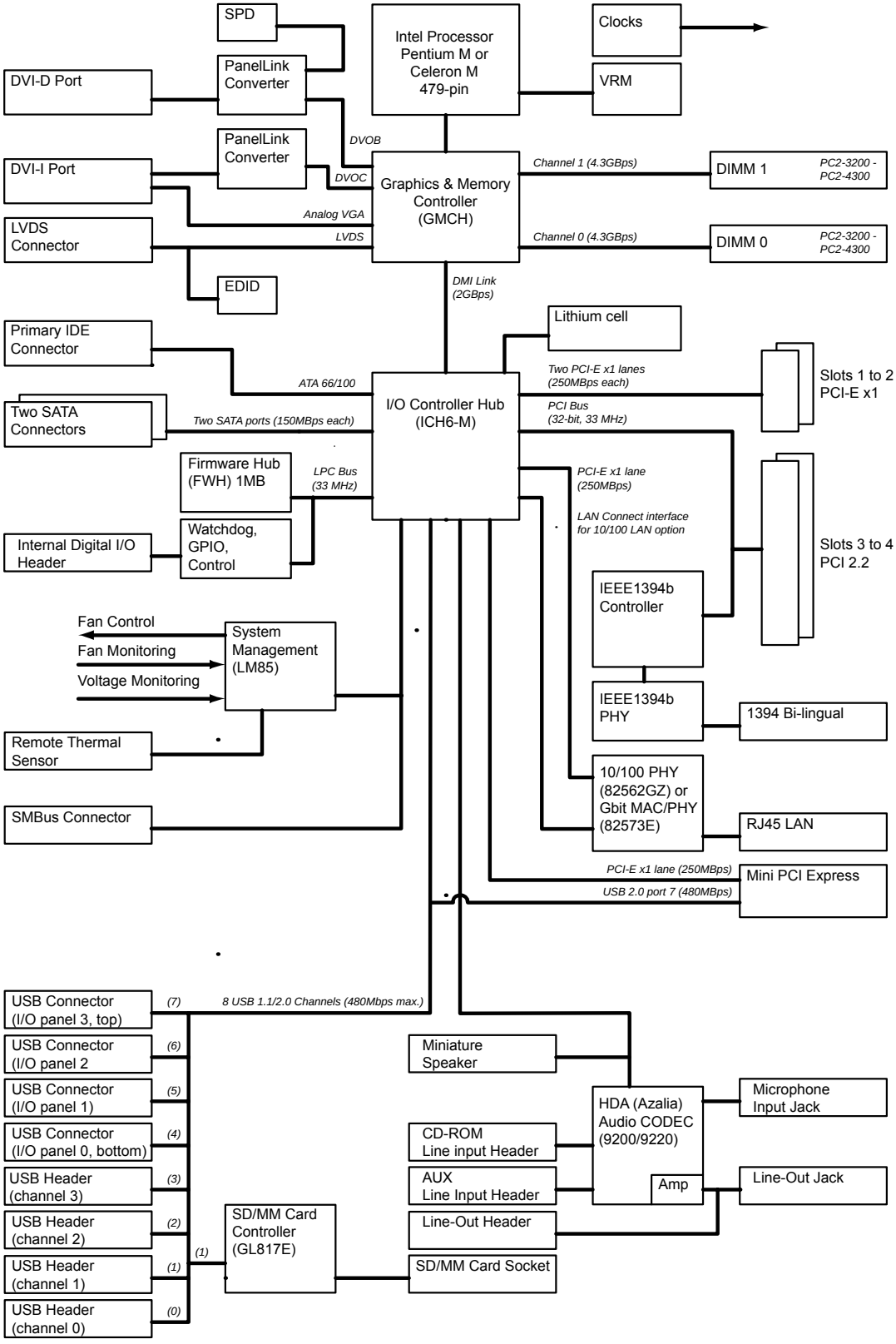
Table 3. Component Identification

	Description		Description		Description
1	Memory socket 2	**19**	USB 2.0 channel 3	**37**	Slot 1 - PCI Express x1
2	System fan 2 power connector	**20**	IEEE1394b PHY	**38**	MM/SD card socket
3	System fan 1 power connector	**21**	USB 2.0 channel 2	**39**	USB 2.0 channel 1 (products without MM/SD)
4	Remote thermal sensor	**22**	DVI-I DVI and analog VGA interface	**40**	SATA port 2
5	Memory socket 1	**23**	DVI-D DVI interface	**41**	SATA port 0
6	I/O controller hub (ICH6M)	**24**	Audio Line output jack	**42**	USB 2.0 channel 0 (shared with Mini Card)
7	Graphics and memory controller (915GM)	**25**	Audio Microphone input jack	**43**	Operating mode and write protect jumpers
8	479-pin socket for processor	**26**	Ethernet port (RJ45)	**44**	Control logic (CPLD)
9	Ethernet controller	**27**	USB 2.0 channel 7	**45**	PCI Express Mini Card slot
10	LVDS data connector	**28**	USB 2.0 channel 6	**46**	SMBus header
11	LVDS backlight control connector	**29**	USB 2.0 channel 5	**47**	Front panel connector
12	DVI controller for DVI-D interface	**30**	USB 2.0 channel 4	**48**	BIOS ROM (FWH)
13	DVI controller for DVI-I interface	**31**	IEEE1394b bi-lingual	**49**	3V Lithium cell – use CR2032
14	Audio CD-ROM Line input header	**32**	IEEE1394b controller	**50**	IDE header
15	Audio AUX Line input header	**33**	High Definition Audio controller	**51**	GPIO header
16	Audio Line output header	**34**	Slot 4 - PCI 2.2	**52**	Power supply connector
17	Clock generator	**35**	Slot 3 - PCI 2.2	**53**	Processor fan power connector
18	Miniature speaker	**36**	Slot 2 - PCI Express x1	**54**	N/A

1.2 Block Diagram

The following figure shows a block diagram of the AB915GM motherboard.

Figure 2. Block diagram



1.3 Build-Time (Soldered-Down) Options

The following hard SKU options are proposed and are subject to change.

Function	Endura AB915GM-W	Endura AB915GM-GD	Endura AB915GM-F
Chipset	Intel 915GM Intel ICH6-M	Intel 915GM Intel ICH6-M	Intel 915GM Intel ICH6-M
Processor	µFC-PGA	µFC-PGA	µFC-PGA
LAN	10/100	10/100/Gbit	10/100/Gbit
LAN remote boot	Yes	Yes	Yes
LAN wake-up	Yes	Yes	Yes
Audio[1]	HDA2, 2 jacks, 3 headers	HDA2, 2 jacks, 4 headers	HDA2, 2 jacks, 3 headers
Watchdog	Yes	Yes	Yes
LVDS	18-bit dual channel, 30-pin	18-bit dual channel, 30-pin	18-bit dual channel, 30-pin
Analog VGA[2]	Via DVI-I	Via DVI-I	Via DVI-I
DVI	Single DVI	Dual DVI	Single DVI
PCI Express Mini Card slot	Yes	Yes	Yes
MM/SD card slot	Yes	No	Yes
IEEE 1394b	No	No	Yes
High temperature operation	Yes	Yes	Yes
Enhanced programmable controller	No	No	No

1.4 Product Options

The following standard product options are proposed and are subject to change.

Table 4. Product Variants and Ordering Codes

Ordering Codes		Description
RadiSys	Customer	
ABW00-0-0	Standard Product	AB915GM-W, no CPU, no memory
ABGD00-0-0	Standard Product	AB915GM-GD, no CPU, no memory
ABF00-0-0	Standard Product	AB915GM-F, no CPU, no memory

[1] HDA*n* is *n*-channel high-definition audio CODEC

[2] Analog VGA is available via the DVI-I connector using a DVI-to-VGA adapter

1.5 Configuration

The majority of the configuration of the motherboard is done through the Setup utility built into the BIOS – discussed later in this document. One jumper block, J1, supports the operating mode jumper and the write-protect logic jumper.

1.5.1 Operation Mode Selection

This jumper selects one of these operating modes for the motherboard:

Normal Mode (Factory default) this is the position the jumper should be in for normal operation of the motherboard.

Recovery Mode If the jumper is in the recovery mode position then recovery mode is entered. The motherboard does not boot and waits until a valid recovery diskette is detected and then copies a new BIOS into the ROM. The motherboard must be powered down and then re-powered with the jumper in the normal position before normal operation can resume.

Configure Mode With the jumper in this position the motherboard automatically runs the BIOS Setup utility regardless of the state of the Setup disable flag that can be set in the BIOS defaults. In this mode, the CMOS RAM contents are ignored and the manufacturer (**F9**) defaults are used to configure the motherboard.

1.5.2 Write-Protection Control

RadiSys does offer write-protect options for the BIOS ROM and the MM/SD card. Contact www.RadiSys.com for details.

1.5.3 Front Panel Connections

The primary controls and indicators for the motherboard are connected to the front panel connector using either a single ribbon cable to a “front panel” assembly, or using a number of small PC-standard connectors. The functions are described below. See page 62 for the connector pin-out information.

Power LED

Connects either a single-color LED (usually green) or a two-terminal bi-color LED (usually green/yellow) to indicate the powered status of the motherboard. In both cases, the “green” anode should be attached to pin 2 of the front panel connector. See the Indicators section on page 26 for further information. This function is also provided on pins 15 (green anode) and 19 for products that use a 3-pin power LED cable.

Power Switch

If the motherboard is used with a soft-switch power supply, a momentary switch should be connected between pins 6 and 8 of the power connector. If the switch is closed for greater than approximately 4 seconds, the motherboard powers off immediately, regardless of the state of the operating system, losing any system context information. This input is redundant when using a hard-switch power supply.

Reset Switch

If used, a momentary switch connected between pins 5 and 7 causes the motherboard to restart when closed.

Hard Disk LED

To indicate disk activity on any of the SATA or PATA channels, a single color LED should be connected between pins 1 (anode) and 3.

Speaker

Connect an external speaker between pins 10 and 11 or 10 and 16. This is used only for the PC "beep" functions. The speaker should typically be 8Ω.

Tamper Switch

To make use of the tamper detection logic of the motherboard, connect a momentary switch between pins 18 and 20. The switch should be open when the chassis is closed.

2. Motherboard Description

2.1 Processor

The AB915GM motherboard supports Intel Celeron M, Pentium M processors in a 479-pin tool-activated ZIF PGA socket for µFC-PGA processor package. The following table lists the currently supported processors. Visit the RadiSys web site at www.radisys.com to verify support for newer processors.

An on-board voltage regulator generates the voltage for the CPU. Both the processor voltage and the operating frequency are automatically adjusted by the motherboard to suit the installed processor.

Table 5. Supported Processors

Processor Type	Processor Speed	CPU bus speed	Cache size	Package
Pentium M, 760	2.0GHz	533 MHz	2MB	µFC-PGA
Pentium M, 745	1.8GHz	400 MHz	2MB	µFC-PGA
Celeron M, 370	1.5GHz	400 MHz	1MB	µFC-PGA

2.2 System Memory

The AB915GM motherboard has two DIMM sockets to accept 64-bit, non-ECC, non-parity DDR2 SO-DIMM memory modules ranging from 128MB to 2GB. The sockets may be populated in either order and each can accept either single or double-sided modules.

The BIOS automatically configures the motherboard for the correct size, speed and type. See the Manuals, Drivers and BIOS section on the RadiSys website for a list of memory modules that were tested with this product. In general, compatible memory modules must:

- Comply with the JEDEC DDR2 specification for 1.8V 200-pin unbuffered DDR2 SDRAM PC2-3200/PC2-4200 DDR2 (DDR2-400/533) unbuffered SO-DIMM modules
- Support bus speed of either PC2-3200 (400MHz) or PC2-4200 (533Mhz)
- Include a valid serial presence detect (SPD) ROM
- Support 256Mbit, 512Mbit and 1Gbit memory technology in x8 and x16 organization

Note

When using the on-board video controller, the frame buffer is held within system memory and less memory is available to the operating system.

2.3 Chipset

The motherboard is based around an Intel 915GM chipset comprising the following parts:

- **Graphics and memory controller hub (GMCH)**. Includes the processor interface, a high-performance graphics controller and the system memory controller. The graphics controller supports dual digital display support (SDVO, used for the dual DVI channels in this product), single analog VGA, and LVDS video interfaces.

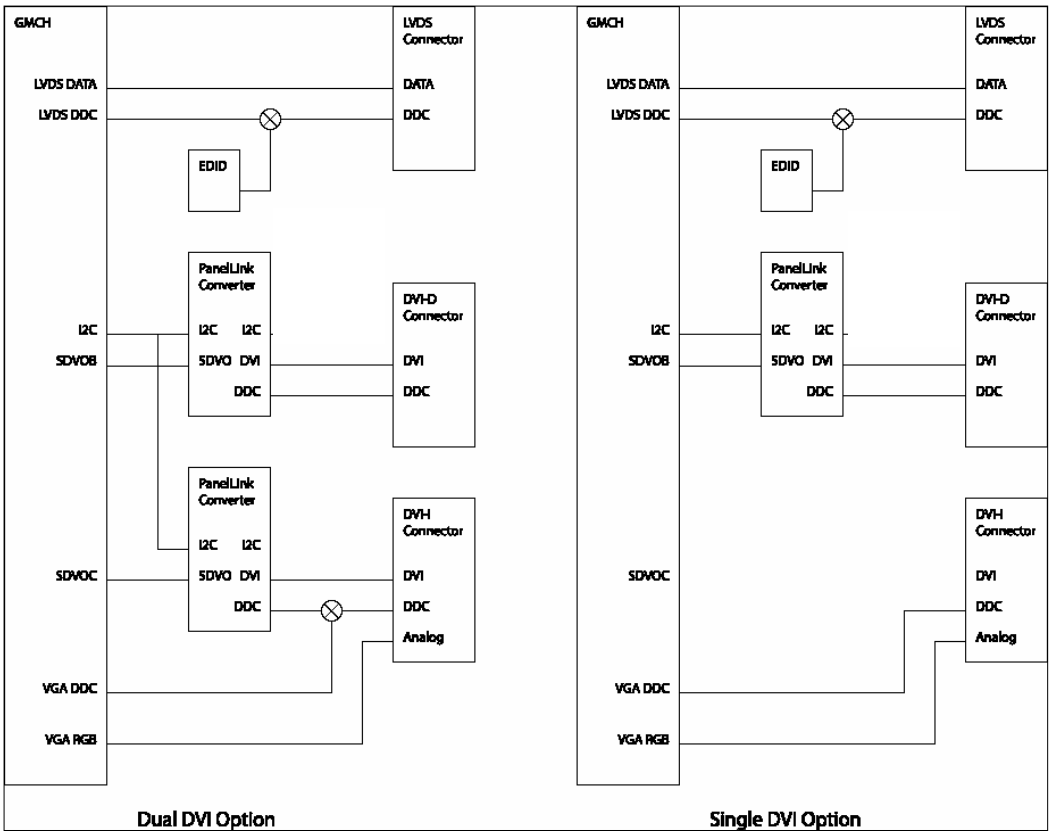
- **I/O controller hub (ICH6M)**. Provides all the PCAT-compatible devices. This includes the PCI bus, PCI-Express bus interfaces, USB 1.1 and 2.0 controllers, an SMBus controller, an UltraATA/100 disk controller, dual SATA disk controllers, High Definition Audio, and power management functions.

In addition, a firmware hub flash ROM contains the system BIOS, Setup utility, video BIOS, and optional remote boot code.

2.4 Video

- Integrated Intel Graphics Media Accelerator 900 video controller
  - 320MHz maximum display and render core frequency (GMCH operates at 1.5V)
  - Uses main memory as frame buffer storage (DVMT 3.0)
  - Intel IPD group Embedded Graphics or GMA (Extreme) drivers and video BIOS
    - IPD drivers (Shingle Springs) are not available with first production but are required to support the dual DVI interfaces
  - Dual independent display pipes allocated to the various display interfaces under software control
- Analog RGB output with DDC2B, via DVI-I connector and DVI-to-VGA adapter
  - Maximum resolution is 1600 x 1200 pixels with 32-bit color support at 75Hz
- On-board LVDS panel CPIS 1.6-compliant interface can be assigned to display pipe B only
  - 1600 x 1200 UXGA or 1920 x x1200 WUXGA maximum resolution (224M pixels/s)
  - Dual channel 18-bit interface (can be operated in single channel mode) – the chipset does not support 24-bit operation
  - 30-pin shielded connector for VDL/VCL
  - 7-pin backlight control connector (DBL)
  - Optional spread-spectrum clock generator for EMC reduction
  - Optional on-board EDID ROM
- Optional Dual DVI connectors (see Flat Panel Architecture on page 19)
  - 1600 x 1200 UXGA maximum resolution at 60Hz (200M pixels/s)
  - Digital interfaces from SDVO ports B and C via PanelLink converters and can be allocated to display pipes A and B under software control
  - Inner connector provides DVI-D digital-only port connected to SDVOB interface
    - Uses DVI-I physical connector to ensure cable compatibility
  - Outer connector provides DVI-I digital port connected to SDVOC interface (dual DVI builds only) & analog port (connector fitted even on single DVI builds)
- No support for PCI-E graphics cards or ADD2 cards

Figure 3. Flat Panel Architecture



2.4.1 System Memory Allocation

The video controller does not have dedicated frame buffer memory but instead makes use of system memory for all its needs. This must be taken into account when the amount of system memory is chosen. When the on-board video controller is not used, it should be disabled completely by the BIOS Setup to prevent system memory being allocated to the controller.

The motherboard BIOS allocates system memory to the video controller to support legacy VGA graphics, controlled by a BIOS Setup option. The amount of system memory reported by the BIOS reflects this reduction when the on-board video controller is enabled. Once the operating system loads, the video driver dynamically allocates further system memory dependent on availability and the application requirement. Systems should have at least 128MB of system memory when using these graphics drivers. The amount of memory allocated is capped to 32MB for systems with 128MB. Consult the Intel DVMT 3.0 white paper for further information (http://support.intel.com/design/chipsets/applnots/302623.htm).

2.5 Disks

Two 150MB/s SATA ports with locking headers.

One Ultra ATA/100 interface via on-board 40-way boxed header.

- 40/80-pin cable host-side detection or forced in BIOS
- Support for hard disks and ATAPI drives
- BIOS support for 48-bit LBA (ATA drives >137GB)

Support for USB drives including boot

- Phoenix Multiboot XP support allows USB boot drives to be selected

Optional on-board MM/SD card slot via the USB 2.0 port (shared with one USB header)

- Internally accessible card (no external access)
- Based on Genesys GL817E controller

2.6 Diskette Drives

This product does not support Legacy floppy drives. Use a USB floppy drive if required.

2.7 Audio

The motherboard audio system comprises the chipset ICH6M digital audio controller and a Sigmatel STA9200 stereo audio CODEC. Three ATAPI headers provide CD-ROM and auxiliary stereo audio Line input, and stereo audio Line output connections. Two 3.5mm audio jacks on the I/O panel provide connections for stereo Line output, a monaural microphone input. The Line output and Microphone headers are duplicates of the I/O panel jacks – care must be taken if both connectors are being used simultaneously to ensure that the combined load does not have an adverse effect on the output levels. See the following table for the audio channel allocation and capability. The I/O panel jacks include “plug and play” (jack sensing) capability when using a suitable driver.

An on-board miniature speaker provides standard PC speaker functionality - error “beep”, for example.

Table 6. Audio Channel Allocation

I/O panel jack	Light Blue	Lime	Pink	N/A
Internal header	N/A	Yellow	White	Black
Nominal function	Line In	Line Out	Microphone	CD In
Line In capability	√	√	√	√
Line Out capability	√	√	√	
Microphone capability		√	√	
Headphone Out capability		√		

Note

It is possible to use both header and I/O panel jack at the same time when configured as a LINE output but this can affect drive levels depending on the load impedance. Do not connect to both header and jack if one load is a headphone.

Note

The internal headers do not support “plug and play” (jack sensing) and must be explicitly configured in the audio drivers when the I/O panel jacks are not used.

2.8 Network

The AB915GM provides one Ethernet port configured as either 10/100 or 10/100/Gbit. The list below describes the features provided by each device.

- 10/100Mbps Ethernet solutions IEEE 802.3 10Base-T and 100Base-TX compatible
  - MAC integrated into ICH with Intel 82562GZ transceiver
- Gbit Ethernet solutions IEEE 802.3 10Base-T, 100Base-TX, 1000Base-T compatible
  - Intel 82573V PCI Express Ethernet controller connected via I/O hub x1 lane
  - Full line-speed operation
- On-board RJ45 connector with two integral LEDs showing combined link integrity and activity (yellow) plus line speed (green/amber)

The Ethernet LED indicators are described in the following table.

Table 7. RJ45 LEDs

LED color	LED state	Indicates
Green/Amber	Off	10Mbps link speed
	Green	100Mbps link speed
	Amber	1Gbps link speed
Yellow	Off	No link established
	Steady on	Link established; communication activity not detected
	Blinking	Link established; communication activity detected

2.9 IEEE 1394b

The optional IEEE 1394b interface is provided by a Texas Instruments TSB82AA2 PCI controller and a TSB81BA3 physical layer interface. A single bi-lingual connector is available on the I/O panel, providing up to 800Mbps data rate capabilities.

Note

The performance of this interface is limited by the bandwidth of the 32-bit PCI bus, which is also shared by expansion slots 3 and 4.

Note

The interface does not have an isolated ground reference and is generally only suitable for applications where all nodes share a common ground.

2.10 Standard PC I/O

The AB915GM does not support the legacy I/O features of serial ports, parallel ports, PS/2 keyboard, PS/2 mouse or flexible diskette interfaces.

In order to support some operating systems that require a keyboard/mouse port, AB915GM provides a readable register at I/O location 064h which always returns zero to indicate that no PS/2 keyboard or mouse is present.

2.11 USB Ports

The motherboard provides eight independent USB 2.0 compliant ports, four on the I/O panel and up to four by internal headers (up to two of the four may not be available when the PCI Express Mini Card slot or the MM/SD controller are installed). The following table indicates how the USB channels are allocated to the hardware ports.

All ports provide a resettable fuse protected +5V supply to the peripheral. The chipset includes three 2-channel USB 1.1 controllers, which allow each port to operate in USB1.1 mode, and a single 8-channel USB2.0 controller, which provides USB2.0 support to each port when a high-speed peripheral is detected.

The BIOS provides emulation of standard keyboards and mice using USB devices using SMI-based routines to intercept traffic. Operating systems that do not support USB devices suffer performance degradation due to this activity. The legacy support activity is automatically switched off once a USB-aware operating systems loads.

Table 8. USB Channel Allocation

EHCI Port	UHCI Controller/Port	Allocation
7	4/1	I/O panel 3 (top)
6	4/0	I/O panel 2
5	3/1	I/O panel 1
4	3/0	I/O panel 0 (bottom)
3	2/1	Header (available on Mini-ITX)
2	2/0	Header (available on Mini-ITX)
1	1/1	FlexATX only. Header or MM/SD card controller (build option)
0	1/0	FlexATX only. Header shared with PCI-E Mini Card (use only one simultaneously)

2.12 General Purpose I/O Lines

To support products that require a small number of internal input or output lines (such as switches or LED indicators), the motherboard provides access to 13 general-purpose lines by a 20-pin header. Ten lines can be programmed as inputs or outputs (in two groups), two are input only and one is output only. It is the responsibility of the customer to provide suitable software to control these lines.

2.13 CMOS RAM & RTC

The chipset integrates a Motorola MC146818A compatible real-time clock (RTC) and 256 bytes of CMOS RAM that is used by the BIOS to store configuration information. A replaceable primary lithium “coin cell” battery (type CR2032) backs up both the RTC and the CMOS RAM, and provides approximately 5 years of un-powered backup.

When available, the RTC and CMOS RAM are powered from the +5V standby power rather than the lithium battery cell. The system management hardware can monitor the lithium cell voltage directly.

2.14 Expansion Cards

The motherboard provides 2 bus-master 5V PCI 2.3 compliant slots and two PCI Express x1 slots. The motherboard generates the 3.3Vaux supply to these slots using the 5V standby input from the power supply. Always ensure that the 5V standby rail can support the required current when using a PCI card that makes use of the 3.3Vaux supply. The AB915GM is designed to support a maximum total power consumption of 60W for all four slots (15W each, on average).

Slots 1 and 2 are the PCI Express x1 slots. Slots 3 and 4 are the PCI 2.3-compliant 5V 33MHz 32bit slots. PCI Express (x16) graphics cards are not supported.

2.15 System management

The motherboard includes hardware system management functions by the National Semiconductor LM85 device. They monitor system voltages, motherboard, processor and external temperatures, fan speed and control system fans. The following sections describe this in detail.

2.15.1 Voltage Monitoring

The following table details the motherboard voltage rails monitored and their usage.

Table 9. Voltage rails

Voltage Rail	Usage on Motherboard
+12V	Fans, expansion slots
+5.0V	Processor voltage regulator, internal voltage regulator for chipset and system memory, internal logic, USB and video ports, expansion slots
+3.3V	Internal voltage regulator for chipset and processor interface, firmware hub, clock generator, system monitor, audio, internal logic, expansion slots
VCPU	Processor core voltage
VBAT	This internal rail is used to power the RTC and the CMOS RAM

The processor voltage regulator generates the operating voltage automatically based on the processor voltage requirement indicated by the processor by the VID pins. The VID can be read by the control logic “General Control and Status” register (VID-5) and by the System Management Controller (LM85) on the SMBUS (VID0-4).

2.15.2 Temperature Monitoring

There are three thermal monitors, two of which connect to temperature sensors on the motherboard. The first measures the motherboard temperature using a sensor contained within the LM85. This is a localized reading dominated by the motherboard surface temperature around the component. The second temperature sensor is located on the processor die and thus accurately measures the local die temperature. Since the local die temperature fluctuates rapidly with activity, the controller within the LM85 filters the signal to produce an average temperature.

Note

There is temperature deviation across the processor die that cannot be observed by this sensor. Intel provides information on this in the processor datasheet. A third sensor can be connected to the motherboard using the external sensor connector. The sensor should be a silicon diode or transistor connected as a diode, such as a Fairchild MMBT3904.

2.15.3 Fan Monitoring

The motherboard supports three fan monitors that check the fan tachometer signals to determine the rotational speed. Fan speeds can be monitored by software to provide early warning of a failing fan, indicated by a slower than normal rotational speed.

Note

When a fan is temperature controlled, the speed is determined by the control mechanism and the fan will sometimes be intentionally slowed or stopped – monitoring software must accommodate this.

The three fan tachometer monitors are assigned to fans as follows. Fan monitor 2 is not supported.

Table 10. Fan monitors

	Usage by motherboard
Fan monitor 1	Processor fansink (see motherboard layout section)
Fan monitor 3	System fan 1 (see motherboard layout section)
Fan monitor 4	System fan 2 (see motherboard layout section)

2.15.4 Fan Control

The motherboard supports individual variable speed controls for the processor fansink and the two system fans by pulse-width modulation of the fan drive output voltage. In addition to direct software control, the LM85 supports automatic fan control based on the temperature indicated by the three thermal sensors. Each sensor defines a thermal zone and the fans can then be independently assigned to these zones. Parameters defining PWM frequency, temperature range, spin-up delays etc. are programmed into the LM85 to enable automatic control. The default parameter set programmed by the BIOS can be customized.

2.15.5 Tamper Detection

The motherboard supports tamper detection security that operates by a chassis tamper switch connected to the front panel connector. When the motherboard detects this signal low the BIOS can be configured to display a warning message or to require a password at the next boot. Since the lithium cell powers the logic, the tamper detection continues to operate even if the board is un-powered.

2.16 Power management

The AB915GM motherboard implements a number of power management features via ACPI.

2.16.1 ACPI Power States

An ACPI-aware operating system directs the power management of the motherboard – causing various devices within the system to change power state as appropriate. The following table describes the ACPI power states available using the motherboard with a soft-switched power supply.

Table 11. ACPI Power States

Global State	Sleep State	Device State	Description
G0	S0	C0, D0	Fully operational, all devices powered.
G0	S0	C1, D1, D2	Sleep state. CPU is stopped but all devices are powered.
G0	S0	C2, D1, D2	Sleep state. CPU is stopped with internal clocks stopped but all devices are powered.
G0	S0	C3, D1, D2	Sleep state. CPU is stopped with internal clocks disabled but all devices are powered.
G1 Sleeping	S4 Suspend to disk	D3	System context is saved to disk and power removed from all circuits except that required to resume.
G2/S5	S5 Soft Off	D3	All devices are un-powered. Memory contents and context are lost. Wake-up from PCI PME (including on-board LAN) possible if enabled via BIOS Setup (and drivers).
G3 Mechanical Off	No power	No power	System is un-powered with no standby rails. No wake-up is possible.

2.16.2 ACPI Wake-up Support

The following table indicates which events can cause an ACPI wake-up and from which sleep states.

Table 12. ACPI wake-up support

Event	Sleep State	Comment
Power switch	S0, S4, S5	
RTC alarm	S0, S4	
PS/2 keyboard or mouse	S0	Ports are un-powered in S4, S5
USB device (any port)	S0	Ports are un-powered in S4, S5
On-board LAN	S0, S4, S5	S5 if enabled via BIOS Setup
PCI PME signal	S0, S4, S5	S5 if enabled via BIOS Setup

2.17 Indicators

2.17.1 Power State Indicators

The motherboard supports a single dual-color LED indicator that shows power status. It is possible to use a single-color LED although some functionality is lost. The following table describes how the indicator is driven when operating with both single and dual-color devices and assumes 5V standby power is available.

Table 13. Power state indicators

LED	LED state	Indicates
Single color	Off	The motherboard is powered down or in one of the ACPI sleep states.
	On	The motherboard is fully powered up.
Dual color (green/yellow)	Off	The motherboard is powered down or in ACPI sleep states S4 or S5 (no +5V supply available).
	Green	The motherboard is fully powered up.
	Yellow	The motherboard is in sleep state.

2.18 BIOS

The motherboard employs the RadiSys PH915 system BIOS, which is based on Phoenix Technologies' First BIOS Notebook Pro, held within an 8Mbit flash ROM device called the firmware hub (FWH) and containing the following code.

- System BIOS, POST and configuration (Setup) utility
- Video BIOS (Intel)
- Product configuration information including boot logo and CMOS defaults
- Processor microcode updates
- Customizations including boot logo (Phoenix "Splash 2")
- Network remote boot and PXE code

The code is built from a number of software and data modules that can be customized and assembled with a software tool available from RadiSys. Software to support BIOS updates and crisis recovery is also available - see the Manuals, Drivers & BIOS section on www.radisys.com for BIOS updates and support software.

The configuration of the motherboard is generally automatic with intervention possible via the built-in BIOS Setup utility. The operation and feature set are described in the BIOS chapter of this document.

2.19 Operating Systems Support

The following operating systems are validated by RadiSys with the AB915GM motherboard. Contact RadiSys for information on the support of other operating systems. For device drivers, see the Manuals, Drivers & BIOS section on www.radisys.com.

- Microsoft Embedded Windows XP, Windows XP, Windows 2000
- Red Hat Enterprise Linux WS v3
- Novell SUSE Linux Professional v9.2
- Knoppix Linux v3.6

3. Specifications

The following sections specify the conditions required for correct operation of the motherboard, usage information and regulatory and industry compliance statements. Failure to operate the product within its specification can result in system failures or reduce product lifetime.

3.1 Environmental

The following table details the environmental operating limits and the calculated product reliability data.

Table 14. Environmental Specifications

Characteristic	State	Value
Temperature[3] (ambient)	Operating	0°C to +70°C (Operation above +30° C reduces the maximum operational relative humidity)
	Operating gradient	±5°C per minute
	Storage	-40°C to +85°C, 5°C per minute maximum excursion gradient.
Relative humidity	Operating	10% to 85% RH non-condensing at +30°C, linearly decreasing to 5% to 15.5% RH non-condensing at +65°C
	Storage	5% to 90% RH non-condensing at +40° C
Vibration	Operating	Random 5Hz to 2kHz, 7.7grms, 10 mins in each of 3 axes 5Hz to 20Hz: 0.004g2/Hz ramping up to 0.04g2/Hz; 20Hz to 1000Hz: 0.04g2/Hz; 1000Hz to 2000Hz: 0.04g2/Hz ramping down to 0.01g2/Hz
	Packaged	Random 5Hz to 2kHz, 9.7grms, 10 min. in each of 3 axes 5Hz to 20Hz: 0.006g2/Hz ramping up to 0.06g2/Hz; 20Hz to 1000Hz: 0.06g2/Hz; 1000Hz to 2000Hz: 0.06g2/Hz ramping down to 0.02g2/Hz Sine 5Hz to 500Hz, 0.15 octave/min up and back, 10 min. dwell at 3 resonance's in each of 3 axes 5 to 50Hz swept – 0.1g; 50 to 500Hz swept – 0.25g
Shock	Non-operating	30g 11ms, half-sine
	Packaged	Drop test, 10-up bulk packaging, 30 inches free-fall, 152 inches/s velocity change
Altitude	Operating	To 15000 ft. (4500m)
	Storage	To 40000 ft. (12000m)
MTBF		The table below summarizes the MTBF (hr) predictions for three configurations of the AB product. Note that the predictions were run without the main processor or battery included. **SKU 35ºC 55ºC** ABGD00 332,350 hours 192,903 hours ABW00 333,503 hours 199,188 hours ABF00 329,585 hours 189,333 hours
Fuses		Self-resetting

[3] See the Thermal Specification section. This specification must be met at all points across the motherboard.

3.2 Thermal

The ambient operating temperature range for the motherboard is 0 to 70°C but the selection of processor and heatsink (or fansink) can reduce the system operating range. The processor and fansink combinations normally supplied as standard with the motherboards are tested by RadiSys to the full operating range, using software designed to cause maximum power dissipation in the processor. This testing is done in an environmental test chamber with forced-air circulation. The maximum operating temperature of the supplied processor and fansink combination is specified in the "Endura Processor Support" document, which can be found in the Support & Service section of the RadiSys website.

CAUTION

- Always test the final system configuration to determine if the operating temperature range limits for the motherboard and processor are being met. Failure to do so can lead to unstable operation, motherboard or processor damage and/or shortened life.

3.3 Regulatory EMC Compliance

When correctly installed in a suitable chassis, the AB915GM motherboard is designed to meet these EMC regulations:

- FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B)
- EN55022:1998 Class B
- EN55024:1998

3.4 Regulatory Safety Compliance

When correctly installed in a suitable chassis, the AB915GM motherboard is designed to meet these safety regulations:

- UL60950/07.95
- CAN/CSA-C22.2 No. 950-95
- IEC60950, 1991 2nd edition with amendments 1, 2, 3, and 4

3.5 Industry Compliance

The AB915GM motherboard implements the industry specifications shown in the following table.

Table 15. Industry specifications

Specification	Description	Revision
ACPI	Advanced Configuration and Power Interface Specification	2.0
ATAPI	ATA Packet Interface for CD-ROMs	2.5
ATX	ATX Motherboard Form Factor Specification	2.03
MicroATX	MicroATX Motherboard Interface Specification	1.1
FlexATX	FlexATX addendum to Motherboard Interface Specification	1.0
PCI	PCI Express Base Specification	1.0
	PCI Express Card Electromechanical Specification	1.0a
	PCI Express Mini Card Electromechanical Specification	1.0
	Peripheral Component Interconnect Local Bus Specification	2.2
	PCI Power Management Interface Specification	1.1
USB	Universal Serial Bus Specification	2.0

3.6 Miscellaneous

Table 16. Miscellaneous specifications

Parameter	Conditions	Specification
RTC Clock accuracy	25°C, 3.3V	+/- 25 ppm max.
Processor fan drive capability	12.0V	800mA max.
System fan drive capability	12.0V	450mA max.

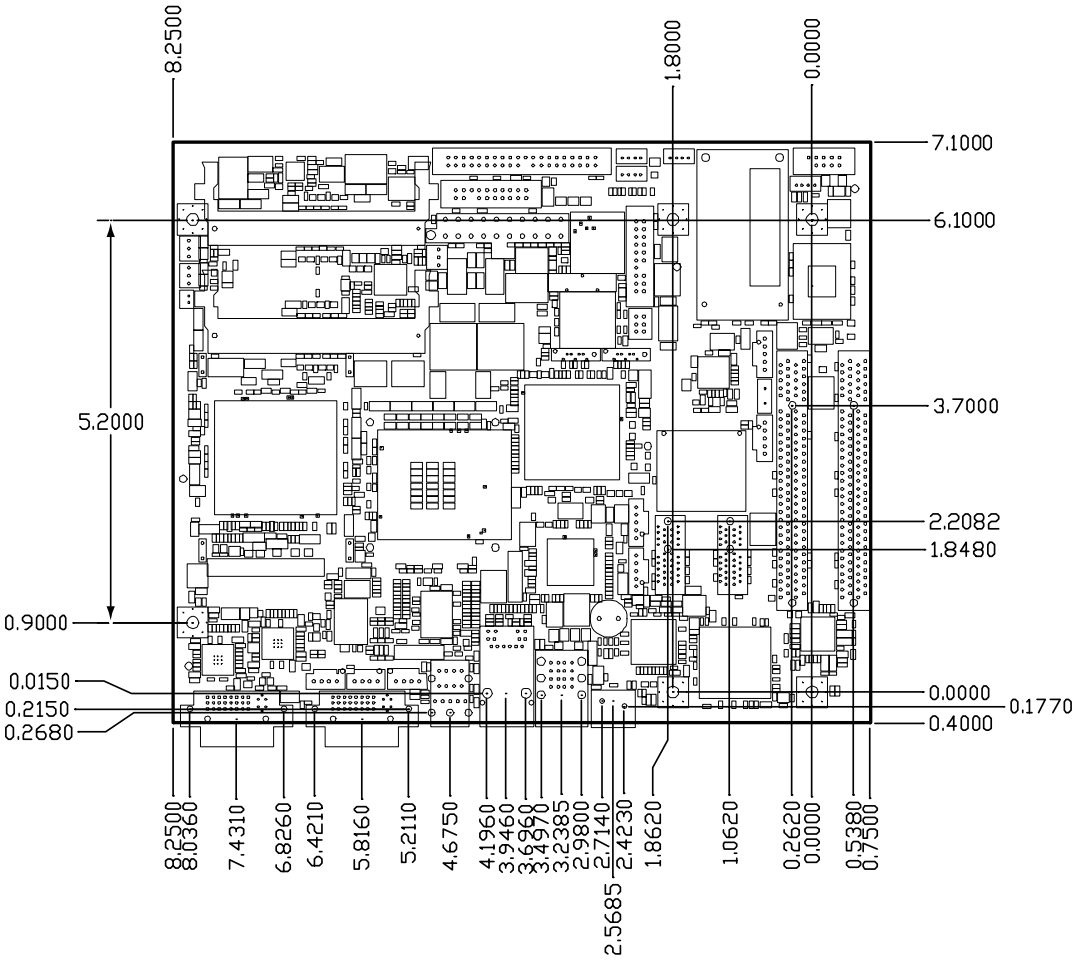
3.7 Mechanical

3.7.1 Motherboard

The AB915GM motherboard meets the microATX Motherboard Interface Specification, v1.1 and the ATX Specification, v2.03 (the ATX12V power is not required). It measures 9.0 x 7.5 inches and is manufactured using a 8-layer PCB with components on the topside only. The screen-printing includes:

- Product Name, RadiSys part number, and RadiSys branding
- Location for serial number and product labels
- Selected component reference designators

Figure 4. AB915GM motherboard dimensions



3.7.2 I/O Shield

Two I/O shields suitable for standard ATX chassis (press-fitted into I/O aperture) are specified. Others may be required dependent on SKU options defined.

- Dual audio jack, no 1394b
- Dual audio jack, 1394b

3.7.3 Heatsinks

The following heatsink solutions are supported:

- GMCH – clip-on passive heatsink as used on Pentium 4 products.
- Processor – fansink, 12V with speed control and monitoring (3-wire fan), is supplied with the processor.
- ICH6M – not fitted on standard, use an adhesive passive heatsink if required
- Ethernet controller – no support for heatsink
- Global heatsink – the board supports additional mounting holes for a single passive heatsink (complex multi-height underside) to cover processor, GMCH, ICH and Ethernet controller. There are no plans to design or validate this configuration.

3.8 Electrical

3.8.1 Motherboard Power Consumption

The motherboard power consumption is highly dependent on the processor, memory and devices attached and also on the software that is running and the power state that the board is in. The figures given in the tables below are a guide to the power requirements to expect under selected conditions. They should not be interpreted as maximum requirements.

The figures are based on measurements of a real system configured as shown in the following table.

Table 17. Configuration for Power Requirements

Memory	2 off 512MB DDR2 PC2-4300 SO-DIMM modules
Drives	Powered independently
Video	On-board
Network	On-board (dual LAN, not operating)

Table 18. Intel Pentium M at 2.0GHz with 533MHz Processor Bus

	Motherboard Current (A)					Power
Mode	+3.3V	+5V	+12V	–12V	+5Vsby	Total
BIOS Setup Screen	0.7	2.8	0.2	0	0.03	19W
Windows XP desktop idle	0.7	3.4	0.2	0	0.02	22W
Windows XP hibernate	0	0	0	0	0.25	1.3W
Windows XP shutdown	0	0	0	0	0.2	1.0W
Windows XP standby	0	0	0	0	0.3	1.5W
Windows XP stress test	0.7	5.6	0.2	0	0.03	33W

Table 19. Intel Pentium M at 1.8GHz with 400MHz Processor Bus

	Motherboard Current (A)					Power
Mode	+3.3V	+5V	+12V	–12V	+5Vsby	Total
BIOS Setup Screen	0.8	2.9	0.1	0	0.01	19W
Windows 2000 desktop idle	0.8	5.2	0.1	0	0.1	31W
Windows 2000 hibernate	0	0	0	0	0.25	1.3W
Windows 2000 shutdown	0	0	0	0	0.2	1.0W
Windows 2000 stress test	0.9	5.5	0.1	0	0.01	32W

Table 20. Intel Celeron M at 1.5GHz with 400MHz Processor Bus

Mode	Motherboard Current (A)					Power
	+3.3V	+5V	+12V	-12V	+5Vsby	Total
BIOS Setup Screen	0.7	3.5	0.2	0	0.03	23W
Windows XP desktop idle	0.7	2.6	0.2	0	0.02	18W
Windows XP hibernate	0	0	0	0	0.25	1.3W
Windows XP shutdown	0	0	0	0	0.2	1.0W
Windows XP standby	0	0	0	0	0.3	1.5W
Windows XP stress test	0.7	3.7	0.2	0	0.03	24W

3.8.2 Power Delivery to Expansion Slots

The following table indicates the maximum current that should be drawn from each expansion slot – do not exceed these ratings. PCI slots are limited to 25W in total on the main +5.0V and +3.3V supplies, all of which can be drawn from either voltage rail. The figures for the riser are for the total current/power delivered to the riser through the motherboard. If more is required, the riser must draw power from an additional source such as a separate power connector from the PSU.

Table 21. Maximum Expansion Slot Current

Slot	+3.3V	+5V	+12V	–12V	+3.3Vaux[4]
PCI-E x1	3.0A (9.9W)	N/A	0.5A (6W)	N/A	375mA/20mA (1.3W/0.1W)
PCI	7.6A (25W) [5]	5.0A (25W) [5]	0.5A (6W)	100mA (1.2W)	375mA/20mA (1.3W/0.1W)

DANGER

Do not exceed the limits for each slot or voltage rail shown in the previous table.

3.8.3 Power Supply Selection

The motherboard is designed to operate with an ATX compatible power supply, as defined in section 3 of the MicroATX v1.1 specification. The provision of a 5V standby power rail is optional but, if not provided, the soft-switched power supply control features of the motherboard cannot be used. Where the standby rail is provided, ensure it can provide sufficient current for the motherboard, particularly for the motherboard LAN controllers and when an adapter card that draws current from the auxiliary 3.3V supply is used. The ATX -5.0V or –12V rails are not used by the motherboard.

[4] One wake-enabled card at 375mA and the remainder at 20mA.

[5] The combined PCI slot power consumption via the +3.3V and +5.0V supplies is a maximum of 25W.

Table 22. Power Supply Selection

Voltage Rail	Tolerance	Voltage Rail	Tolerance
+5.0V DC	± 5%[6]	+3.3V DC	± 5%
+12.0V DC	± 5%	+5.0V DC standby	± 5%

Note

When operating with a hard-switched power supply, the BIOS should be customized with the PSU flag in the enclosure data set to "Hard-Switched" using the tools described in the BIOS Customization section of this document.

CAUTION

Ensure the power supply can support the required load current on all rails – failure to meet this can cause damage to the power supply or the motherboard. Pay particular attention to the 5V Standby power requirement — the LAN controllers are powered from this rail.

DANGER

The power supply must be properly approved by a third party agency for use in IEC/EN/UL/CSA 60950 applications.

3.8.4 Power Budget

The following table gives an example power budget for the motherboard with processor, memory and expansions cards fitted. The figures are based on the maximum figures from the motherboard power consumption section of this document (measured under stress testing except for the standby rail) and they should not be interpreted as typical values. Before choosing a power supply, always create a power budget for your system. These figures yield a total power requirement of 172W.

Table 23. Power Budget

	Motherboard Current					Power
	+3.3V	+5V	+12V	–12V	+5Vsby	
Motherboard	0.9A	5.5A	0.1A		0.01A	32.0W
Eight USB ports		4.0A				20.0W
Slots (total)	21.2A	10.0A	2.0A	0.2A	0.44A	98.4W
Fans			1.7A			20.4W
Front panel		0.1A				0.5W
Video DDC channel		0.05A				0.3W
Total	22.1A	19.7A	3.8A	0.2A	0.45A	172W

[6] To meet the USB output supply voltage specification, the minimum +5V should be 4.90V.

3.8.5 General Purpose I/O Lines

Table 24. General Purpose I/O Lines

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5	V
V_{IL}	Input Low Voltage		–0.3	0.8	V
I_{IL}	Input Leakage Current	V_{IN} = 3.6V, V_{CC} = max		5	µA
		V_{IN} = 0V, V_{CC} = max		–5	µA
V_{OH}	Output High Voltage	I_{OH} = -3.2mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24mA[7]		0.5	V

[7] Total I_{OL} of outputs within each port must not exceed 64mA, for ports 1 and 2.

4. Motherboard BIOS

4.1 Configuration

The motherboard BIOS includes a Setup utility that can be used to both view and modify the board's configuration. The settings are stored in CMOS RAM with the default settings held in the flash ROM. To start the utility, press the **F2** key when prompted. If "silent-boot" is on (logo displays) then press the **ESC** key to show the start-up messages.

The display is divided into these areas:

- Top bar shows the five main menus
- Large left area: shows the options
- Large right area: displays help text specific to the highlighted option or menu
- Bottom bar: shows the action of the active keys

The primary menus are briefly described in the following table. The help text describes each option more fully. Many options have sub-menus.

Table 25. BIOS menus

Menu	Options
Main	Product description including processor and memory fitted. Date and time.
Information	Product information. Status of system monitors.
Configuration	Peripheral device configuration I/O device and expansion slot configuration Power control System monitors configuration Security passwords and permissions Console redirection configuration
Boot	Selects device boot order. Start-up display mode (silent-boot etc.) Operating system type (ACPI etc.).
Exit	Save with or without changes.

4.2 Update and Recovery

This section describes how to update the code and data held in the BIOS ROM. The process should be undertaken with care and must not be interrupted. A recovery mechanism is also described that enables a corrupted BIOS ROM (as a result of an interrupted update, for example) to be repaired.

Updates are available online from the RadiSys site in the form of a compressed image (ZIP) of a number of files. Using the software contained in the ZIP file, you must first create a flash diskette that is then used for the update or recovery process. Included in the ZIP file is a Readme.txt file that contains information on the update and instructions on how to use it. Always read this document before proceeding as it may contain updates to the descriptions below.

The update process assumes you have a PC that can be used to create an update diskette and that the system to update or recover has a diskette drive attached.

> **CAUTION**
>
> Updating the BIOS is a process that should be undertaken with caution. Always complete the process before powering-down or restarting the motherboard – failure to do this may result in a corrupted BIOS that will require recovery.

4.2.1 Creating a BIOS Update Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95 or Windows 98 and a blank diskette.

1. Obtain the update ZIP file from the Manuals, Drivers and BIOS section on the RadiSys website, www.radisys.com.
2. Unzip the contents to an empty directory on your hard drive.
3. Insert a blank diskette into the floppy drive.
4. Run CRISDISK from the directory created in step 2 to create the update diskette.
5. Follow the steps as directed. A copy of MS-DOS "Format.com" must be available for CRISDISK to complete successfully.

4.2.2 Updating the System BIOS

The system BIOS can be updated from MS-DOS without changing jumpers as described below. It is recommended that you create a recovery diskette (described later) before updating the BIOS. This operation does not affect the customization area in the BIOS. If you use the BIOS Setup utility CMOS Save and Restore functions to save a set of defaults, you need to recreate and re-save these once the update is complete.

1. Create an update diskette as described above.
2. Boot the system to be updated into MS-DOS without memory managers or boot from the update diskette.
3. If you did not boot from the update diskette, do the following.
   A. Insert the update diskette into the floppy drive.
   B. Change the MS-DOS directory to match the floppy drive's directory.
   C. Type UPDATE and press Enter.
   D. Follow the instructions to initiate the update. When it is finished, the following message appears:

```
Flash memory has been successfully programmed
PRESS ANY KEY TO RESTART THE SYSTEM
If the system does not restart
TURN THE POWER OFF, THEN ON
```

   E. Turn off the system power and re-boot. The motherboard boots using RadiSys defaults.

If the update operation fails for any reason (if it was interrupted, for example), and the motherboard no longer operates, then the BIOS must be recovered.

4.2.3 Creating a BIOS Recovery Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95, Windows 98 or Windows NT and a blank diskette.

1. Obtain the update ZIP file from the Manuals, Drivers & BIOS section on the RadiSys website, www.radisys.com.
2. Unzip the contents to an empty directory on your hard drive.
3. Insert a blank diskette into the floppy drive.
4. Run CRISDISK /R from the directory created in step 2 and follow the steps as directed to create the recovery diskette. A copy of MS-DOS Format.com must be available for CRISDISK to complete successfully.

4.2.4 Recovering the System BIOS

The recovery diskette should be used to recover a system BIOS when the motherboard no longer operates after a failed BIOS update operation. The process is described below.

1. Remove the operating mode selection jumper to place the board into the recover mode (see Configuration section of this document).
   A. Turn off the power.
   B. Remove any covers to gain access to the jumper.
   C. Remove the jumper from the operating mode selection block
2. Insert the recovery diskette into the floppy drive.
3. Power up the motherboard when you hear the following audio signals from the on-board speaker. If you cannot hear the speaker, wait for approximately 1 minute after all activity has stopped to ensure the operation has completed.

Table 26. Beep codes

Beep code	Definition
One short beep	BIOS update begins.
One long beep	BIOS update is finished.
Three beeps	This indicates an error.

4. Power down the motherboard.
5. Refit the jumper into the normal operating position and replace the system cover(s).
6. Power up the motherboard. The recovery process is now complete and the product should boot normally.

4.2.5 Updating the Flash Bootblock

There is an area of the BIOS ROM, the bootblock, which is normally not updated. It contains code to perform the recovery process and data that identifies the motherboard. Occasionally, a BIOS release may require this bootblock area to be updated and the update disk will do this automatically. However, exercise caution when attempting such an update as a damaged bootblock area means that the motherboard may need to be returned to RadiSys for repair.

CAUTION

Exercise caution when updating BIOS that includes a bootblock update. If this process is interrupted, the motherboard cannot be recovered and must be returned to RadiSys for repair.

4.3 Customization

There are a number of features of the BIOS that can be customized and the software to accomplish this is contained within the BIOS OEM kit ZIP file that can be obtained from the Manuals, Drivers & BIOS section on the RadiSys website, www.radisys.com. The “Readme.txt” file also contained in this ZIP provides updated customization information and should be read before proceeding.

The process involves creating a new update disk that contains the customized BIOS. The steps below guide you through the process.

1. Obtain both the updated and OEMKIT ZIP files from the Manuals, Drivers & BIOS section on the RadiSys website, www.radisys.com.
2. Unzip the contents of the update ZIP to an empty directory on your hard drive.
3. Unzip the contents of the OEMKIT ZIP to the same directory as step 2. This may replace some files.
4. Replace the “Logo.bmp” file with a customized logo if required (see description below).
5. Replace the “P6upd.bin” file with a customized version if required (see description below).
6. Run MAKEBIOS to create the customized binary.
7. Create the update diskette by running CRISDISK /O with a blank diskette in the floppy drive and following the instructions.
8. Using a reference or “gold” board, update its BIOS with the diskette created in step 6 above using the standard update procedure.
9. Re-boot the board and run the BIOS Setup utility.
10. Configure the board as required.
11. From the Exit menu, save the new settings to flash and re-boot the board with the update disk still in the floppy drive.
12. There should be no reported difference between disk and ROM BIOS versions at this point and you are prompted to read-back the BIOS. Select this to extract the motherboard ROM image and save it to the update disk, replacing the BIOS binary in the file BIOS.ROM.
13. The diskette is now a fully customized update disk. Save the BIOS.ROM file back to the directory on your hard disk used in step 2, replacing the previous version.
14. Create a new version of the update disk by running CRISDISK (with no switches) with a blank diskette in the floppy drive and following the instructions.

The “Splash 2” logo customization process requires Phoenix Technologies software which RadiSys is not licensed to deliver to customers. Consequently, RadiSys must provide the customization service to create the logo. See the Phoenix Technologies Splash 2 specification for more details on the logo files required. The logo itself is stored in one of the available 64kB ROM blocks.

Intel microprocessors allow for their microcode to be updated by the BIOS to workaround some outstanding errata. Each processor type and revision has a unique update image and the BIOS supports a maximum of four contained in the “P6upd.bin” file. To customize the processor microcode update selections, create a new version of this file by concatenating four microcode updates in binary form — these can be obtained from Intel.

4.4 BIOS Error Indications

Once the motherboard powers-up the BIOS code runs Power-On-Self-Test software to check that the motherboard is operating correctly. During this process, the code writes an 8-bit value to an error port at various code checkpoints. If a fatal error is determined, then the error code indicates the last successful checkpoint reached. The BIOS attempts to write this code to the display. The error port (I/O location 80h) can be read via “off-the-shelf” Debug cards. The following table lists the checkpoint codes.

There are a number of checkpoints that also generate an audible “beep” code on failure using the standard PC speaker (also routed though the motherboard audio system). The beep codes are made up of up to four groups of short beeps and are also listed in the following table.

Once the video is enabled, further errors generated during and after POST are sent to the video display as text messages. These messages always display unless the motherboard is configured for silent boot or headless (no keyboard, mouse or display) operation.

Table 27. BIOS POST Check Point codes

Addr	Description	Addr	Description
02h	Verify Real Mode	89h	Enable NMI
04h	Get CPU type	8Ah	Initialize Extended BIOS Data Area
06h	Initialize system hardware	8Bh	Initialize mouse
08h	Initialize chipset registers with initial POST values	8Ch	Initialize floppy controller
09h	Set in POST flag	8Fh	Hard disk controller fast pre-initialization
0Ah	Initialize CPU registers	90h	Initialize hard disk controller
0Bh	Enable CPU cache	91h	Initialize local bus hard disk controller
0Ch	Initialize cache to initial POST values	92h	Disable unused PCI clocks
0Eh	Initialize I/O	93h	Build MPTABLE for multiprocessor boards
0Fh	Initialize local bus IDE	95h	Install CDROM for boot
10h	Initialize Power Management	97h	Fix up MP table
11h	Load alternate registers with initial POST values	98h	Search for option ROMs (beep for bad checksum)
13h	Reset PCI BM	9Ah	Shadow option ROMs
14h	Initialize keyboard controller	9Ch	Set up Power Management
16h	BIOS ROM checksum	9Dh	Initialize security

Table 27. BIOS POST Check Point codes

Addr	Description	Addr	Description
17h	Pre-size DRAM	9Eh	Enable hardware interrupts
18h	8254 timer initialization	9Fh	(Second) HDD fast initialization
1Ah	8237 DMA controller initialization	A0h	Set time of day
1Ch	Reset Programmable Interrupt Controller	A2h	Check keylock
20h	Test DRAM refresh	A4h	Initialize typematic rate
22h	Test 8742 Keyboard Controller	A8h	Erase F2 prompt
24h	Set ES segment to register to 4GB	AAh	Scan for F2 keystroke
28h	Autosize DRAM	ACh	Enter SETUP
29h	Initialize PMM	AEh	Clear in-POST flag
2Ah	Clear 512KB base RAM	B0h	Check for errors
2Ch	Test 512KB base address lines	B2h	POST done--prepare to boot operating system
2Eh	Test low byte of 512KB base memory	B4h	One beep before boot
2Fh	Pre-System Shadow	B5h	Quiet boot end/Display MultiBoot menu
32h	Test CPU bus-clock frequency	B6h	Check password (optional)
33h	Initialize PDM	B9h	Prepare to boot
38h	Shadow system BIOS ROM	BAh	DMI
3Ah	Auto-size cache	BCh	Clear parity checkers
3Ch	Configure advanced chipset registers	BDh	Boot Menu
3Dh	Load alternate registers with CMOS values	BEh	Clear screen (optional)
42h	Initialize interrupt vectors	BFh	Check virus and backup reminders
45h	Core Device Init	C0h	Try to boot with INT19
46h	Check ROM copyright notice	C1h	Initialize PEM
48h	Check video configuration against CMOS	C2h	PEM log
49h	Initialize PCI bus and devices	C3h	PEM Display
4Ah	Initialize all video adapters in system	C4h	PEM sys error initialization
4Bh	Display QuietBoot™ screen	C5h	Dual CMOS
4Ch	Shadow video BIOS ROM	C6h	Docking initialization
4Eh	Display copyright notice	C7h	Late docking initialization
50h	Display CPU type and speed	C8h	Force check (optional)
51h	Initialize EISA board	C9h	Extended checksum (optional)
52h	Test keyboard	D2h	Unknown interrupt error
54h	Set key click if enabled	E0h	Initialize the chipset
58h	Test for unexpected interrupts	Elh	Initialize the bridge
59h	Initialize PDS	E2h	Initialize the CPU

Table 27. BIOS POST Check Point codes

Addr	Description	Addr	Description
5Ah	Display prompt "Press F2 to enter SETUP"	E3h	Initialize system timer
5Bh	CPU cache off	E4h	Initialize system 1/0
5Ch	Test RAM between 512KB and 640KB	E5h	Check force recovery boot
60h	Test extended memory	E6h	Checksum BIOS ROM
62h	Test extended memory address lines	E7h	Go to BIOS
64h	Jump to UserPatch1	E8h	Initialize Multi Processor
66h	Configure advanced cache registers	E9h	Set Huge Segment
68h	Enable external and CPU caches	EAh	Initialize OEM special code
6Ah	Display external cache size	EBh	Initialize PIC and DMA
6Ch	Display shadow message	ECh	Initialize Memory type
6Eh	Display non-disposable segments	EDh	Initialize Memory size
70h	Display error messages	EEh	Shadow Boot Block
72h	Check for configuration errors	EFh	System memory test
76h	Check for keyboard errors	F0h	Initialize interrupt vectors
7Ch	Set up hardware interrupts vectors	Flh	Initialize Run Time Clock
7Eh	Test coprocessor if present	F2h	Initialize video
80h	Disable onboard I/O ports	F3h	Initialize Beeper
81h	Late device initialization	F4h	Initialize Boot
82h	Detect and install external RS232 ports	F5h	Clear Huge segment
83h	Configure IDE controller	F6h	Boot to Mini DOS
85h	Initialize PCI PCC devices	F7h	Boot to Full DOS
86h	Re-initialize onboard I/O ports	FBh	Missing Microcode Update.
87h	Configure MCD devices	FEh	Thermal Configuration or Limits. See *Temperature* Sub-Menu.

Table 28. BIOS POST checkpoint codes with beep

Check point Code		Beep Code
16h	BIOS ROM checksum	1-2-2-3
20h	Test DRAM refresh	1-3-1-1
22h	Test 8742 Keyboard Controller	1-3-1-3
28h	Autosize DRAM	1-3-3-1
29h	Initialize PMM	1-3-3-2
2Ch	Test 512KB base address lines	1-3-4-1
2Eh	Test low byte of 512KB base memory	1-3-4-3

Table 28. BIOS POST checkpoint codes with beep

Check point Code		Beep Code
34h	Test CMOS RAM	1-4-3-1
3Ah	Auto-size cache	1-4-3-3
46h	Check ROM copyright notice	2-1-2-3
58h	Test for unexpected interrupts	2-2-3-1
90h	Initialize hard disk controller	3-2-1-1
98h	Search for option ROMs (beep for bad checksum)	1-2
B4h	One beep before boot	1
DFh	A20 Error	4-2-4-4

5. References

5.1 Industry Standard References

Table 29. Industry Standard References

Specification	Description	Location
ACPI	Advanced Configuration and Power Interface specification	www.acpi.info
Intel 915GM Chipset	915GM Family Specification	http://developer.intel.com/design/mobile/datashts/305264.htm
	ICH6 Family Specification	http://developer.intel.com/design/chipsets/datashts/301473.htm
Intel Pentium M processor	Intel Pentium M processor datasheet	http://developer.intel.com/products/notebook/processors/pentiumm/index.htm
Intel Celeron M processor	Intel Celeron M processor datasheet	http://developer.intel.com/products/notebook/processors/celeron_m/index.htm
ATX, microATX, FlexATX	Form factor specifications	www.formfactors.org
PCI	PCI local bus specification	http://www.pcisig.com/specifications/conventional/conventional_pci_23/
PCI Express	PCI Base Specification	http://www.pcisig.com/specifications/pciexpress/
	PCI CEM Specification	
	PCI Mini Card Specification	
DDR2 SDRAM SO-DIMMs	Memory module specifications	http://developer.intel.com/technology/memory/ http://www.jedec.org/
SMBus	System management bus	www.smbus.org
USB	Universal Serial Bus specification	www.usb.org/developers
VESA	Video Electronics Standards Association	www.vesa.org
SATA	Serial ATA	www.serialata.org

A Technical Reference

A.1 I/O Map

Table 30. I/O map

Address (hex)[8]	Description
0000 – 000F	DMA controller 1
0020 – 0021	Interrupt controller 1
0040 – 0043	Timer counter
0060, 0064	Keyboard controller emulation register (returns zero)
0062, 0066	Motherboard control registers
0070 – 0073	RTC and CMOS RAM
0080 – 008F	DMA controller page registers (for channels 1 and 2)
0092	PC compatible Port 92 (fast A20 and PIC)
00A0 – 00A1	Interrupt controller 2
00B2 – 00B3	Advanced power management (APM) control registers
00C0 – 00DF	DMA controller 2
00F0	Floating point error control
0170 – 0177	Secondary IDE controller (mapped to SATA or PATA interface)
01F0 – 01F7	Primary IDE controller (mapped to SATA or PATA interface)
0374 – 0376	Secondary IDE controller (mapped to SATA or PATA interface)
x3B0 – x3BB	VGA controller
x3C0 – x3CF	EGA controller registers
x3D4 – x3DA	CGA controller registers
03F6 – 03F7	Primary IDE controller (mapped to SATA or PATA interface)
04D0 – 04D1	Interrupt controller
0CF8 – 0CFF	PCI configuration address and data registers
1000 – 105F	ACPI registers
1060 – 107F	TCO controller
1200 – 12FF	Audio mixer
1300 – 133F	Audio master
FFA0 – FFA7	Primary IDE bus master registers
FFA8 – FFAF	Secondary IDE bus master registers
Dynamically assigned	USB controller (four) (32 locations on 32-byte boundary)
Dynamically assigned	SMBus controller (16 locations on 16-byte boundary)
Dynamically assigned	LAN controller (4096 locations on a 4096-byte boundary)

[8] An “x” prefix for the address indicates that only the low-order 10 address bits are decoded.

A.2 PCI Interrupt Allocation

In order to share PCI interrupts efficiently, the routing of the PCI interrupts INTA - INTD to the motherboard PCI interrupts PIRQE – PIRQH are rotated for each slot. Thus the PCI card INTA signals for the PCI slots are spread across these four motherboard inputs. Interrupt routing for the riser slots is determined by the riser design. Entries marked INTx are assignable in software. Some options can be overridden via the system enclosure/baseboard data (BIOS customization).

Table 31. PCI interrupt allocation

Device	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
Slot 1 (PCI-E x1)	INTA	INTB	INTC	INTD	–	–	–	–
Slot 2 (PCI-E x1)	INTD	INTA	INTB	INTC	–	–	–	–
Slot 3 (PCI 2.3)	–	–	–	–	INTC	INTD	INTA	INTB
Slot 4 (PCI 2.3)	–	–	–	–	INTB	INTC	INTD	INTA
PCI Express Mini Card	INTB	INTC	INTD	INTA	–	–	–	–
HDA audio controller	INTA	–	–	–	–	–	–	–
PCI Express root hub	INTA	INTB	INTC	INTD	–	–	–	–
Host to PCI Express graphics bridge	INTA	–	–	–	–	–	–	–
DMI to PCI bridge	–	–	–	INTA	INTB	–	–	–
Graphics controller 0	INTA	–	–	–	–	–	–	–
Graphics controller 1	INTA	–	–	–	–	–	–	–
USB UHCI controller 1	–	–	–	–	INTx	–	–	–
USB UHCI controller 2	–	–	–	–	INTx	–	–	–
USB UHCI controller 3	–	–	–	–	INTx	–	–	–
USB UHCI controller 4	–	–	–	–	INTx	–	–	–
USB EHCI controller	–	–	–	–	INTx	–	–	INTD
IDE controller, PCI to LPC bridge, SMBus controllers	–	–	INTA	INTB	INTC	–	–	–
Ethernet controller (Gbit)	–	–	INTA	–	–	–	–	–
Ethernet controller (10/100)	–	–	–	–	INTA	–	–	–
IEEE1394b controller	–	–	–	–	–	INTA	–	–

Example: From the previous table, the INTA interrupt from a card plugged into slot 3 would be routed to the motherboard PIRQG.

A.3 PCI Device Assignments

Table 32. PCI device assignments

Device	IDSEL	Bus Number	Device Number	Function Number
Host bridge and memory controller	–	0	0	0
Host to PCI Express graphics controller	–	0	1	0
Graphics controller 0	–	0	2	0
Graphics controller 1	–	0	2	1
HDA audio controller (if HDA is enabled)	–	0	27	0
AC97 Audio controller (if AC97 is enabled)	–	0	30	2
Slot 1 root (PCI-E 1)	–	0	28	0
Slot 2 root (PCI-E 2)	–	0	28	1
Gbit Ethernet root (PCI-E 3)	–	0	28	2
PCI Express Mini Card root (PCI-E 4)	–	0	28	3
USB UHCI controller 1	–	0	29	0
USB UHCI controller 2	–	0	29	1
USB UHCI controller 3	–	0	29	2
USB UHCI controller 3	–	0	29	3
USB EHCI controller	–	0	29	7
DMI to PCI bridge	–	0	30	0
LPC bridge (Includes DMA, timers, PIC, APIC, RTC, power & system management, GPIO)	–	0	31	0
PATA IDE controller	–	0	31	1
SATA IDE controller	–	0	31	2
SMBus controller	–	0	31	3
Slot 1 (PCI-E x1)	–	2	0	–
Slot 2 (PCI-E x1)	–	3	0	–
PCI Express Mini Card	–	4	0	–
Gbit Ethernet controller	–	5	0	–
Slot 3 (PCI 2.3)	AD18	6	2	–
Slot 4 (PCI 2.3)	AD19	6	3	–
10/100 Ethernet controller	AD24	6	8	0
IEEE1394b controller	AD25	6	9	0

A.4 SMBus Resource Allocation

Table 33. SMBus resource allocation

Address	Description
0101 110X	System management controller (LM85)
1010 000X	Memory module 1
1010 001X	Memory module 2
1101 001X	Clock synthesizer

A.5 ISA Interrupt Allocation

Whilst the motherboard does not include an ISA bus, it includes an ISA-compatible interrupt controller (PIC) in order to be compatible with AT standard architecture. The interrupts are allocated as described in the following table.

Table 34. ISA interrupt allocation

Interrupt	Description
IRQ0	System Timer
IRQ1	Not used
IRQ2	Cascade interrupt
IRQ3	Unassigned (pooled)
IRQ4	Unassigned (pooled)
IRQ5	Unassigned (pooled)
IRQ6	Unassigned (pooled)
IRQ7	Unassigned (pooled)
IRQ8	Real time clock/CMOS RAM
IRQ9	ACPI SCI (when configured for ACPI operating system, pooled)
IRQ10	Unassigned (pooled)
IRQ11	Unassigned (pooled)
IRQ12	Unassigned (pooled)
IRQ13	Floating point unit
IRQ14	Primary IDE or unassigned
IRQ15	Secondary IDE or unassigned
NMI	PCI PERR and SERR signals

A.6 ISA DMA Channel Allocation

Whilst the motherboard does not support an ISA bus, it includes an ISA-compatible DMA controller in order to be compatible with AT standard architecture. The DMA channels are allocated as described in the following table.

Table 35. ISA DMA channel allocation

DMA Channel	Description
Channel 0	Unassigned 8-bit channel
Channel 1	Unassigned 8-bit channel
Channel 2	Unassigned 8-bit channel
Channel 3	Unassigned 8-bit channel
Channel 4	Cascade channel
Channel 5	Unassigned 16-bit channel
Channel 6	Unassigned 16-bit channel
Channel 7	Unassigned 16-bit channel

B Control Logic and Registers

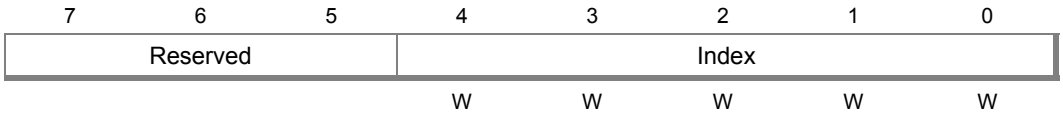
The control logic provides the following functions.

- Write-protection control for FWH and SD card
- Legacy keyboard and mouse emulation port
- Power LED, sleep state, power control

Notes:

- The following abbreviations are used in register descriptions:
  R=Read RO=Read only R/W=Read/Write W=Write only
- The MSB (Most Significant Bit) is listed first.

B.1 Index Register



I/O location: 062h
Default: None

Version — A read-only field containing the software version number for the logic.

0001	Version 1

Index — Value description.

00000	Watchdog Control
00000	Watchdog Kick
00000	Watchdog Status
00001	Watchdog Timeout Period
00010	General Purpose I/O Port 1
00011	General Purpose I/O Port 2 and Control
01000	PWM Control
01001	Part Number, low digits
01010	General Control and Status
01011	Part Number, high digits
01000	Write Enable Control 1
01001	Write Enable Control 2

B.2 Watchdog Control

7	6	5	4	3	2	1	0
Prescale				RES	SMI	WEN	0
W	W	W	W	W	W	W	W

I/O location: 066h
Index: 00h
Default: N/A

Prescale — 4-bit value to set the watchdog counter period

0..15	16..1s period (a value of 1010b gives a period of 6 seconds)
1	Description

RES — Reset after second timeout:

0	No reset
1	Force system reset after second watchdog timeout

SMI — Generate SMI after first timeout:[9]

0	No SMI
1	Generate SMI after first watchdog timeout

WEN — Watchdog enable:

0	Disable watchdog timer
1	Enable and start watchdog timer

B.3 Watchdog Kick

7	6	5	4	3	2	1	0
Don't care							1
W	W	W	W	W	W	W	W

I/O location: 066h
Index 00h
Default: N/A

[9] Use of this feature normally requires a custom BIOS – contact RadiSys for more information. The standard BIOS does not route the SMI and thus ignores the event – causing a system reset after the second timeout unless the timer is restarted.

B.4 Watchdog Status

7	6	5	4	3	2	1	0
Prescale				TO2	TO1	WEN	0
RO	RO	RO	RO	RO	RO	RO	RO

I/O location: 066h
Index: 00h
Default: 00000000b

Prescale — 4-bit value to set counter period (copy of data written)

TOC1 — First timeout:

- 0 — First timeout has not occurred
- 1 — Timer has expired at least once

TOC2 — Second timeout:

- 0 — Second timeout has not occurred
- 1 — Timer has expired at least once

WEN — Timer enable:

- 0 — Timer is disabled
- 1 — Timer is enabled and counting

B.5 Watchdog Timeout Period

7	6	5	4	3	2	1	0
Watchdog timeout period							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I/O location: 066h
Index 01h
Default: 11111111b

Timeout period

- 0 — Do not use (causes immediate timeout)
- 1–255 — Timeout period in units of 1 x prescale value seconds

B.6 General Purpose I/O Port 1

7	6	5	4	3	2	1	0
PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I/O location: 066h
Index: 02h
Default: 00000000b

P17–P10, GPIO Port 1 data:

When programmed as an output, the GPIO port 1 bit follows the value written into this register and reads reflect the value written.

When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 1 signal. Direction control is via the GPIO port 2 and control register.

B.7 General Purpose I/O Port 2 and Control

7	6	5	4	3	2	1	0
D201	D157	D104	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I/O location: 066h
Index: 03h
Default: 00000000b

P21 – P20, GPIO Port 2 data:

When programmed as an output, the GPIO port 2 bit follows the value written into this register and reads reflect the value written. When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 2 signal. Direction control is via the D201 control.

P22, GPIO Port 2 data:

This bit is output only. GPIO port 2 bit 2 follows the value written into this register and reads reflect the value written.

P24 - P23, GPIO Port 2 data:

These bits are input only. Writes to these bits have no effect, reads reflect the state of the GPIO port 2 bits 4 and 3 respectively.

D104, GPIO Port 1 bits 0 – 4 direction control:

GPIO bits 10 – 14 are inputs

GPIO bits 10 – 14 are outputs

D157, GPIO Port 1 bits 5 – 7 direction control:

GPIO bits 15 – 17 are inputs

GPIO bits 15 – 17 are outputs

D201, GPIO Port 2 bits 0 – 1 direction control:

GPIO bits 20 – 21 are inputs

GPIO bits 20 – 21 are outputs

B.8 PWM Control

7	6	5	4	3	2	1	0
Reserved					PWM control		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I/O location: 066h
Index: 08h
Default: 00000000b

PWM Control Determines the pulse width of the PWM output.

B.9 General Control and Status

7	6	5	4	3	2	1	0
EDE	LE	VID5	Reserved				
RW	RW	RO					

I/O location: 066h
Index: 0Ah
Default: 01*v*00000b

EDE EDID ROM Enable:

0 On-board LVDS EDID ROM is disabled

1 On-board LVDS EDID ROM is enabled (if fitted)

LE LAN Controller Enable:

0 Ethernet controller is disabled

1 Ethernet controller is enabled

VID5 Processor voltage ID bit 5 (selected by processor):

Returns the voltage identification VID5 value presented by the processor.

B.10 Write Enable Control 1

7	6	5	4	3	2	1	0
Reserved				WPT	WPU	WPL	Rsvd
RO	RO	RO	RO	RW	RW	RW	RO

I/O location: 066h
Index: 010h
Default: 00000000b

WPT Write Protect Top Block (0F0000h – 0FFFFFh):

0 Area is protected (writes are blocked)

1 Area is unblocked (writes are enabled)

WPU Write Protect Upper Sectors (080000h – 0EFFFFh):

	0	Area is protected (writes are blocked)
	1	Area is unblocked (writes are enabled)
WPL	Write Protect Lower Sectors (010000h – 07FFFFh):	
	0	Area is protected (writes are blocked)
	1	Area is unblocked (writes are enabled)

B.11 Write Enable Control 2

7	6	5	4	3	2	1	0
Reserved							WPB
RO	RO	RO	RO	RO	RO	RO	RW

I/O location: 066h
Index: 011h
Default: 00000000b

WPB	Write Protect Bottom Sector (000000h – 00FFFFh):	
	0	Area is protected (writes are blocked)
	1	Area is unblocked (writes are enabled)

B.12 Controller Part Number

The controller part number format is 082-0HHLL-000v where v is version number (top 4 bits of index register), HH is the high byte value and LL is the low byte value. BCD encoding is used for all digits.

The programmed part number is 082-02152-0v for production motherboards – HH is 21h, LL is 52h.

Controller Part Number, low digits

7	6	5	4	3	2	1	0
Part number, low byte							
RO	RO	RO	RO	RO	RO	RO	RO

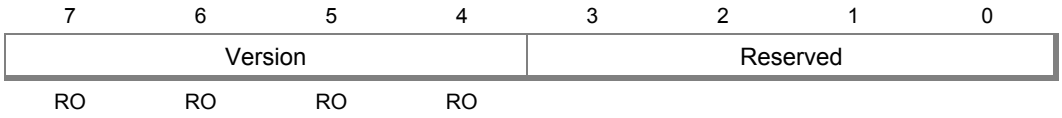
I/O location: 066h
Index: 09h
Default: N/A

Controller Part Number, high digits

7	6	5	4	3	2	1	0
Part number, high byte							
RO	RO	RO	RO	RO	RO	RO	RO

I/O location: 066h
Index: 0Bh
Default: N/A

B.13 Version Register



I/O location: 062h
Default: None

Version — A read-only field containing the software version number for the logic.

0000 Version 0

C Connector Descriptions

Refer to the motherboard layout diagram on page 11 for connector locations.

C.1 Connector Part Numbers

The various motherboard connectors are listed in the following table along with the part number of one of the approved vendors. The list is intended to assist in the selection of mating connectors.

Table 36. Connector part numbers

Connector	Part Number	Type
I/O panel quad USB	Foxconn UB11123-Q8-4F	Quad vertically stacked USB
I/O panel 10/100 RJ45	Bel 0826-1AX1-47-F	RJ45 with LEDs, 10/100
I/O panel Gbit RJ45	Bel 0826-1XX1-46-F	RJ45 with LEDs, Gbit
I/O panel DVI-I/DVI-D	Foxconn QH11121-EP1-4F	30-way right angle DVI-I
Fan drive headers	Foxconn HF0603E	3-way with locking ramp
Parallel ATA connector	Foxconn HL20201-D2	40-pin shrouded header
Serial ATA connector	Foxconn LD1807V-S01B	7-pin shrouded header
GPIO header	Foxconn HL20101-L7	2 by 10-way shrouded header
Processor socket	Foxconn PZ47913-2741-01	479-pin ZIF PGA, tool lock
SO-DIMM sockets	Foxconn AS0A426-MASN-7F	200-pin, 1.8V DDR2 SDRAM
PCI Express x1 connector, slots 1 and 2	Foxconn 2EG0181V-D2D	PCI Express x1 vertical
PCI connector, slots 3 and 4	Foxconn EH0600V-DAW	PCI 32-bit, 5V signaling
Front panel header	Foxconn HC1910V-L6	2 by 10-way header
ATAPI CD-ROM header	Foxconn HF1104E-P1	4-way header with latch, black
ATAPI Line input header	Foxconn HF1104E-NP1	4-way header with latch, white
ATAPI Line output header	Foxconn HF1104E-YP1	4-way header with latch, yellow
LVDS panel data	JAE FI-X30S-HF	30-pin 1mm flat cable
LVDS panel backlight control	Foxconn HS8207E	7-pin 1.25mm header
Double stack audio jacks	Foxconn JA23331-HA6Q-4F	Double vertically stacked 3.5mm, independent switches
Internal USB headers	Foxconn HF01051	5-pin locking ATAPI-style, black
Remote thermal sensor	Foxconn HF5502E	2-pin 2mm header
SMBus header	Foxconn HF5504E	4-pin 2mm header
Lithium cell holder	Renata VBH2032-1	Vertical loading, CR2032
Power Supply, main	Foxconn HM2010E-HP1	2 by 10-way ATX power header
SD Card slot	Foxconn WK22903-S6-4F	13-way horizontal loading
Mini PCI Express Card slot	Foxconn 2EG0181V-D2D	2x18-way horizontal 1mm

C.2 Expansion Slots

Table 37. PCI 2.2 Expansion slots

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST#[13]	B1	-12V	A32	AD16	B32	AD17
A2	+12V	B2	TCK[13]	A33	+3.3V	B33	C/BE2#
A3	TMS[14]	B3	GND	A34	FRAME#	B34	GND
A4	TDI[14]	B4	TDO[1]5	A35	GND	B35	IRDY#
A5	+5V	B5	+5V	A36	TRDY#	B36	+3.3V
A6	INTA#	B6	+5V	A37	GND	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	GND
A8	+5V	B8	INTD#	A39	+3.3V	B39	LOCK#
A9	CLKRUN#[15]	B9	PRSNT1#	A40	*Not Used*	B40	PERR#
A10	+5V	B10	*Reserved*	A41	*Not Used*	B41	+3.3V
A11	*Reserved*	B11	PRSNT2#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	+3.3V
A13	GND	B13	GND	A44	AD15	B44	C/BE1#
A14	+3.3V AUX	B14	*Reserved*	A45	+3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	+5V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PME#	B19	+5V	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	+3.3V	B21	AD29	A52	C/BE0#	B52	AD8
A22	AD28	B22	GND	A53	+3.3V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	+3.3V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	+3.3V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3#	A57	AD2	B57	GND
A27	+3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	+5V	B59	+5V
A29	AD20	B29	AD21	A660	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	+5V	B61	+5V
A31	AD18	B31	+3.3V	A62	+5V	B62	+5V

[13] Not used but pulled low

[14] Not used but pulled high to +5V

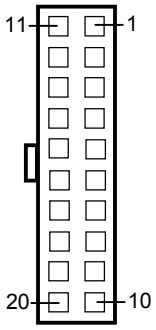
[15] Not connected

Table 38. PCI Express x1 Expansion Slots

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#	B10	+3.3Vaux	A10	+3.3V
B2	+12V	A2	+12V	B11	WAKE#	A11	PERST#
B3	Reserved	A3	+12V	B12	Reserved	A12	GND
B4	GND	A4	GND	B13	GND	A13	REFCLK+
B5	SMCLK	A5	JTAG2	B14	PETp0	A14	REFCLK-
B6	SMDAT	A6	JTAG3	B15	PETn0	A15	GND
B7	GND	A7	JTAG4	B16	GND	A16	PERp0
B8	+3.3V	A8	JTAG5	B17	PRSNT2#	A17	PERn0
B9	JTAG1	A9	+3.3V	B18	GND	A18	GND

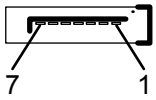
C.3 Connectors for Internal Devices

Table 39. Power Supply Connector (ATX)



Pin	Description	Pin	Description
11	+3.3V	1	+3.3V
12	–12.0V	2	+3.3V
13	GND	3	GND
14	PS_ON#	4	+5.0V
15	GND	5	GND
16	GND	6	+5.0V
17	GND	7	GND
18	*Not Used*	8	PWR_OK
19	+5.0V	9	+5.0VSBY
20	+5.0V	10	+12.0V

Table 40. SATA Connectors



Pin	Description	Pin	Description
1	GND	5	B-
2	A+	6	B+
3	A-	7	GND
4	GND		

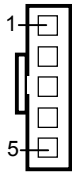
Table 41. LVDS Data Connector

Pin	Description	Pin	Description
1	GND	16	SHIELD
2	+3.3V	17	CLKAM
3	+3.3V	18	CLKAP
4	+3.3V	19	SHIELD
5	*Not Used*	20	B0M
6	DDCCLK	21	B0P
7	DDCDATA	22	SHIELD
8	A0M	23	B1M
9	A0P	24	B1P
10	SHIELD	25	SHIELD
11	A1M	26	B2M
12	A1P	27	B2P
13	SHIELD	28	SHIELD
14	A2M	29	CLKBM
15	A2P	30	CLKBP

Table 42. LVDS Backlight Control Connector

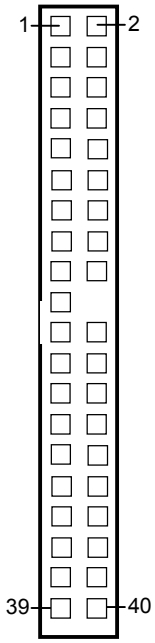
Pin	Description	Pin	Description
1	Inverter Power, +12V	5	CLK
2	GND	6	DATA/PWM Control
3	GND	7	ENABLE
4	+5V		

Table 43. USB Internal Ports



Pin	Description	Pin	Description
1	+5V	4	GND
2	DATA-	5	GND
3	DATA+		

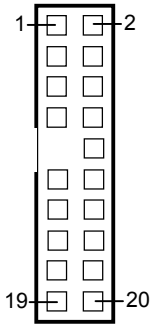
Table 44. IDE Header (PATA)



Pin	Description	Pin	Description
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	DRQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	CSEL
29	DAK#	30	GND
31	IRQ[17]	32	*Not Used*
33	DA1	34	CBLID#
35	DA0	36	DA2
37	CS1#	38	CS3#
39	HDACT#	40	GND

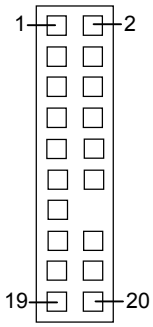
[17] IRQ14 for Primary, IRQ15 for Secondary

Table 45. GPIO Header



Pin	Description	Pin	Description
1	GND	2	+5V fused
3	PWM	4	GPIO20
5	GPIO21	6	GPO22
7	GPIO10	8	GPIO11
9	GPIO12	10	GPIO13
11	GPIO14	12	GPIO15
13	GPIO16	14	GPIO17
15	*Reserved*	16	KEY
17	GND	18	GPI23
19	GND	20	GPI24

Table 46. Front Panel Header

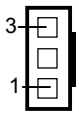


Pin	Description	Pin	Description
1	HDLED+	2	GREENLED+
3	HDLED-	4	GREENLED-
5	RESETSW-	6	PWRSW+
7	RESETSW+	8	PWRSW-
9	+5V fused	10	SPKR+
11	*Not Used*	12	SPKR-
13	GND	14	KEY
15	GREENLED+	16	SPKR-
17	*Not Used*	18	TMPSW+
19	GREENLED-	20	TMPSW-

Table 47. Audio Line Input and Output Headers

Pin	Description	Pin	Description
1	LEFT	3	GND
2	GND	4	RIGHT

Table 48. Processor and System Fan (1 & 2) Power Connectors



Pin	Description	Pin	Description
1	GND	3	TACH#
2	POWER		

Table 49. Remote Thermal Sensor

Pin	Description	Pin	Description
	DIODE+		DIODE-

Table 50. SMBus Header

Pin	Description	Pin	Description
1	+3.3V	3	CLOCK
2	DATA	4	GND

C.4 External Device Ports

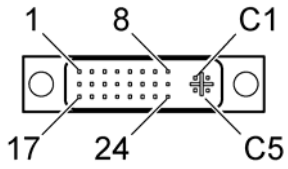


Table 51. DVI-I Connector[10]

Pin	Description	Pin	Description
1	DATA2-	13	*Not Used*
2	DATA2+	14	+5V (fused)
3	DATA2SHLD	15	GND
4	*Not Used*	16	HPD (Hot Plug Detect)
5	*Not Used*	17	DATA0-
6	DDCCLK	18	DATA0+
7	DDCDATA	19	DATA0SHLD
8	ASYNC	20	*Not Used*
9	DATA1-	21	*Not Used*
10	DATA1+	22	CLOCKSHLD
11	DATA1SHLD	23	CLOCK+
12	*Not Used*	24	CLOCK-
C1	RED	C4	HSYNC
C2	GREEN	C5	AGND
C3	BLUE		

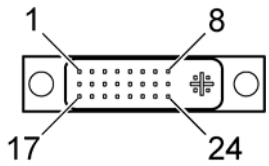
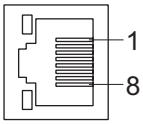


Table 52. DVI-D Connector

Pin	Description	Pin	Description
1	DATA2-	13	*Not Used*
2	DATA2+	14	+5V (fused)
3	DATA2SHLD	15	GND
4	*Not Used*	16	HPD (Hot Plug Detect)
5	*Not Used*	17	DATA0-
6	DDCCLK	18	DATA0+
7	DDCDATA	19	DATA0SHLD
8	ASYNC	20	*Not Used*
9	DATA1-	21	*Not Used*
10	DATA1+	22	CLOCKSHLD
11	DATA1SHLD	23	CLOCK+
12	*Not Used*	24	CLOCK-
C1	*Not Used*	C4	*Not Used*
C2	*Not Used*	C5	*Not Used*
C3	*Not Used*		

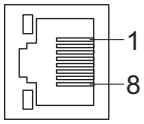
[10] Digital signals not supported for products with single DVI interface

Table 53. RJ45 Ethernet (10/100)



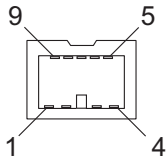
Pin	Description	Pin	Description
1	TxD+	5	75Ω AC termination
2	TxD-	6	RxD-
3	RxD+	7	75Ω AC termination
4	75Ω AC termination	8	75Ω AC termination

Table 54. RJ45 Ethernet (Gbit)



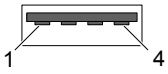
Pin	Description	Pin	Description
1	A+	5	C-
2	A-	6	B-
3	B+	7	D+
4	C+	8	D-

Table 55. IEEE 1394b



Pin	Description	Pin	Description
1	TPB1-	6	GND
2	TPB1+	7	*Not Used*
3	TPA1-	8	+12V (fused)
4	TPA1+	9	GND
5	SHLD		

Table 56. USB 2.0 Ports



Pin	Description	Pin	Description
1	+5V	3	DATA+
2	DATA-	4	GND

Table 57. Audio Line Output Jack

Pin	Description	Pin	Description
TIP	LEFT	SLEEVE	GND
RING	RIGHT		

Table 58. Audio Microphone Input Jack

Pin	Description	Pin	Description
TIP	MIC MONO INPUT	SLEEVE	GND
RING	BIAS VOLTAGE		