



SCSI/

FSSCSIA Users Manual

For use with Hewlett-Packard Logic Analyzers

Revision 1.0

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Setting Up the FSSCSIA

Introduction

This section explains how to install and configure the FSSCSIA Preprocessor Interface to perform measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the FSSCSIA software, make a duplicate copy of the FSSCSIA master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The FSSCSIA SCSI Bus Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The inverse assembler software on a 3.5-inch disk.
- This user's manual.

Equipment Required

The minimum equipment required for SCSI Bus analysis consists of the following items:

- An HP 1650A (with memory upgrade), HP 1650B, HP 1652B, HP 166X, HP 167X, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 1655X.
- The FSSCSIA Preprocessor Interface and Inverse Assembler.
- An additional cable to connect the FSSCSIA to your SCSI bus system (see pages 2 and 3).

Setting Up the FSSCSIA Front Panel

The FSSCSIA has three switches on the front panel:

Bus Type. Allows the user to test either a Single-Ended or a Differential Bus system. This switch setting must match the type of SCSI bus you are currently monitoring.

Bus Size. Allows the user to select either 8-bit or 16-bit bus size.

State Parity Check. The use of the parity bit is not mandatory on a SCSI bus system. This switch allows the user to switch off the parity check.

Note

Excessive parity errors may appear on screen if parity is on with a system that does not use parity.

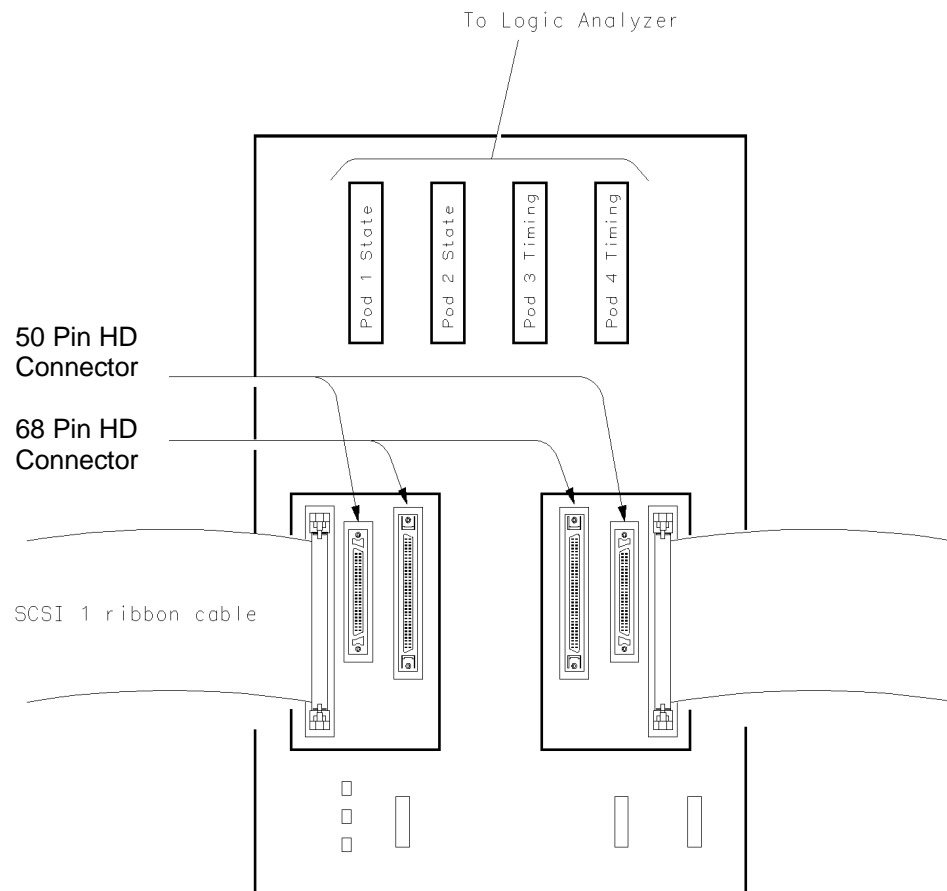


Figure 1-1. FSSCSIA Preprocessor Interface

Connecting the FSSCSIA to the SCSI Bus

The connectors on the FSSCSIA are tied in parallel so that all the connectors and cable combinations can be used with a Single-Ended or Differential. Also, there are always four connectors that are not used. These connectors may be used for additional analysis with an oscilloscope or other measurement device.

Figure 1-1 shows the connectors on the SCSI Preprocessor Interface. There are three types of connectors on the front panel:

- Two 68-pin D-Shell shielded high-density type;
- Two 50-pin D-Shell shielded high-density type; and
- Two 50-pin (25-pin dual row, 0.1" spacing) nonshielded connectors (see Caution on next page).

You will always need at least one additional cable or terminator to connect the FSSCSIA to your SCSI bus system.

The following section provides instructions for connecting the cables to the SCSI bus and the FSSCSIA Preprocessor Interface.

To connect the FSSCSIA to the bus, daisy chain the connectors so both of the matching connectors are used together (see figure 1-2). This is accomplished by the following steps:

- 1) Turn off the power to the bus system and logic analyzer.
- 2) Disconnect one end of a cable from the bus system and connect it to one of the connectors on the FSSCSIA.
- 3) Connect the optional or custom cable from the matching connector on the FSSCSIA to your bus system.
- 4) Turn on the bus and logic analyzer.

You can also connect the FSSCSIA to either end of your SCSI bus system. Remove the termination device from one end of the SCSI bus, and use the appropriate cable to connect the FSSCSIA to the SCSI bus. Connect the termination device to the matching connector on the opposite side of the FSSCSIA board.

Caution

Some 50-pin ribbon cables have a connector clamped in the center of the cable for connecting devices to the SCSI bus with only a single connection. Do not use a center connector to connect the FSSCSIA to the SCSI bus. Since the circuitry of the FSSCSIA is part of the transmission line for the SCSI bus, a center connector will cause stub-length violations and the SCSI bus might not operate properly. You should always have a cable or termination device on both of the matching connectors on the FSSCSIA.

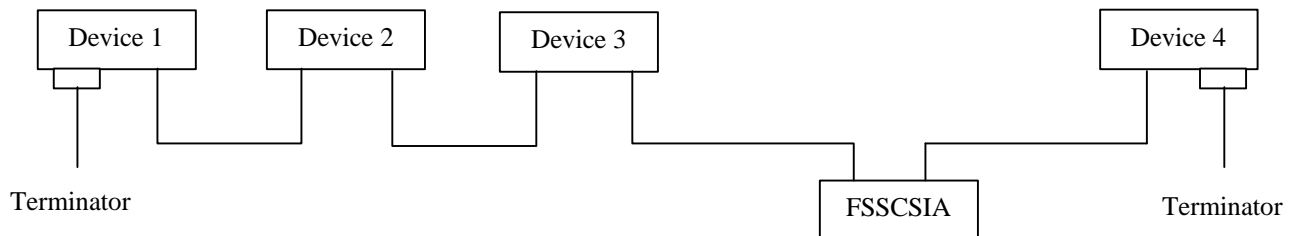


Figure 1-2. Connecting to the SCSI

Connecting to the FSSCSIA

Connect the logic analyzer probes to the cable connectors as listed in Table 1-1. The column heads refer to the logic analyzer pods, while designations such as P1 refer to a connector on the preprocessor interface.

Figure 1-3 shows the relative locations of the logic analyzer cards.

Note

HP 16542A with three or four Expansion Cards

The locations for the HP 16542A expansion cards, relative to the Master Card, depend on the number of expansion cards used. If one or two expansion cards are used, Card 1 is located above the Master Card and Card 2 is located below the Master Card. If three expansion cards are used, two of them are located above the Master Card and the third is located below the Master Card. When four expansion cards are used, they are located as shown in Figure 1-3.

Table 1-1 shows the physical location and connections for a one-expansion-card system.

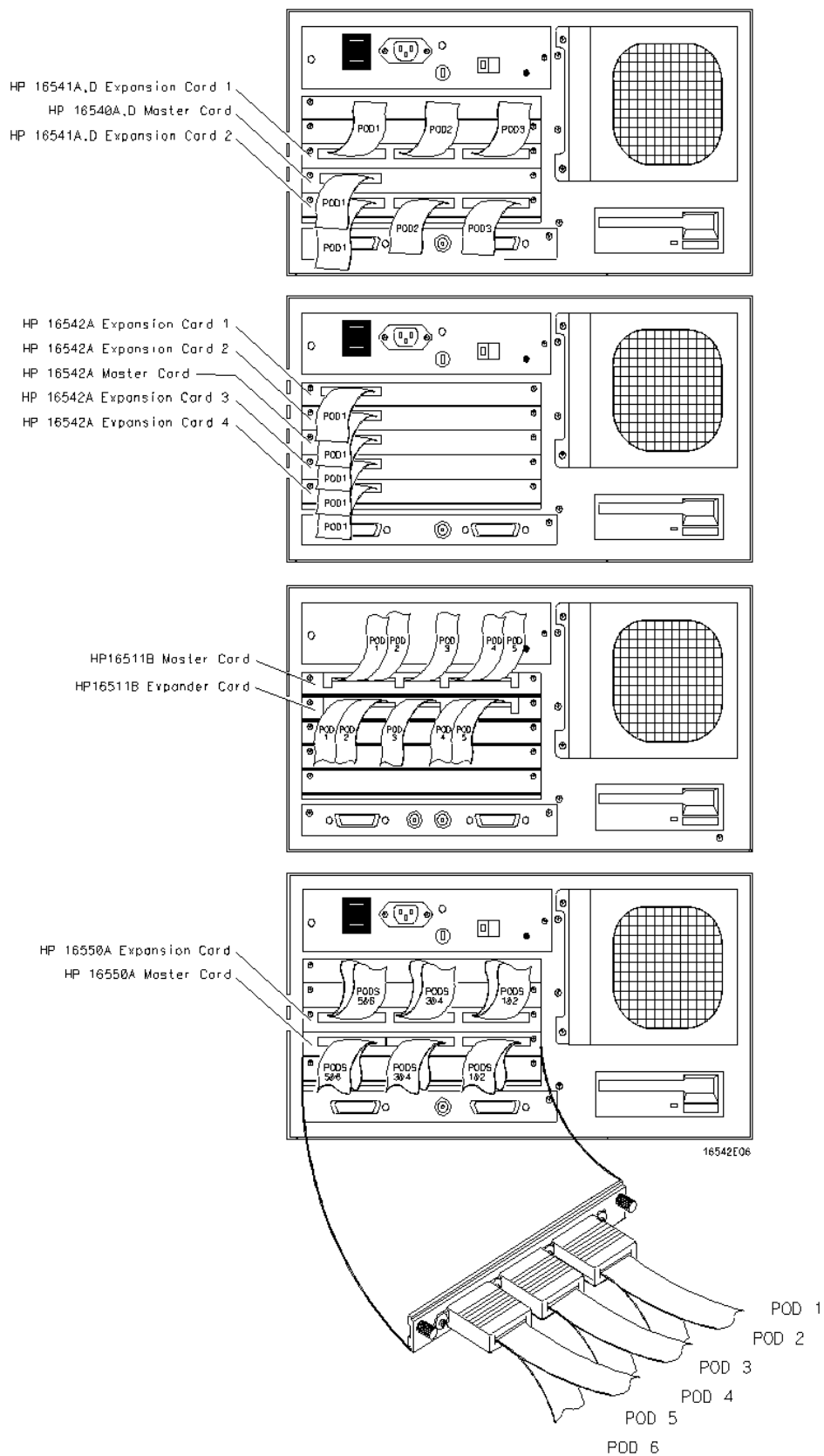


Figure 1-3. Logic Analyzer Card Locations
 (relative locations, actual slots used may vary)

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

Table 1-1. Logic Analyzer Connections and Configuration Files

(HP 1650 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A, HP 1660X Series, HP 16555X Series)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A/B, HP1652B, HP16510A/B	CSCSI2 state, timing		--	P4 Timing DATA	P3 Timing STAT	P2 State DATA	P1 State STAT Clk ↓
HP 16511B Upper Card	DSCSI2 state, timing		--	--	--	P2 State DATA	P1 State STAT Clk ↓
HP 16511B Lower Card			--	--	--	P4 Timing DATA	P3 Timing STAT
HP 16541A,D Exp. Card 1	ESCSI2ST state ESCSI2TM timing				P4 Timing DATA	P3 Timing STAT	P2 State DATA
HP 16540A,D Master Card							P1 State STAT Clk ↓
HP 16550A HP 1660X HP 1661X	FSCSI2 state, timing ½channel	P4 Timing DATA	P3 Timing STAT		P2 State DATA		P1 State STAT Clk ↓
HP 1662X	GSCSI2 state, timing			P4 Timing DATA	P3 Timing STAT	P2 State DATA	P1 State STAT Clk ↓
HP 1663X	GSCSI2 (state only)					P2 State DATA	P1 State STAT Clk ↓
HP 16555X HP 16554X HP 16556X	HSCSI2 state, timing			P4 Timing DATA	P3 Timing STAT	P2 State DATA	P1 State STAT Clk ↓

Table 1-1. Logic Analyzer Connections and Configuration Files

(HP 1670X series, HP 16542A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Exp. Card 1	ESCSI2ST state						P2 State DATA
HP 16542A Master Card							P1 State STAT Clk ↓
HP 16542A Exp. Card 1	ESCSI2TM timing						P4 Timing DATA
HP 16542A Master Card							P3 Timing STAT
HP 1670X HP 1671X HP 1672X	HSCSI2 state, timing			P4 Timing DATA	P3 Timing STAT	P2 State DATA	P1 State STAT Clk ↓

Setting Up the Analyzer from the Disk

The logic analyzer is configured for SCSI bus analysis by loading the appropriate configuration file. The configuration files also load the inverse assembler "ISCSIDIR." You can then load a different inverse assembler from the list in Table 1-2.

For all logic analyzers except the HP 16540/16541A,D and HP 16542A, the same configuration file is used for state or timing analysis. For the HP 16540/16541A,D and HP 16542A, separate configuration files are provided for state and timing. To load the files:

- 1) Install the FSSCSIA disk in the logic analyzer front disk drive.
- 2) Select one of the following menus:
- 3) For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
- 4) For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk or Flexible Disk menu.
- 5) Configure the menu to "Load" the analyzer configuration from disk.
- 6) For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
- 7) Use the knob to select the appropriate configuration file (see Table 1-1).
- 8) Execute the load operation to load the file into the logic analyzer.

Caution

DO NOT Autoscale the timing analyzer. The Autoscale operation will destroy the previously loaded configuration. The only way to recover the configuration after Autoscale is to reload it from the disk.

Loading an Inverse Assembler

The following section describes the different inverse assemblers available with the FSSCSIA. To load a different inverse after loading the configuration file:

- 1) Install the FSSCSIA disk in the front disk drive of the logic analyzer.
- 2) Select one of the following menus:
- 3) For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
- 4) For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk or Flexible Disk menu.
- 5) Configure the menu to "Load" the inverse assembler from disk.
- 6) For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
- 7) Use the knob to select the appropriate inverse assembler (see Table 1-2, next page).
- 8) Execute the load operation to load the file into the logic analyzer.

Note

To properly load the FSSCSIA inverse assemblers, Analyzer 1 of the logic analyzer must be on and configured as a State machine. If Analyzer 1 and 2 are on and configured as State machines, a field will appear on screen to allow you to select which analyzer to load the inverse assembler into. Load the FSSCSIA inverse assembler into Analyzer 1.

Selecting the Correct Inverse Assembler

The FSSCSIA has seven inverse assemblers available for SCSI Bus system analysis. The interpretation of the SCSI command set varies in each inverse assembler to match the applications of various device types. Only one inverse assembler can be used at a time. Table 1-2 lists the different inverse assemblers and the devices which are generally supported by the command sets.

There is a good possibility that your SCSI Bus system will be made up of several different device types, and each device type will interpret the commands differently. For example, a disk drive connected to a communication device contains two different device types. In this situation you may need to decide which inverse assembler will best fit your needs. To make it easier to select the appropriate inverse assembler, the commands for each device type are listed in Tables 1-3 through 1-9. By comparing the commands for each inverse assembler, the most appropriate inverse assembler can be selected. The commands which are common to all devices are listed in normal type, and the commands which vary from device to device are listed in bold type.

Note

A different inverse assembler can be loaded into the logic analyzer without losing the accumulated data.

Table 1-2. Inverse Assemblers

Inverse Assembler	Devices Supported
ISCSIDIR	Direct Devices, Write Once Read Multiple Devices, and Optical Devices
ISCSISEQ	Sequential Devices like tape backup drives, and Scanner Devices
ISCSIPTR	Printers
ISCSIPRC	Processor Devices
ISCSIDSE	A special application which is used when there is Sequential Access Device on the SCSI Bus that uses Group 0 (6 byte) commands which communicates with a Direct Access Device that uses Group 1 (10 byte) commands
ISCSIAMC	Automatic Media Changers, and Communication Devices
ISCSICDR	CD ROMs

Table 1-3. ISCSIDIR Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rezero	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	A9	Play Track
05	Read Block Limits	2A	Write	44	Read Header	AA	Write
07	Reassign Block	2B	Seek	45	Play Audio	AC	Erase
08	Read	2C	Erase	47	Play Audio MSF	AE	Write and Verify
0A	Write	2D	Read Update	48	Play Audio Track	AF	Verify
0B	Seek		Block		Index	B0	Search High
0F	Read Reverse	2E	Write and Verify	49	Play Audio Track	B1	Search Equal
10	Write Filemarks	2F	Verify		Relative	B2	Search Low
11	Space	30	Search High	4B	Pause/Resume	B3	Set Limits
12	Inquiry	31	Search =	4C	Log Select	B5	Request Volume
13	Verify	32	Search Low	4D	Log Sense		Element Address
14	Recovered Buffer	33	Set Limits	55	Mode Select	B6	Send Volume Tag
15	Mode Select	34	Pre-Fetch	5A	Mode Sense	B7	Read Defect Data
16	Reserve	35	Flush Cache			B8	Read Element
17	Release	36	Lock/Unlock				Status
18	Copy		Cache				
19	Erase	37	Read Defect Data				
1A	Mode Sense	38	Media Scan				
1B	Start/Stop Unit	39	Compare				
1C	Receive	3A	Copy and Verify				
	Diagnostics	3B	Write Buffer				
1D	Send Diagnostics	3C	Read Buffer				
1E	Prevent/Allow	3D	Update Block				
	Removal	3E	Read Long				
1F	Read Log	3F	Write Long				

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-4. ISCSISEQ Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rewind	25	Get Window	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	AA	Write
05	Read Block Limits	2A	Send	44	Read Header	AC	Erase
07	Reassign Block	2B	Locate	45	Play Audio	AE	Write and Verify
08	Read	2C	Erase	47	Play Audio MSF	AF	Verify
0A	Write	2D	Read Update	48	Play Audio Track	B0	Search High
0B	Seek		Block		Index	B1	Search Equal
0F	Read Reverse	2E	Write and Verify	49	Play Audio Track	B2	Search Low
10	Write Filemarks	2F	Verify		Relative	B3	Set Limits
11	Space	30	Search High	4B	Pause/Resume	B5	Request Volume
12	Inquiry	31	Object Position	4C	Log Select		Element Address
13	Verify	32	Search Low	4D	Log Sense	B6	Send Volume Tag
14	Recovered Buffer	33	Set Limits	55	Mode Select	B7	Read Defect Data
15	Mode Select	34	Read Position/ Get Buffer	5A	Mode Sense	B8	Read Element
16	Reserve Unit	35	Flush Cache				Status
17	Release Unit	36	Lock/Unlock				
18	Copy		Cache				
19	Erase	37	Read Defect Data				
1A	Mode Sense	38	Media Scan				
1B	Load/Unload	39	Compare				
1C	Receive	3A	Copy and Verify				
	Diagnostics	3B	Write Buffer				
1D	Send Diagnostics	3C	Read Buffer				
1E	Prevent/Allow	3D	Update Block				
	Removal	3E	Read Long				
1F	Read Log	3F	Write Long				

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-5. ISCSIPTR Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rezero	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	AA	Write
05	Read Block Limits	2A	Write	44	Read Header	AC	Erase
07	Reassign Block	2B	Seek	45	Play Audio	AE	Write and Verify
08	Read	2C	Erase	47	Play Audio MSF	AF	Verify
0A	Print	2D	Read Update Block	48	Play Audio Track Index	B0	Search High
0B	Slew and Print	2E	Write and Verify	49	Play Audio Track Relative	B1	Search Equal
0F	Read Reverse	2F	Verify	4B	Pause/Resume	B2	Search Low
10	Sync Buffer	30	Search High	4C	Log Select	B3	Set Limits
11	Space	31	Search =	4D	Log Sense	B5	Request Volume Element Address
12	Inquiry	32	Search Low	55	Mode Select	B6	Send Volume Tag
13	Verify	33	Set Limits	5A	Mode Sense	B7	Read Defect Data
14	Recover Buffer Data	34	Pre-Fetch			B8	Read Element Status
15	Mode Select	35	Flush Cache				
16	Reserve	36	Lock/Unlock Cache				
17	Release	37	Read Defect Data				
18	Copy	38	Media Scan				
19	Erase	39	Compare				
1A	Mode Sense	3A	Copy and Verify				
1B	Stop Print	3B	Write Buffer				
1C	Receive	3C	Read Buffer				
	Diagnostics	3D	Update Block				
1D	Send Diagnostics	3E	Read Long				
1E	Prevent/Allow Removal	3F	Write Long				
1F	Read Log						

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-6. ISCSIPRC Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rezero	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	AA	Write
05	Read Block Limits	2A	Write	44	Read Header	AC	Erase
07	Reassign Block	2B	Seek	45	Play Audio	AE	Write and Verify
08	Receive	2C	Erase	47	Play Audio MSF	AF	Verify
0A	Send	2D	Read Update Block	48	Play Audio Track Index	B0	Search High
0B	Seek	2E	Write and Verify	49	Play Audio Track Relative	B1	Search Equal
0F	Read Reverse	2F	Verify	4B	Pause/Resume	B2	Search Low
10	Write Filemarks	30	Search High	4C	Log Select	B3	Set Limits
11	Space	31	Search =	4D	Log Sense	B5	Request Volume Element Address
12	Inquiry	32	Search Low	55	Mode Select	B6	Send Volume Tag
13	Verify	33	Set Limits	5A	Mode Sense	B7	Read Defect Data
14	Recovered Buffer	34	Pre-Fetch			B8	Read Element Status
15	Mode Select	35	Flush Cache				
16	Reserve	36	Lock/Unlock Cache				
17	Release	37	Read Defect Data				
18	Copy	38	Media Scan				
19	Erase	39	Compare				
1A	Mode Sense	3A	Copy and Verify				
1B	Start/Stop	3B	Write Buffer				
1C	Receive	3C	Read Buffer				
	Diagnostics	3D	Update Block				
1D	Send Diagnostics	3E	Read Long				
1E	Prevent/Allow Removal	3F	Write Long				
1F	Read Log						

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-7. ISCSIDSE Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rewind	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	A9	Play Track
05	Read Block Limits	2A	Write	44	Read Header	AA	Write
07	Reassign Block	2B	Seek	45	Play Audio	AC	Erase
08	Read	2C	Erase	47	Play Audio MSF	AE	Write and Verify
0A	Write	2D	Read Update	48	Play Audio Track	AF	Verify
0B	Seek		Block		Index	B0	Search High
0F	Read Reverse	2E	Write and Verify	49	Play Audio Track	B1	Search Equal
10	Write Filemarks	2F	Verify		Relative	B2	Search Low
11	Space	30	Search High	4B	Pause/Resume	B3	Set Limits
12	Inquiry	31	Search =	4C	Log Select	B5	Request Volume
13	Verify	32	Search Low	4D	Log Sense		Element Address
14	Recovered Buffer	33	Set Limits	55	Mode Select	B6	Send Volume Tag
15	Mode Select	34	Pre-Fetch	5A	Mode Sense	B7	Read Defect Data
16	Reserve Unit	35	Flush Cache			B8	Read Element
17	Release Unit	36	Lock/Unlock				Status
18	Copy		Cache				
19	Erase	37	Read Defect Data				
1A	Mode Sense	38	Media Scan				
1B	Load/Unload	39	Compare				
1C	Receive	3A	Copy and Verify				
	Diagnostics	3B	Write Buffer				
1D	Send Diagnostics	3C	Read Buffer				
1E	Prevent/Allow	3D	Update Block				
	Removal	3E	Read Long				
1F	Read Log	3F	Write Long				

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-8. ISCSIAMC Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Move Medium
01	Rezero	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Get Message	42	Read Sub-Channel	A8	Get Message
04	Format Unit	29	Read Generation	43	Read TOC	AA	Send Message
05	Read Block Limits	2A	Send Message	44	Read Header	AC	Erase
07	Initialize Element Status	2B	Position to Element	45	Play Audio	AE	Write and Verify
08	Read	2C	Erase	47	Play Audio MSF	AF	Verify
0A	Write	2D	Read Update	48	Play Audio Track	B0	Search High
0B	Seek		Block		Index	B1	Search Equal
0F	Read Reverse	2E	Write and Verify	49	Play Audio Track	B2	Search Low
10	Write Filemarks	2F	Verify		Relative	B3	Set Limits
11	Space	30	Search High	4B	Pause/Resume	B5	Request Volume
12	Inquiry	31	Search Equal	4C	Log Select		Element Address
13	Verify	32	Search Low	4D	Log Sense	B6	Send Volume Tag
14	Recovered Buffer	33	Set Limits	55	Mode Select	B7	Read Defect Data
15	Mode Select	34	Pre-Fetch	5A	Mode Sense	B8	Read Element
16	Reserve	35	Flush Cache				Status
17	Release	36	Lock/Unlock				
18	Copy		Cache				
19	Erase	37	Read Defect Data				
1A	Mode Sense	38	Media Scan				
1B	Start/Stop	39	Compare				
1C	Receive	3A	Copy and Verify				
	Diagnostics	3B	Write Buffer				
1D	Send Diagnostics	3C	Read Buffer				
1E	Prevent/Allow	3D	Update Block				
	Removal	3E	Read Long				
1F	Read Log	3F	Write Long				

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

Table 1-9. ISCSICDR Commands

Group 0 Commands (6 byte)		Group 1 Commands (10 byte)		Group 2 Commands (10 byte)		Group 5 Commands (12 byte)	
00	Test Unit Ready	24	Set Window	40	Change Definition	A5	Play Audio
01	Rezero	25	Read Capacity	41	Write Same	A6	Exchange Medium
03	Request Sense	28	Read	42	Read Sub-Channel	A8	Read
04	Format Unit	29	Read Generation	43	Read TOC	AA	Write
05	Read Block Limits	2A	Write	44	Read Header	AC	Erase
07	Reassign Block	2B	Seek X	45	Play Audio	AE	Write and Verify
08	Read	2C	Erase	47	Play Audio MSF	AF	Verify
0A	Write	2D	Read Update	48	Play Audio Track	B0	Search High
0B	Seek		Block		Index	B1	Search Equal
0F	Read Reverse	2E	Write and Verify	49	Play Audio Track	B2	Search Low
10	Write Filemarks	2F	Verify		Relative	B3	Set Limits
11	Space	30	Search High	4B	Pause/Resume	B5	Request Volume
12	Inquiry	31	Search =	4C	Log Select		Element Address
13	Verify	32	Search Low	4D	Log Sense	B6	Send Volume Tag
14	Recovered Buffer	33	Set Limits	55	Mode Select	B7	Read Defect Data
15	Mode Select	34	Pre-Fetch	5A	Mode Sense	B8	Read Element
16	Reserve	35	Flush Cache				Status
17	Release	36	Lock/Unlock				
18	Copy		Cache				
19	Erase	37	Read Defect Data				
1A	Mode Sense	38	Media Scan				
1B	Start/Stop	39	Compare				
1C	Receive	3A	Copy and Verify				
	Diagnostics	3B	Write Buffer				
1D	Send Diagnostics	3C	Read Buffer				
1E	Prevent/Allow	3D	Update Block				
	Removal	3E	Read Long				
1F	Read Log	3F	Write Long				

The commands in **bold** type vary from device to device; the commands in normal type are common to all devices.

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Analyzing the SCSI Bus

Introduction

This section provides reference information on the format specification and symbols configured by the FSSCSIA software. It also provides information about the inverse assemblers and LED indicators.

Format Specification

The FSSCSIA software sets up format specifications for the logic analyzer. There will be some slight differences in the displays, according to which logic analyzer you are using. For example, some of the logic analyzers do not have a Clock Period field.

The ADDR, DATA_, and DATA labels all contain the same information. The ADDR field is required by the inverse assembler software, but the information is not applicable for SCSI bus analysis. The DATA_ field shows the data in hexadecimal format in the Listing menu. The DATA field is decoded and shows the instruction in SCSI mnemonics.

The following section lists the SCSI bus signals for the FSSCSIA and their corresponding lines to the logic analyzer.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (>60 ns) since the SCSI bus has bus cycle periods greater than 60 ns. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Symbols and Labels

The configuration file sets up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns.

Table 2-1 lists the bits assigned to the STAT and BUSIZE labels. Table 2-2 lists the symbols for the STAT label. Table 2-3 lists the symbols for the PHASE label.

Table 2-1. STAT Label and BUSIZE Label Bits

Bit	Signal	Description
0	I/O	This signal is true when data flows to the initiator and false when data flows to the target.
1	C/D	This signal is true when not in the data phase and false when in the data phase.
2	MSG	This signal is true when in the message phase and false when not in the message phase.
3	SEL	This signal is true during selection of target device.
4	BSY	This signal is true when the bus is in use and false when the bus is free or during selection of target device.
5	REQ	This signal is a handshake driven by the target device.
6	ACK	This signal is a handshake driven by the initiator.
7	ATN	This signal is used by the initiator to request an output phase.
8	RST	A true signal resets all devices on the bus.
9	LBUSPT	DBP Low byte bus parity bit (odd).
10	HBUSPT	DBP1 High byte bus parity bit (odd).
11	LPTYER	DBP Error. This bit is true when there is a low byte parity error.
12	HPTYER	DBP1 Error. This bit is true when there is a high byte parity error.
15 (BUSIZE Label)	BUSIZE	This bit sends the position of the Bus Size switch on the FSSCSIA front panel.

Table 2-2. STAT Symbols

Symbol	Pattern	
RST BUS FREE	X X X X 1	X X X 0 0 X X X
RESET	X X X X 1	X X X X X X X X
BUS FREE	X X X X 0	X X X 0 0 X X X
ARBITRATION	X X X X 0	0 0 0 1 1 0 0 0
ATTEN ARBIT	X X X X 0	1 0 0 1 1 X X X
HL_PTY ERROR	1 1 X X 0	X X X X X X X X
L_PTY ERROR	0 1 X X 0	X X X X X X X X
H_PTY ERROR	1 0 X X 0	X X X X X X X X
SELECT	X X X X 0	X 0 0 0 1 X X 0
RESELECT	X X X X 0	X 0 0 0 1 X X 1
DATA OUT	X X X X 0	X X X 1 0 0 0 0
DATA IN	X X X X 0	X X X 1 0 0 0 1
COMMAND	X X X X 0	X X X 1 0 0 1 0
STATUS	X X X X 0	X X X 1 0 0 1 1
MSG OUT	X X X X 0	X X X 1 0 1 1 0
MSG IN	X X X X 0	X X X 1 0 1 1 1
DATA XFR	X X X X X	0 X X X 1 0 0 X

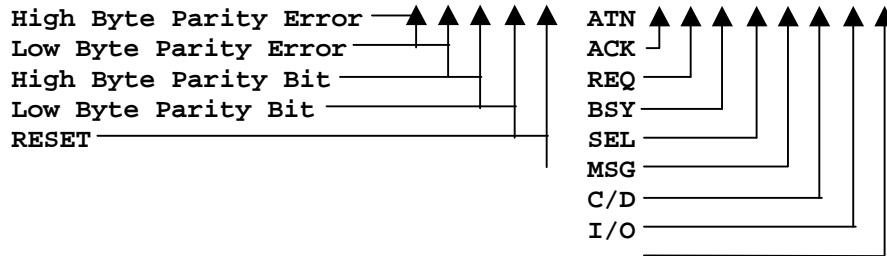
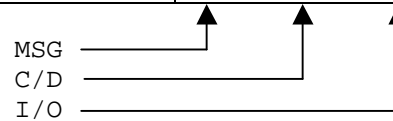


Table 2-3. Phase Symbols

Symbol	Pattern		
DATA OUT	0	0	0
DATA IN	0	0	1
COMMAND	0	1	0
STAT	0	1	1
PHASE 4	1	0	0
PHASE 5	1	0	1
MSG OUT	1	1	0
MSG IN	1	1	1



Accumulating Data

Touch RUN, and as soon as there is activity on the bus the logic analyzer will begin to accumulate data. The logic analyzer will continue to accumulate data and will display the data when the logic analyzer memory is full or when you touch STOP.

Note

The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus.

Listing Menu

Captured data is displayed as shown in Figure 2-1. Additional labels may be viewed by rolling the display. The inverse assemblers are constructed so that the output lists the actual commands, status conditions, messages, and phases of the SCSI bus. The DATA_ label lists the data in hexadecimal format, and the DATA label lists the instructions in SCSI mnemonics.

100/500MHz LA C		Listing 1		Cancel		Run	
Markers Off		Acquisition Time 10 Dec 1997 15:51:28					
Label>	DATA_	FUTUREPLUS SYSTEMS c 1997				PH	
Base>	Hex	Phase	SCSI mnemonic			Sy	
0	0018	Arbitrate	ID=04			DA	
1	0298	Select	Atn ID=07			DA	
2	0296	Msgout	Atn Identify No Disconnect Logical=6			MS	
3	0096	Msgout	Atn Identify No Disconnect Logical=6			MS	
4	0016	Msgout	Reserved			MS	
5	0012	Commd	Inquiry			CO	
6	0212	Commd	Lu=0			CO	
7	0212	Commd	ASCII Infomation page			CO	
8	0212	Commd				CO	
9	0012	Commd	Allocation Length=12H bytes			CO	
10	0012	Commd				CO	
11	0212	Commd				CO	
12	0212	Commd				CO	
13	0012	Commd				CO	
14	0212	Commd	Flag bit set,			CO	
15	0217	Msg_in	Reserved			MS	

Figure 2-1. Listing Menu

The SCSI Bus Inverse Assemblers

The FSSCSIA has seven inverse assemblers available for use with various SCSI devices. These give you the flexibility of selecting the correct inverse assembler to decode any of the different device types that are called out in the SCSI Standard ANSI X3.131 - 1994. The command sets for the inverse assemblers are listed in Tables 1-3 through 1-9.

The interpretation of the SCSI Command Sets vary in each inverse assembler to match the applications of various device types. Only one inverse assembler can be used at a time.

The FSSCSIA inverse assemblers are designed to decode commands, messages, phases, and status conditions for 8-bit and 16-bit Single-Ended and Differential SCSI Bus systems. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, simply roll the screen up to inverse assemble that block of memory.

Note

In order to correctly inverse assemble, the first byte of a command or message sequence must have been captured. The first byte does not have to be on the screen. If state capture starts or ends in the middle of a command or message byte sequence the inverse assembler will make an error in decoding that command or message.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Commands

The FSSCSIA inverse assemblers decode six, ten, and twelve byte commands. The first line of the command lists the hexadecimal code of the command and the actual command. Blocks are decoded on the byte where they begin. The second line lists the logical unit for the selected peripheral device and lists the names of any bits that are true (logical 1). For example, byte 1 of a command often has bit 4 as DPO, bit 3 as FUA, and bit 1 as RelAdr. If all three of these bits were set as true, the following information would be displayed on the second line:

DPO FUA RelAdr

The last line lists the Flag and Link conditions when they are true (logical 1).

Interpreting Vendor Unique and Reserved Information

The SCSI Standard ANSI X3.131 - 1994 has set aside some of the byte assignments for messages, status, and commands as either reserved for later definition vendor unique. In the case of message and status, the FSSCSIA inverse assembler listing will display the hexadecimal code for the information, list the information as either a message or status, and indicate if the information is vendor unique or reserved.

For commands, the FSSCSIA inverse assembler listing will display the hexadecimal code for the command, list the information as a command, and indicate which group the command is from.

Interpreting Messages

The FSSCSIA inverse assemblers decode the name of the message on the first line and indicate whether the message is going into the initiator (Msg_in) or out of the initiator (Msgout). The messages supported by the FSSCSIA are:

- 00h Command Complete
- 01h Extended Message
- 02h Save Data Pointer
- 03h Restore Pointers
- 04h Disconnect
- 05h Initiator Detected Error
- 06h Abort
- 07h Message Reject
- 08h No Operation
- 09h Message Parity Error
- 0Ah Linked Command Complete
- 0Bh Linked Command Complete (with Flag)
- 0Ch Bus Device Reset
- 0Dh Abort Tag
- 0Eh Clear Queue
- 0Fh Initiate Recovery
- 10h Release Recovery
- 11h Terminate I/O Process
- 20h Simple Queue Tag
- 21h Head of Queue Tag
- 22h Ordered Queue Tag
- 23h Ignore Wide Residue
- 80h - FFh Identify

Note

Identify messages include a logic unit specifier.

Extended Messages. Most messages are only one byte long, but extended messages may be up to 256 bytes long. When the FSSCSIA inverse assemblers decode an extended message, the name of the message is shown on the first line along with "xmsg" to identify it as an extended message. Also, Msg_in or Msgout appears on the first line to indicate whether the message is going into the initiator or out of the initiator.

Each extended message will also include information specific to that message on the first line:

- Modify Data Pointer includes the message arguments;
- Synchronous Data Transfer Request includes the transfer period and offset as a hexadecimal byte;
- Extended Identify includes a logical unit number;
- Wide Data Transfer Request includes the transfer width as a hexadecimal byte.

The next line shows the length of the extended message in hexadecimal, and the third line lists the message code. For a complete description of specific extended messages, refer to the SCSI Standard ANSI X3.131 - 1994, Section 6.5.

Interpreting Status

The FSSCSIA inverse assemblers decode all status conditions. Since status is only one byte, the actual status is listed following the status identifier. The status values supported by the FSSCSIA inverse assemblers are:

- Good
- Check Condition
- Condition Met
- Busy
- Intermediate
- Intermediate/Condition Met
- Reservation Conflict
- Command Terminated
- Queue Full

Interpreting Data

Since the data going across the bus is totally dependent and defined by the user, the FSSCSIA inverse assemblers can only indicate whether the data is going into the initiator (Dat_in) or out of the initiator (Datout) The rest of the data information cannot be interpreted by the FSSCSIA.

Arbitration, Select, and Reselect Phases

When an Arbitration, Select, or Reselect phase occurs, the FSSCSIA inverse assemblers identify the phase and list the interface device that is involved. For example:

Arbitr ID=3

indicates that interface device 3 has started an Arbitration phase.

Attention, Reset and Bus Free

The FSSCSIA inverse assemblers will display the Attention bit (Atn) for every state in which the Attention bit is asserted true.

The Reset bit (Rst) will be displayed for every state where it is asserted true. If the Reset bit becomes true while the SCSI bus is in the Bus Free state, the state is displayed as "Reset Bus Free." Otherwise, a true Reset bit is displayed as "Reset."

The Bus Free state is displayed as "Bus Free." If a Reset occurs while the bus is free, the state is displayed as "Reset Bus Free."

Parity Error

When the inverse assembler detects a parity error, it stops inverse assembly until the next valid state.

If a parity error is detected on the first line of a command, status, or message, then that line is not decoded. If the parity error is detected after the first line, the command or message is decoded.

Note

If parity is selected for the FSSCSIA and parity is not used in your SCSI Bus system, excess parity errors will appear on the listing display.

The Trigger Menu

The configuration files provided with the FSSCSIA set up the Trigger Specification so that only five lines of data are stored for each data transfer. Figure 2-2 shows the Trigger Specification. The events which occur in sequences 1, 2, and 3 are as follows:

Note

In the following descriptions, Phases refers to the type of information being transferred (data or commands), while State refers to a single line of information on the logic analyzer screen.

1. Sequence 1 defines the starting point of state storage in the logic analyzer memory. 'While storing "no state"' indicates that storage will not begin until the specified trigger. If this is changed to 'While storing "anystate"', the logic analyzer will use half of the memory to store pretrigger states and half of the memory to store posttrigger states.
2. Sequence 2 stores the states after the trigger. However, it will only store five consecutive data phases. After the fifth data phase it moves to sequence 3. You can change the number of data phases that are stored by changing the 5 to the desired number.
3. Sequence 3 filters out the data phases while it looks for a non data phase. When a non data phase occurs, it stores that phase and transfers control back to sequence 2.

You can count the number of data phases that are filtered out in sequence 3 by setting the Count window to "STATES." The number of filtered data phases will be displayed on the first line after the five data states. The time lapse between states can be observed by setting the Count window to "TIME." However, the STATES and TIME selections reduce the state storage memory by one half.

For further information on changing the Trigger menu specifications, refer to your logic analyzer operating manual.

100/500MHz LA C
Trigger 1
Cancel
Run

State Sequence Levels				Timer	
				1	2
1	While storing "no state"	TRIGGER on "ARBIT" 1 time		-	-
2	While storing "anystate"	Then find "DATA" 5 times		-	-
	Else on "≠DATA" go to level 2				
3	Store "≠DATA"			-	-
	On "≠DATA" go to level 2				

Label

DATA_

STAT

PHASE

ATN

RST

Terms

Hex

Symbol

Symbol

Symbol

Symbol

ARBIT	XXXX	ARBITRATION	DATA OUT		
DATA	XXXX	DATA XFR	DATA XFR	abs X	
c	XXXX	absolute XXXX	absolute X	abs X	abs X
d	XXXX	absolute XXXX	absolute X	abs X	abs X

Figure 2-2. Trigger Screen

LED Indicators

Three LED light bars of 10 LEDs each are used as front panel indicators of the static condition of the bus.

- One group for Data; and
- One group for Status.

The following LEDs are provided for Data: data bits 0 through 15, two Parity, and two Parity Error. Parity Error is not one of the SCSI signal lines; it is generated by internal hardware of the preprocessor interface when a parity error occurs and the front panel State Parity Error switch is on.

Nine SCSI Status lines are shown on the other LED light bar. These include I/O, C/D, MSG, and the SCSI phases.

Additional Information

Introduction

This section contains additional reference information including the characteristics and signal mapping for the FSSCSIA Preprocessor Interface.

Characteristics

The following characteristics are not specifications, but are typical operating characteristics for the FSSCSIA Preprocessor Interface. These characteristics are included as additional information for the user.

Bus Compatibility:

8-bit and 16-bit Single-Ended and Differential SCSI Bus systems containing any of the device types specified in the SCSI Standard ANSI X3.131 - 1994.

SCSI Standard Supported:

ANSI X3.131 - 1994.

SCSI Device Types Supported:

Direct Access Devices, Write Once Read Multiple Devices, and Optical Devices (ISCSIDIR)

Sequential Devices (ISCSISEQ)

Printers (ISCSIPTR)

Processor Devices (ISCSIPRC)

Sequential Devices using Group 0 (6 byte) commands communicating with a Direct Access Device using Group 1 (10 byte) commands (ISCSIDSE)

Automatic Media Changers (ISCSIAMC)

CD ROM Devices (ISCSICDR)

Accessories Required:

Adapter cables may be required for some SCSI bus systems

Maximum Bus Speeds:

10 MHz

Timing Specifications:

Meets all timing specifications set forth in SCSI ANSI Specification (ANSI X3.131 - 1994.)

Signal Line Loading:

0.4 mA TTL Low at 0.5 V.

Bus Cycles Interpreted:

Arbitration Select/Reselect Commands Messages Status Reset Bus Free

Power Requirements:

0.80 A at +5 Vdc max, supplied by the logic analyzer.

Logic Analyzer Required:

HP 1650A (with HP 10449A memory upgrade), HP 1650B, HP 1652B, HP 1660X/61X/62X/63X, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and one expansion card), HP 16542A (Master Card and one expansion card), or HP 16550A, HP 1670X/71X/72X, HP 16554X/55X/56X.

Number of Probes Used:

Two for state or timing, four for both.

Environmental Temperature:

Operating: 0 to +55 degrees C (+32 to +131 degrees F)

Nonoperating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude:

Operating: 4600 m (15, ft)

Nonoperating: 15,300 m (50, ft)

Humidity:

To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Clocking

The SCSI bus signals are sampled and routed to the logic analyzer so that all signals for a bus cycle are sent to the logic analyzer at the same time. Since the SCSI bus signals become active at different times throughout the bus cycle, some of the signals are latched by the preprocessor interface, while others are connected directly to the logic analyzer. When the logic analyzer is clocked, the latched and straight through signals are all read at the same time.

The 16 Data bus lines plus the two Parity bits and the two Parity Error bits that are generated by the preprocessor interface hardware are sampled by internal latches. The I/O, C/D and MSG signals are latched internally at the same time. The outputs of these latches are then read at a later time when the logic analyzer receives its clock.

The Attention, Reset, Busy and Select signals are not latched internally but are connected directly to the logic analyzer. These signals are sampled after the signals listed in the previous paragraph. Figure 3-1 shows the latching and clocking cycle for the FSSCSIA.

Arbitration Phase. The SCSI bus is sampled by the FSSCSIA Preprocessor Interface 800 ns after both BUSY and SELECT become active. The logic analyzer is clocked 40 ns after these signals are sampled.

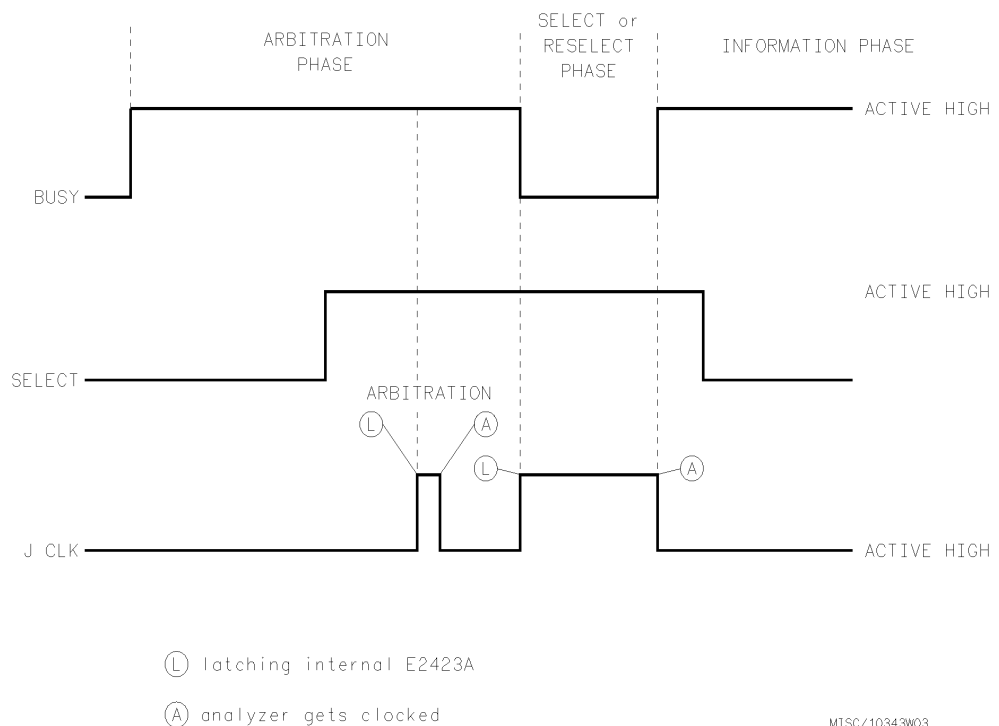


Figure 3-1. FSSCSIA Latching and Clocking Timing

Select and Reselect Phase. Internal latching takes place at the beginning of the select phase when BUSY becomes negated. The logic analyzer is clocked when BUSY becomes active at the end of the SELECT phase.

Information Phases. When the SCSI bus is transferring data and instructions, the handshake lines determine the clock. Figure 3-2 and Table 3-1 show the latching and clocking for the information phase.

Command, Status, and Message Phases. Internal latching takes place when the Request handshake goes active. The logic analyzer is clocked when the Acknowledge line goes inactive (negated).

Data In Phase. Request is the only controlling signal for the Data In phase. Internal latching takes place on the active edge of Request. The analyzer is clocked on the negating edge of Request.

Data Out Phase. Acknowledge is the only controlling signal for the Data Out phase. Internal latching takes place on the active edge of Acknowledge. The analyzer is clocked on the negating edge of Acknowledge.

Bus Free. The FSSCSIA waits for 400 ns after both BUSY and SELECT are negated. Then the bus is sampled. First a latching operation takes place, and 40 ns later the logic analyzer is clocked. If RESET is active, a Reset Bus Free is displayed on the analyzer screen. Otherwise only a Bus Free is displayed on screen.

Reset. The RESET signal is sampled along with all other signals during the bus active phases. If in the Bus Free condition and a reset takes place, a latching operation takes place with a logic analyzer clock following 40 ns later.

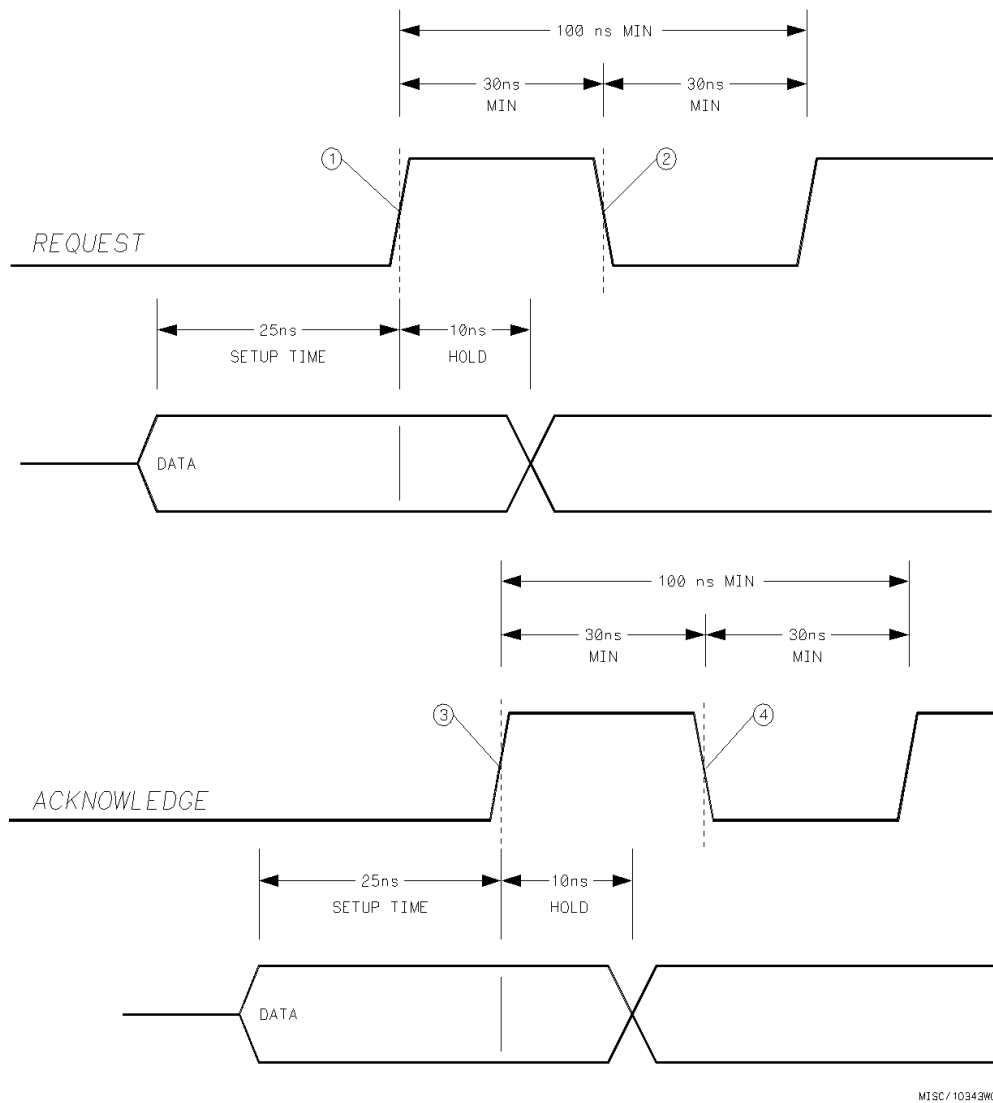


Figure 3-2. Request and Acknowledge Timing

Table 3-1. Information Phase Latching and Clocking

Phase	Internal Latching	Analyzer Clocked
Command Status MSG	1 (See Drawing above)	4
Data In	1	2
Data Out	3	4

Interface Description

The FSSCSIA provides a complete mechanical and electrical interface between the logic analyzer and an 8-bit or 16-bit SCSI bus system. This interface allows the logic analyzer to capture and decode all of the activities on the SCSI bus. The SCSI bus is observed by high impedance comparators on the FSSCSIA. The outputs of these comparators go directly to the logic analyzer for timing analysis.

For state analysis, the SCSI bus phase activities are decoded by the Phase Detection Logic. The logic analyzer clock is sent out at the correct times to capture the data.

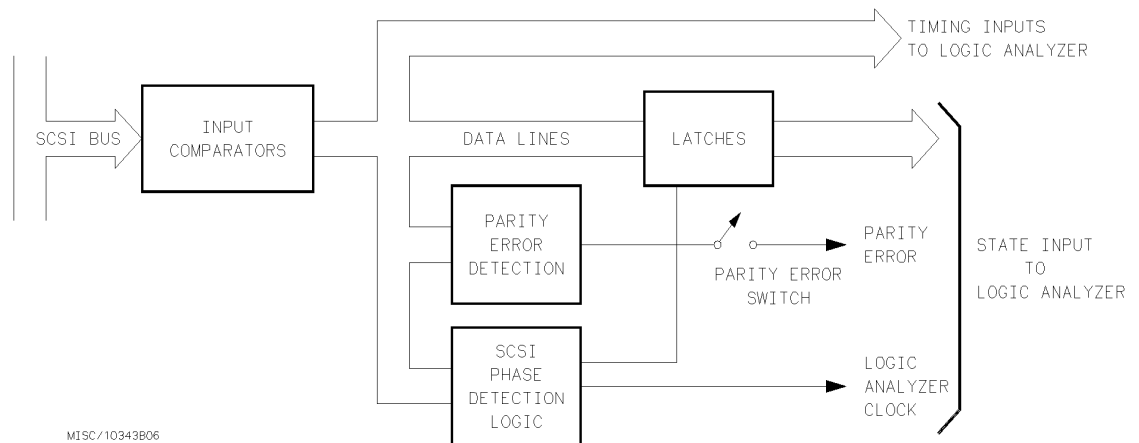


Figure 3-3. FSSCSIA Block Diagram

SCSI Bus Signal to FSSCSIA Connector Mapping

The following table describes the electrical interconnections implemented with the FSSCSIA Preprocessor Interface. Since the pods on the logic analyzer may be numbered differently than the other logic analyzers, refer to table 1-1 to correlate the pod numbers.

Note

The interconnections implemented for state analysis with the FSSCSIA are not direct interconnections. The FSSCSIA Preprocessor Interface places digital circuitry between SCSI bus signals and the logic analyzer input on pods 1 and 2. For timing analysis, the interconnections are straight through.

Table 3-2. Logic Analyzer to SCSI Signal Connections

Preprocessor Pod	Logic Analyzer Probe	SCSI Bus Signal	Analysis Type
1	0	I/O	State
1	1	C/D	State
1	2	MSG	State
1	3	SEL	State
1	4	BSY	State
1	5	REQ	State
1	6	ACK	State
1	7	ATN	State
1	8	RESET	State
1	9	LBUSPT	State
1	10	HBUSPT	State
1	11	LPTYER	State
1	12	HPTYER	State
1	13	(Blank)	State
1	14	(Blank)	State
1	15	BUSIZE	State
2	0	Data 0	State
2	1	Data 1	State
2	2	Data 2	State
2	3	Data 3	State
2	4	Data 4	State
2	5	Data 5	State
2	6	Data 6	State
2	7	Data 7	State
2	8	Data 8	State
2	9	Data 9	State
2	10	Data 10	State
2	11	Data 11	State
2	12	Data 12	State
2	13	Data 13	State
2	14	Data 14	State
2	15	Data 15	State

Table 3-2. Logic Analyzer to SCSI Signal Connections (continued)

Preprocessor Pod	Logic Analyzer Probe	SCSI Bus Signal	Analysis Type
3	0	I/O	Timing
3	1	C/D	Timing
3	2	MSG	Timing
3	3	SEL	Timing
3	4	BSY	Timing
3	5	REQ	Timing
3	6	ACK	Timing
3	7	ATN	Timing
3	8	RESET	Timing
3	9	LBUSPT	Timing
3	10	HBUSPT	Timing
3	11	LPTYER	Timing
3	12	HPTYER	Timing
3	13	(Blank)	Timing
3	14	(Blank)	Timing
3	15	BUSIZE	Timing
4	0	Data 0	Timing
4	1	Data 1	Timing
4	2	Data 2	Timing
4	3	Data 3	Timing
4	4	Data 4	Timing
4	5	Data 5	Timing
4	6	Data 6	Timing
4	7	Data 7	Timing
4	8	Data 8	Timing
4	9	Data 9	Timing
4	10	Data 10	Timing
4	11	Data 11	Timing
4	12	Data 12	Timing
4	13	Data 13	Timing
4	14	Data 14	Timing
4	15	Data 15	Timing

SCSI Overview

Introduction

The Small Computer Systems Interface (SCSI) is a that may be used for fast transfers of data between computers and peripherals. The standard hardware of the 8-bit or 16-bit SCSI Bus is a 50- or 68-wire cable that interconnects up to a maximum of 8 or 16 devices on the bus. By definition there are 8 or 16 data lines with one or two parity bits. Parity is odd and the use of the parity is optional for SCSI.

There are two SCSI Bus Types:

- Single-Ended
- Differential

The Single-Ended bus runs at TTL levels with a logical 1 (active) being a low level on the bus. The Differential bus uses two lines per signal with the lines moving between approximately 2 and 3 volts.

Each device on the bus is assigned a device number of 0 through 15. If there is a condition of more than one device asking for the bus at one time, the highest priority device gets the bus. The device priority is in the following order, with 7 the highest and 8 the lowest priority: 7, 6, 5, 4, 3, 2, 1, 0, 15, 14, 13, 12, 11, 10, 9, 8. Each device is assigned one line on the data bus for a device ID.

With SCSI, the host computer is not the bus controller. The device that the host calls is the bus controller. Most often this is a mass storage device.

The host computer is called the INITIATOR and the device that the host calls on the bus is called the TARGET.

SCSI Status Lines

Nine status lines are defined by the SCSI Standard ANSI X3.131 - 1994:

- I/O
- C/D
- MESSAGE
- BUSY
- SELECT
- REQUEST
- ACKNOWLEDGE
- ATTENTION
- RESET

There are also ten phases defined by the SCSI standard. These are not timing phases, but conditions of the bus action. They are:

- ARBITRATION
- SELECT
- RESELECT
- DATA OUT
- DATA IN
- COMMAND
- STATUS
- MESSAGE OUT
- MESSAGE IN
- BUS FREE

I/O, C/D, and Message. The I/O, C/D, and Message Status lines define six of these phases of the SCSI Bus (see Table A-1).

Busy. The bus is considered free when the Busy and Select lines are inactive. An initiator asks for the bus by driving Busy active and driving its identification (ID) line active on the data lines. If no other device with a higher priority drives the line, then the initiator signals that it has the bus by driving Select active. This is called the Arbitration Phase. The parity bit is not tested in the Arbitration Phase.

Select. After the initiator has the bus and drives Select active it then drives the ID line of the device it is calling (the target) active and releases Busy. The device being called responds by driving Busy active. The Initiator at this point releases Select. Select is not used for any other purpose. This is called the Select or Reselect phase. Reselect is when the Target is calling the Initiator. This is accomplished by driving the I/O line active after the Arbitration phase. The target device is now in control of the Busy line and is the only device that can release the bus. At this point the bus is ready to transfer information.

Request and Acknowledge. These are handshake lines. Request is driven by the target and Acknowledge is driven by the initiator. These handshakes are used to transfer information between devices in either direction. The information that is transferred between devices is enveloped in one of six phases that are determined by the setting of the three lines: I/O, C/D, and Message (see Table A-1).

Attention. Since the target is in control of the bus lines, the Attention line (Atn) is used by the Initiator to request to send a Message or a Command.

Reset. This is used to reset the bus to a Bus Free State and reset the devices that are on the bus.

Note

The SCSI standard includes over 82 commands, 9 Status conditions, and 25 Messages in its instruction set and has room for more to be added. The bus is defined to be capable of transferring 10 Megabytes per second using an 8-bit bus or 20 Megabytes per second using a 16-bit bus.

Table A-1. Phases

Message	C/D	I/O	Name of Phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Phase 4
1	0	1	Phase 5
1	1	0	Message Out
1	1	1	Message In

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check that the logic analyzer pods are connected to the proper connectors, as listed in Table 1-1.

For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity, the +5 V supply coming from the analyzer may not be getting to the preprocessor interface.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the FSSCSIA and measure across pins 1 and 2 or pins 39 and 40 (see Figure B-1).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

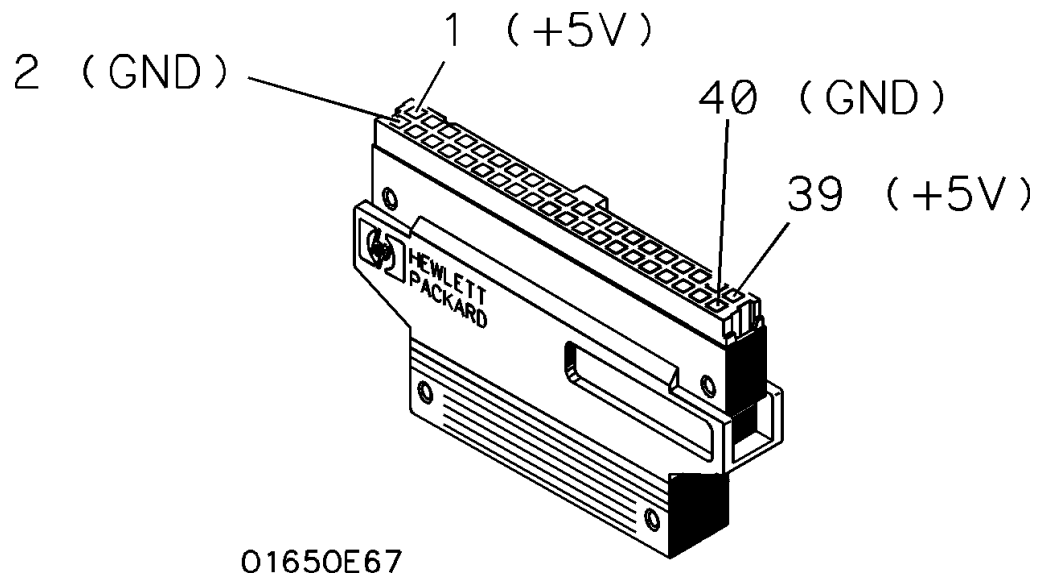


Figure B-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT and DATA format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to <60 ns. If this error message is observed with the Clock Period set to >60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message on an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer indicates that the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.