Acquisition Clock Dithering in a Digital Oscilloscope

When a frequency component of the input signal is greater than half the sample rate, aliasing can occur. When the oscilloscope is equivalent time sampling, signals that are subharmonics of the sample clock will be poorly displayed. In the HP 54645A/D oscilloscopes, these effects are greatly reduced by dithering the sample clock during and between acquisitions.

by Derek E. Toeppen

A common concern of digital oscilloscope users is that there are combinations of oscilloscope settings and input signals that will cause the standard digital oscilloscope architecture to display a signal poorly or incorrectly. Since an oscilloscope is a device intended to display a variety of signals, sooner or later one of these combinations of settings and signals will be encountered, leaving the user confused and with diminished confidence in the instrument.

The classic case occurs when the sample rate and input signal violate the Nyquist sampling theorem, or specifically, when a frequency component of the input signal is greater than half the sample rate. When this happens, an aliased waveform will be displayed. A more subtle case occurs when the digital oscilloscope is random repetitive sampling (also known as equivalent time sampling).[1] In this case, signals that are subharmonics of the sample clock will be poorly displayed. This occurs because the repetitive samples are not randomly distributed over the input signal, but rather are bunched together.

There are ways of designing digital oscilloscopes that greatly reduce these effects. These techniques involve dithering the sample clock during and between acquisitions (intra-acquisition and interacquisition dithering). Two such techniques used in the design of the 54645A/D oscilloscopes will be discussed here.
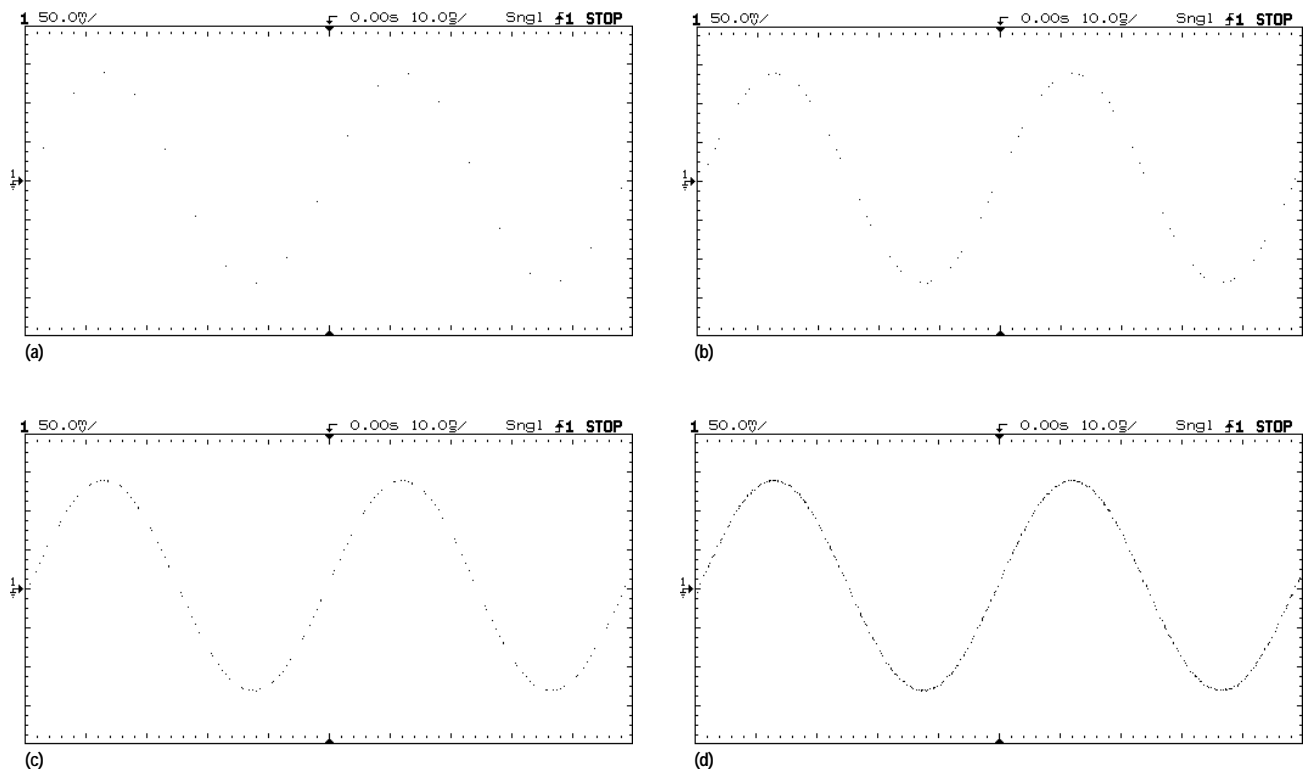

Fig. 1. *The development of a waveform during random repetitive sampling. (a) The result of one acquisition of an input signal. (b) The same signal after three acquisitions. (c) After seven acquisitions. (d) After 20 acquisitions.*

Interacquisition Dithering

The underlying principle of random repetitive sampling is that there is no phase correlation between the sample clock and the signal being sampled. This principle ensures that samples taken of the signal are randomly distributed over the signal, and when accumulated over time, will develop a detailed reconstruction of the input signal. The accumulation of samples is illustrated in Fig. 1. Fig. 1a shows the initial set of samples acquired during the first acquisition of the signal. The sample rate and input frequency meet the Nyquist criterion but that there are, nonetheless, large gaps between samples. Fig. 1b shows the same signal after accumulating three acquisitions. Note the random placement of the second and third sets of samples relative to the first set. The shape of the signal is becoming more defined. Fig. 1c is after seven acquisitions and Fig. 1d after 20. In Fig. 1d, the signal shape is well-defined and accurately represented.

The typical digital oscilloscope relies on the fact that the sample clock (f_s) inside the oscilloscope is derived from a clock separate and independent from the signal being measured (f_i) to satisfy the criterion that there is no phase correlation between the two signals. However, nothing prevents the oscilloscope user from applying a signal that is the same frequency as the sample clock or subharmonically related to it ($f_i = f_s/n$). When this happens, the sample points are no longer randomly distributed across the input waveform as in Fig. 1. This case is illustrated in Fig. 2. In Fig. 2, a sine wave with a frequency equal to precisely 1/10 the sample clock ($f_i = f_s/10$) is applied to a random repetitive sampling digital oscilloscope. The result is that all sets of samples accumulate around the same locations, creating the bunching effect mentioned before. Since the acquisition clock and the input sine wave are not phase-locked to each other, if the waveform is allowed to accumulate long enough, the points will spread out, but the time it takes to do this will depend on the stability of the two sources.
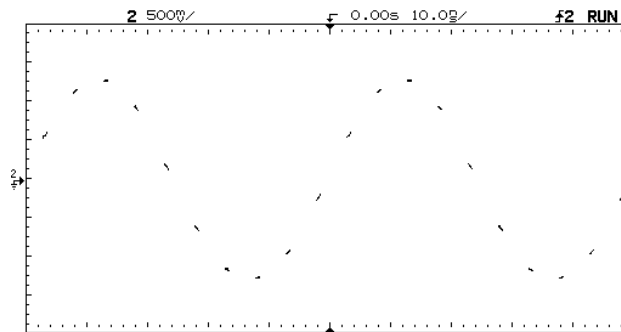

Fig. 2. *The result of applying a sine wave with a frequency equal to precisely 1/10 the sample clock frequency to a random repetitive sampling digital oscilloscope. All sets of samples accumulate around the same locations.*

If the sample set acquired during the first acquisition in Fig. 2 is taken as a reference, then what is needed is a way to shift subsequent sets of samples so that they fall in between the points of the first set (as they did in Fig. 1), or, viewed in terms of the phase of the sample clock, to spread subsequent sets over the 360 degrees of phase between the initial sample points. This can be achieved by shifting the phase of the acquisition clock after each acquisition.

A circuit ideally suited for this task is the phase-locked loop. The basic phase-locked loop is illustrated in Fig. 3a. In this circuit, the phase of the reference clock is compared to the phase of the output of the voltage-controlled oscillator (VCO). The loop filter drives the VCO input to cause the phase difference between the reference clock and the VCO output to be zero. If an error voltage is injected into the filter at the output of the phase comparator, as in Fig. 3b, then the error voltage appears as a phase error to the loop. The loop will adjust the VCO to create a real phase error to cancel the injected error voltage, thereby generating a nonzero phase difference between the reference clock and the VCO output. If the VCO output is used as an acquisition clock, then the error voltage node can be used to create phase shifts in the acquisition clock.

A block diagram of the phase-locked loop circuit used in the HP54645A/D to produce this type of interacquisition clock dither is shown in Fig. 4. In this circuit, the error voltage is generated by a 8-bit digital-to-analog converter (DAC). This provides 2^8 or 256 discrete phase shifts in the acquisition clock. The 8-bit digital word written to the DAC is pseudorandomly generated by one of the oscilloscope's processors to be consistent with the nature of random repetitive sampling. Fig. 5 illustrates the effectiveness of this technique. It is a plot of the sine wave of Fig. 2 using phase-locked-loop-generated interacquisition dither of the acquisition clock. All bunching of the sample points has been eliminated.

Intra-Acquisition Dithering

Real-time sampling is generally considered to be the solution for aliasing in a digital oscilloscope. The reasoning is that if the oscilloscope's sampling rate is always at least twice its bandwidth then aliasing cannot occur. However, what is commonly overlooked is that to overcome finite memory limitations, even real-time sampling oscilloscopes are forced to reduce their sample rates at some point to capture long time periods (see *Article 4*). When this occurs, the oscilloscope becomes susceptible to aliasing.

A common technique for decreasing the sample rate in a digital oscilloscope is illustrated in the block diagram in Fig. 6. In this circuit, the digitizer always samples at the maximum rate but not all digitized points are stored into memory. The
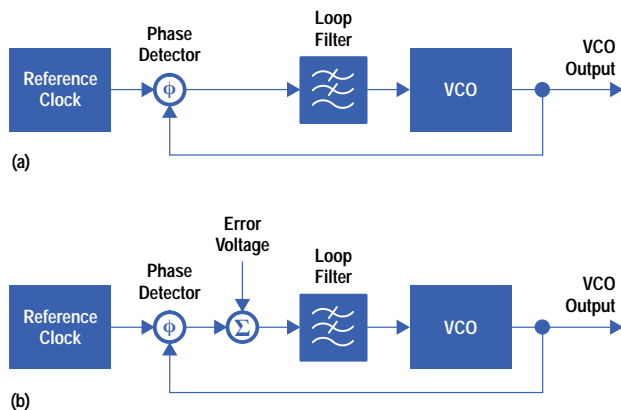
Fig. 3. (a) Phase-locked loop. (b) Phase error voltage injected into the loop.
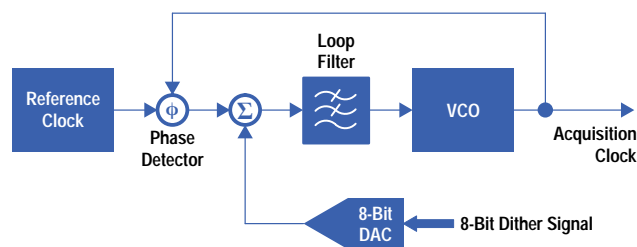

Fig. 4. Method of introducing acquisition clock dither in the HP 54645A/D oscilloscope phase-locked loop to prevent the bunching effect shown in Fig. 2.
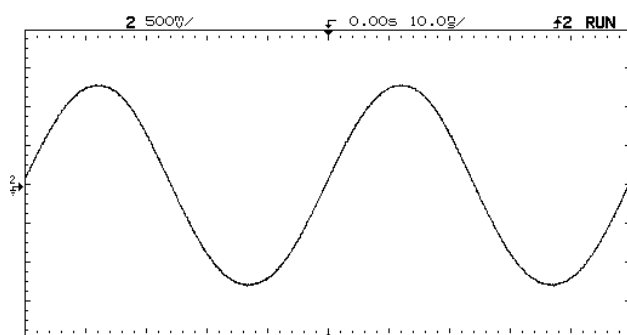

Fig. 5. Acquiring the signal of Fig. 2 with interacquisition dither eliminates the bunching effect.
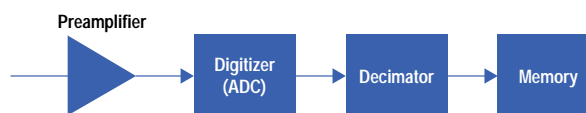

Fig. 6. Decreasing the sample rate by decimation. The digitizer always samples at the maximum rate but not all samples are stored into memory.

decimator between the digitizer and memory handles the selection of the desired digitized points. To reduce the sample rate by the factor N, the decimator passes only every Nth point on to the memory. All other digitized points are lost. This technique can be modified slightly in a way that will greatly reduce the likelihood of an aliased waveform developing.

To understand this, first consider how an aliased waveform is generated. If a sine wave with frequency f_i is sampled with frequency f_s, where $f_i > f_s/2$, then an aliased sine wave of frequency equal to $|f_i - f_s|$ will occur. For example, suppose that a 1.01-MHz sine wave is applied to a digital oscilloscope sampling at 1 MSa/s. An aliased frequency (or beat frequency) of 10 kHz will result. What is seen on screen is what appears to be an untriggered 10-kHz sine wave.

This phenomenon repeats itself at each harmonic of the sample clock, so if a frequency of 10.01 MHz, near the tenth harmonic of the sample clock, is input to the same oscilloscope, the same aliased 10-kHz signal is produced. However, between the samples taken at 1-μs intervals (1/1 MSa/s), ten cycles of the input sine wave occur. When the decimator process shown in Fig. 6 is used to reduce the sample rate, samples of those cycles are thrown away. It is these discarded sample points that can be used to prevent the aliased waveform.

Instead of storing every Nth digitized point, the decimator can be designed to randomly select one out of every N points for storage. In the case of the 10.01-MHz input, the points placed in memory are points randomly selected from the ten cycles of the input that occur in every 1-μs interval. This random sample selection technique effectively dithers the acquisition clock during the acquisition and prevents a beat frequency from developing.

This intra-acquisition dithering technique has been used throughout the HP546XX oscilloscope product line and again in the HP54645A/D products. The effect it has on aliasing is dramatic. Fig. 7a shows the aliased 10-kHz sine wave that is produced when a 10.01-MHz sine wave is sampled at 1 MSa/s. Fig. 7b shows the same display using the dithering process just described. The resulting display is a fuzzy band much like what would be seem on an analog oscilloscope, with all signs of an aliased waveform removed.
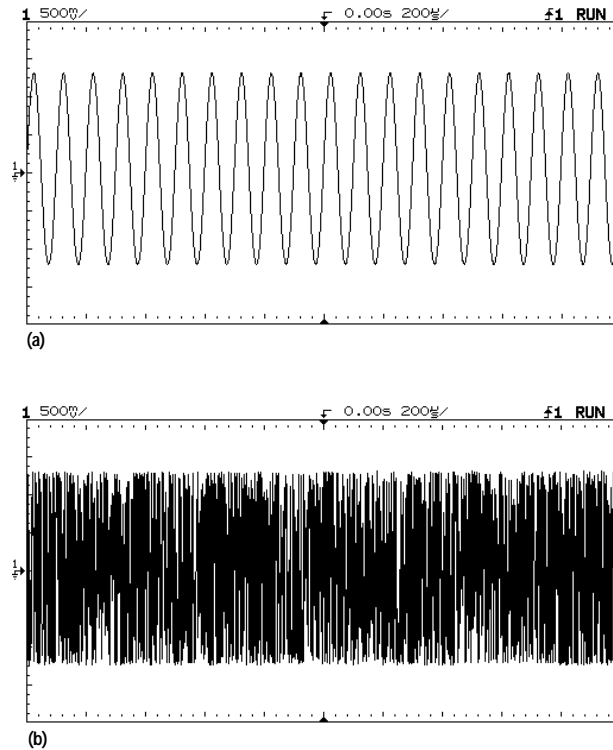
Acknowledgments

Fig. 7. *(a) An aliased 10-kHz sine wave produced when a 10.01-MHz sine wave is sampled at 1 MHz. (b) The same display using intra-acquisition dithering (random decimation) is a fuzzy band much like what would be seem on an analog oscilloscope, with all signs of an aliased waveform removed.*

Reference

1. K. Rush and D.J. Oldfield, "A Data Acquisition System for a 1-GHz Digitizing Oscilloscope," Hewlett-Packard Journal, Vol. 38, no. 4, April 1986, pp. 4-11.

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