Timer/Counter/ Analyzer

PM6690

Service Manual

FLUKE®

4822 872 20306
May 2006 - Fourth Edition

GENERAL INFORMATION

Method of Notation

This manual contains directions and information that apply to the PM6690 Timer/Counter/Analyzer. In order to simplify the references, the following designation system is used throughout the manual:

– PM6690 is abbreviated to *'90'*.

Warranty

The Warranty Statement is included in the Getting Started Manual.

Declaration of Conformity

The complete text with formal statements concerning product identification, manufacturer and standards used for type testing is available on request.

Hardware Versions

This Service Manual provides Source of Supply information for the Fluke Model PM6690 Timer/Counter/Analyzer, which may contain an OLD version of the Main CCA, called Version A, or a NEW version of the Main CCA, called Version B. Both the old and the new version of the Main CCA have the same part number. All orders for the old version of the Main CCA will be filled with the new version of the Main CCA. When the old version of the Main CCA is returned to the factory for repair, the new version of the Main CCA will be returned in place of the old version of the Main CCA, if the microprocessor has to be replaced.

Devices with serial numbers up to and including 916779 are equipped with a Triscend microprocessor, whereas devices with higher serial numbers have a Sharp microprocessor. Both are based on an ARM7 core, and from the operator's point of view the behavior is not affected. However, essential parts of the main PCB differ, and the corresponding sections of the service manual are consequently affected. Even though large parts of the hardware are common to both versions, we have preferred to divide the pertinent chapters into separate sections, where certain parts are repeated, all in order to improve legibility and simplify troubleshooting.

Version A refers to devices equipped with the Triscend microprocessor.
Version B refers to devices equipped with the Sharp microprocessor.

The chapters that need special attention are:

Chapter 4, Circuit Descriptions
Chapter 6, Repair
Chapter 8, Replacement Parts
Chapter 9, Schematic Diagrams

■ Firmware Compatibility

Despite the relatively large hardware differences, we have managed to integrate the firmware, so that future upgrades can be applied to both versions by means of the same hex file. Thus there is no need to check the serial number or else find out which processor is inside the cover. Just proceed according to the instructions given in Chapter 5, Corrective & Preventive Maintenance.

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Contents

Chapter 1

Safety Instructions

WARNING: These servicing instructions are for use by qualified personnel only. To reduce the risk of electric shock, do not perform any servicing other than that specified in the Operators Manual unless you are fully qualified to do so.

Caution and Warning Statements

Introduction

Read this chapter carefully before you check, adjust or repair the instrument.

It is essential for your own safety to know the restrictions that are applicable to all equipment that can be connected to line power. Therefore, read the section on *Safety Precautions* below.

In addition to the general statements given in this chapter you will find specific caution and warning statements where necessary throughout the manual.

Safety Precautions

This instrument has been designed and tested for Measurement Category I, Pollution Degree 2, in accordance with EN/IEC 61010-1:2001 and CAN/CSA-C22.2 No. 61010-1-04 (including approval). It has been supplied in a safe condition.

This manual contains information and instructions that should be followed by the user and the service technician to ensure safe operation and repair in order to keep the instrument in a safe condition. It is essential that you follow generally accepted safety procedures in addition to the safety precautions specified in this manual.

The instrument is designed to be used by trained personnel only. Removing the cover for repair, maintenance, and adjustment of the instrument must be done by qualified personnel who are aware of the hazards involved.

The warranty commitments are rendered void if unauthorized access to the interior of the instrument has taken place during the given warranty period.

CAUTION: Indicates where incorrect procedures can cause damage to, or destruction of equipment or other property.

WARNING: Indicates a potential danger that requires correct procedures or practices to prevent personal injury.

Symbols

Shows where the protective ground terminal is connected inside the instrument. **Never** remove or loosen this screw.

Indicates that the operator should consult the manual.

You can, for instance, find such a symbol on the front panel below the A and B inputs. It points out that the damage level for the input voltage decreases from 350 V_p to 12 V_{rms} when you switch the input impedance from 1 MΩ to 50 Ω.

If in Doubt about Safety

Whenever you suspect that it is unsafe to use the instrument, you must make it inoperative by doing the following:

– Disconnecting the line cord

– Clearly marking the instrument to prevent its further operation by unauthorized personnel

For example, the instrument is likely to be unsafe if it is visibly damaged.

Grounding

Grounding faults in the line voltage supply will make any instrument connected to it dangerous. Before connecting any unit to the power line, you must ensure that the protective ground functions correctly. Only then can a unit be connected to the power line and only by using a three-wire line cord. No other method of grounding is permitted. Extension cords must always have a protective ground conductor.

CAUTION: If a unit is moved from a cold to a warm environment, condensation may cause a shock hazard. Ensure, therefore, that the grounding requirements are strictly met.

WARNING: Never interrupt the grounding cord. Any interruption of the protective ground connection inside or outside the instrument or disconnection of the protective ground terminal is likely to make the instrument dangerous.

Operation

Orientation and Cooling

The instrument can be operated in any position desired. Make sure that the air flow through the ventilation slots at the top,

and side panels is not obstructed. Leave 5 centimeters (2 inches) of space around the counter.

Fold-Down Support

For bench-top use, a fold-down support is available for use underneath the counter. This support can also be used as a handle to carry the instrument.

Rackmount Adapter

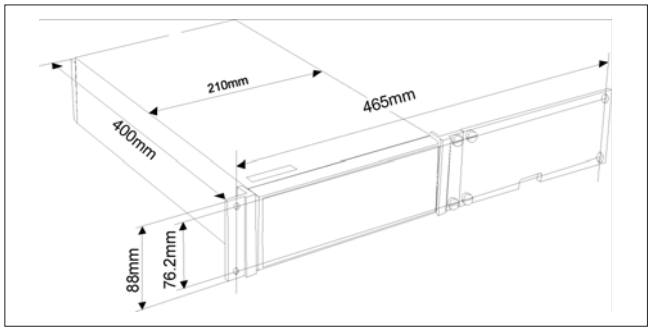

Fig. 1-1 *Dimensions for rackmounting hardware.*

If you have ordered a 19-inch rack-mount kit for your instrument, it has to be assembled after delivery of the instrument. The rackmount kit consists of the following:

– 2 brackets, (short, left; long, right)

– 4 screws, M5 x 8

– 4 screws, M6 x 8

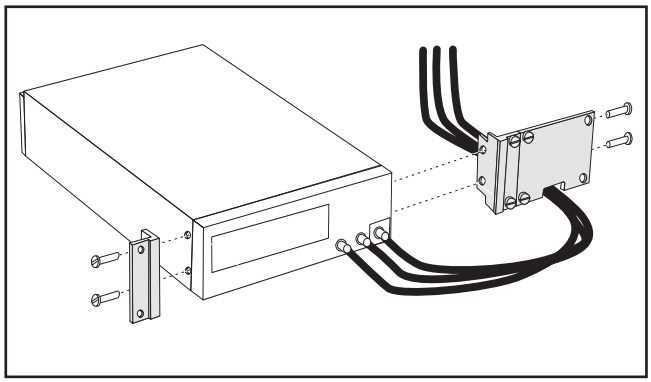

Fig. 1-2 *Fitting the rack mount brackets on the counter.*

WARNING: Do not perform any internal service or adjustment of this instrument unless you are qualified to do so.

Before you remove the cover, disconnect mains cord and wait for one minute.

Capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

■ Assembling the Rackmount Kit

– Make sure the power cord is disconnected from the instrument.

– Turn the instrument upside down.
See Fig. 1-3.

– Undo the two screws (A) and remove them from the cover.

– Remove the rear feet by undoing the two screws (B).

– Remove the four decorative plugs (C) that cover the screw holes on the right and left side of the front panel.

– Grip the front panel and gently push at the rear.

– Pull the instrument out of the cover.

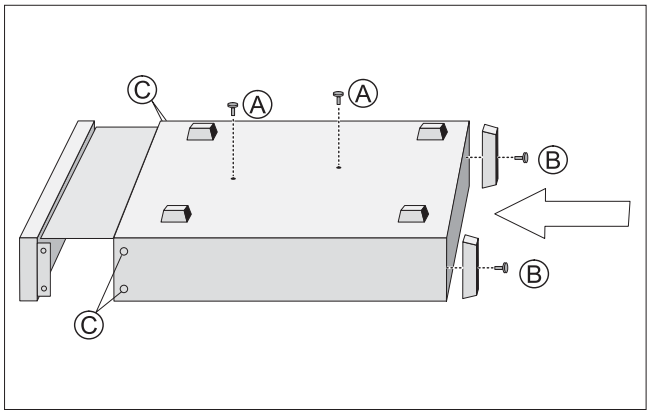

Fig. 1-3 *Remove the screws and push the counter out of the cover.*

– Remove the four feet from the cover.

Use a screwdriver as shown in the following illustration or a pair of pliers to remove the springs holding each foot, then push out the feet.

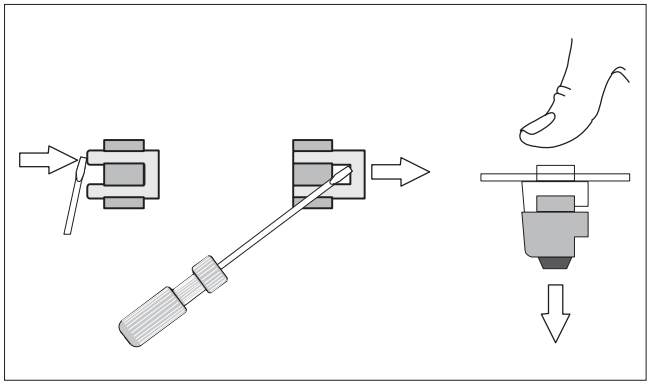

Fig. 1-4 *Removing feet from the cover.*

– Push the instrument back into the cover. See Fig. 1-3.

– Mount the two rear feet with the screws (B) to the rear panel.

– Put the two screws (A) back.

– Fasten the brackets at the left and right side with the screws included as illustrated in Fig. 1-1.

– Fasten the instrument in the rack via screws in the four rack-mounting holes

The long bracket has an opening so that cables for Input A, B, and C can be routed inside the rack.

■ Reversing the Rackmount Kit

The instrument may also be mounted to the right in the rack. To do so, first remove the plate on the long bracket and fasten it on the short one, then perform the preceding steps.

Line Voltage

■ Setting

The Counter may be connected to any AC supply with a voltage rating of 90 to 265 V_{rms}, 45 to 440 Hz. The counter automatically adjusts itself to the input line voltage.

■ Fuse

The secondary supply voltages are electronically protected against overload or short circuit. The primary line voltage side is protected by a fuse located on the power supply unit. The fuse rating covers the full voltage range. Consequently there is no need for the user to replace the fuse under any operating conditions, nor is it accessible from the outside.

CAUTION: If this fuse is blown, it is likely that the power supply is badly damaged. Replace the complete power supply unit. Do not replace the fuse.

Chapter 2

Performance Check

General Information

WARNING: Before turning on the instrument, ensure that it has been installed in accordance with the Installation Instructions outlined in Chapter 1 of the Operators Manual.

This performance procedure is intended for:

– checking the instrument's specification.

– incoming inspection to determine the acceptability of newly purchased instruments and recently recalibrated instruments.

– checking the necessity of recalibration after the specified recalibration intervals.

NOTE: The procedure does not check every facet of the instrument's calibration; rather, it is concerned primarily with those parts of the instrument which are essential for determining the function of the instrument.

It is not necessary to remove the instrument cover to perform this procedure.

Test Equipment

Type of Equipment	Required Specifications
Reference Oscillator	10 MHz, $1*10^{-8}$ (e.g. 908) for calibrating PM6690/_1_
	10 MHz, $1*10^{-9}$ (e.g. 909) for calibrating PM6690/_5_ & PM6690/_6_
Voltage Calibrator	DC -50 V to +50 V (e.g. 5500A) for calibrating the built-in voltage reference, alternatively corresponding DC power supply + DVM with uncertainty <0.1 %
LF Synthesizer	Square/ Sine up to 10 MHz, 10 V_{RMS}
Pulse Generator	2 ns rise time, 5 V peak, >10 MHz, continuous & one-shot trigger
Oscilloscope	350 MHz, <3% voltage uncertainty
RF Signal Generator	10 MHz to 3 or 8 GHz dep. on prescaler option, 10 MHz ext.ref.
Power Splitter	50 Ω 6 dB BNC
T Adapter (F-M-F)	BNC
Termination	50 Ω feedthrough BNC
Lowpass Filter	50 kHz (for 1 MΩ load)
BNC Cables	5 to 7 pcs of suitable lengths

Table 2-1 *Recommended equipment for calibration and performance check.*

Preparations

Power up your instrument at least 30 minutes before checking to let it reach normal operating temperature. Failure to do so may result in certain test steps not meeting equipment specifications.

Front Panel Controls

Internal Self-Tests

The test programs forming the self-diagnosis can be activated from the front panel as follows:

– Press **USER OPT**

– Press **Test**.

– Press **Test Mode**.

– Select one of the six tests available by pressing the softkey below the label with the name of the test function. Five of the tests (RAM, ROM, Logic, Display, and Interface) are individual. They are briefly described below. The sixth, named **All**, performs all five individual tests in sequence.

- **All** - all tests performed in sequence
- **RAM** - test of RAM memory
- **ROM** - test of ROM memory
- **Logic** - test of counter ASIC and other logic circuits.
- **Display** - test of graphic display module
- **Interface** - test of GPIB and USB

– Press **Start Test**.

– If a fault is detected, an error message appears on the display and the program halts. Note any error messages.

– If no faults are detected, the instrument returns to the normal measurement mode.

Keyboard Test

See Table 2-3. This test verifies that the timer/counter responds when you press any key. It is not a functional test. Such tests are performed later in this chapter. The important thing here is that something changes on the display when you press a key. Consequently you can press the keys in almost any order without paying attention to the exact response, but for those who want to be more systematic there is a table overleaf, where all keys are exercised at least once.

Press the keys as described in the first column and look at the display for the text in the second column. Some keys change more text on the display than described here. The display text mentioned here is the one mostly associated with the selected key.

NOTE: For the instrument to respond correctly, this test must be carried out in sequence and you must start with the DEFAULT setting. Do as follows:

– Press **USER OPT**.

– Press **Save/Recall**.

– Press **Recall Setup**.

– Press **Default**.

See Table 2-2 for the complete list of default settings.

PARAMETER	VALUE/SETTING
Input A & B	
Trigger Level	AUTO
Trigger Slope	POS
Impedance	1 MΩ
Attenuator	1x
Coupling	AC
Filter	OFF
Arming	
Start	OFF
Start Slope	POS
Start Arm Delay	200 µs
Stop	OFF
Stop Slope	POS
Hold-Off	
Hold-Off State	OFF
Hold-Off Time	200 µs
Time-Out	
Time-Out State	OFF
Time-Out Time	100 ms
Statistics	
Statistics	OFF
No. of Samples	100
No. of Bins	20
Pacing State	OFF
Pacing Time	20 ms
Mathematics	
Mathematics	OFF
Math Constants	K=1, L=0, M=1
Limits	
Limit State	OFF
Limit Mode	ABOVE
Lower Limit	0
Upper Limit	0
Burst	
Sync Delay	200 µs
Start Delay	200 µs
Meas. Time	200 µs
Freq. Limit	300 MHz
Miscellaneous	
Function	FREQ A
Meas. Time	200 ms
Smart Time Interval	OFF
Auto Trig Low Freq	100 Hz
Timebase Reference	INT

Table 2-2 *Default settings for functions and parameters.*

KEY(S)	DISPLAY	NOTES	P/F
STANDBY	**Off**	Red standby LED On (Key common to ON)	
ON	**Backlight On**	Red standby LED Off (Key common to STANDBY)	
INPUT A	**Input A:**	Menu for setting Slope, Coupling, Impedance etc.	
Man	**Trig xx mV**		
Trig	**Trig: xx mV**	Menu for entering numeric values	
0.123V	**Trig: 0.123 V**		
◀ (5 times)	**Trig: _ V**		
4.567	**Trig: 4.567 V**		
◀ (5 times)	**Trig: _ V**		
8.9	**Trig: 8.9 V**		
±	**Trig: -8.9 V**		
mV	**Trig: -8.9 mV**		
V	**Trig: -8.9 V**		
AUTOSET	**Menu** disappears		
INPUT B	**Input B:**	Menu for setting Slope, Coupling, Impedance etc.	
SETTINGS	**Settings:**	Menu for setting Meas Time, Hold-Off, Ref. Source etc.	
ENTER	**Meas Time: 200 ms**		
▲	**Meas Time: 500 ms**		
▼	**Meas Time: 200 ms**		
EXIT/OK	**Settings:**	Menu for setting Meas Time, Hold-Off, Ref. Source etc.	
EXIT/OK	**Menu** disappears		
MATH/LIM	**Math/Limit:**	Menu for selecting post-processing formula and alarm limit	
USER OPT	**User options:**	Menu for Calibration, Memory Management, Interface etc.	
CANCEL	**Menu** disappears		
HOLD/RUN	**Hold**	At upper right corner	
HOLD/RUN	**Hold** disappears		
MEAS FUNC	**Measure function:**	Menu for selecting measurement function	
▶	**Period**	Cursor position marked by text inversion	
ENTER	**Single A**		
EXIT/OK	**Menu** disappears	Period Single A: at upper left corner	
STAT/PLOT	**Period Single A MEAN:**	Aux parameters: Max, Min, P-P, Adev, Std	
VALUE	**Stat** parameters disappear		

Table 2-3 *Keyboard test.*

Short Form Specification Test

Sensitivity and Frequency Range

– Recall the DEFAULT settings.
– Press **INPUT A**.
– Select **50** Ω input impedance, **1x** attenuation, **MAN**ual trigger and **Trig**ger level **0 V**.
– Connect a signal from a HF generator to a BNC power splitter.
– Connect the power splitter to Input A of your counter and an oscilloscope.
– Set the input impedance to 50 Ω on the oscilloscope.
– Adjust the amplitude according to the following table. Read the level on the oscilloscope. The timer/counter should display the correct frequency.
– Connect the signal to Input B.
– Press **INPUT B**.
– Select **50** Ω input impedance, **1x** attenuation, **MAN**ual trigger and **Trig**ger level **0 V**.
– Press **MEAS FUNC → Freq → Freq A →B**
– Repeat the measurements above for Input B.

Frequency (MHz)	Level		Pass/Fail	
	mV_{rms}	dBm	Input A	Input B
10	15	–23		
50	15	–23		
100	15	–23		
200	15	–23		
300	25	–19		

Table 2-5 *Sensitivity for inputs A & B at various frequencies*

Voltage

– Recall the DEFAULT settings.
– Press **MEAS FUNC → Volt → Vpp → A**
– Press **INPUT A** and select **DC** coupling. Do not apply an input signal to Input A yet.
– Press **EXIT/OK**.
– The display should now indicate (disregard the main parameter V_{PP}):
V_{MIN} = 0 ± 0.015 V and
V_{MAX} = 0 ± 0.015 V
– Adjust the current limit of the voltage source to <200 mA.
– Connect +2.500 V_{DC} to Channel A, using the external low-pass filter on the input.
– The display should now indicate:
V_{MIN} = 2.500 ± 0.040 V and
V_{MAX} = 2.500 ± 0.040 V
– Repeat the measurement with inverted polarity.
– Press **INPUT A** and select **10x**.
– Press **EXIT/OK**.

CAUTION: Before the next step, make sure the input impedance is still 1 MΩ. Applying more than 12 V without proper current limiting may cause extensive damage to the main PCB, if the impedance is set to 50 Ω.

– Change the DC level to +50.00 V.
– The display should now indicate:
V_{MIN} = 50.00 ± 0.65 V and
V_{MAX} = 50.00 ± 0.65 V
– Repeat the measurement with inverted polarity.
– Disconnect the DC voltage from Channel A.
– Remove the external low-pass filter.
– Press **INPUT A** and select **1x**.
– Press **EXIT/OK**.
– Connect a sinusoidal signal to Input A with an amplitude of 4.000 Vpp and a frequency of 100 kHz.
– The display should now indicate: 4.000 ± 0.150 V_{PP}.
– Press **INPUT A** and select **10x**.
– Press **EXIT/OK**.
– Change the amplitude to 18.00 V_{PP}.
– The display should now indicate:
18.00 ± 0.84 V_{PP}.
– Disconnect the signal from Channel A.
– Press **MEAS FUNC → Volt → Vpp →B**
– Press **INPUT B** and select **DC** coupling. Do not apply an input signal to Input B yet.
– Press **EXIT/OK**.
– The display should now indicate
(disregard the main parameter V_{PP}):
V_{MIN} = 0 ± 0.015 V and
V_{MAX} = 0 ± 0.015 V
– Proceed by repeating the measurements for Input B as described above for Input A.

Trigger Indicators vs. Trigger Levels

Trigger Level (manually set)	Trigger Indicator	Pass	
		Input A	Input B
+1 V	off		
-1 V	on		
0.0 V	blinking		

Table 2-4 *Trigger indicator check.*

NOTE: This test must be performed in the sequence given.

– Recall the DEFAULT settings.

– Press **INPUT A** and select **MAN**ual trigger level and **50** Ω input impedance.

– Connect the LF synthesizer to Input A. Use the following settings (into 50 Ω):
Sine, 10 kHz, 0.9 V_{PP}, and +0.50 V_{DC}.

– Verify that the three modes for the trigger indicator are working properly by changing the trigger level:
  – Press the **Trig** key and enter +1 V via the keyboard, then verify by pressing **EXIT/OK.** Check the trigger indicator according to Table 2-4.
  – Press the **Trig** key and enter –1 V via the keyboard by pressing the **±** key, then verify by pressing **EXIT/OK**. Check the trigger indicator according to Table 2-4.
  – Press the **Trig** key and enter 0 via the keyboard, then verify by pressing **EXIT/OK**. Check the trigger indicator according to Table 2-4.

– Apply the signal to Input B instead.

– Press **MEAS FUNC → Freq → Freq (A) → B**

– Press **INPUT B** and select **MAN**ual trigger level and **50** Ω input impedance..

– Repeat the trigger level settings above to verify the three trigger indicator modes for Input B.

Input Controls

– Recall the DEFAULT settings.

– Connect the LF synthesizer to Input A. Use the same settings as in the previous test.

– Press **INPUT A** and select **DC** and **50** Ω.

– Press **EXIT/OK**.

– Check the V_{max} and V_{min} voltage levels on the display according to the first row in Table 2-6.

– Perform the rest of the settings in sequence, and read the corresponding V_{max} and V_{min} values. Remember that all these values are approximate and serve only as indicators of state changes.

Settings	V_{max}	V_{min}	Pass/Fail	
			Input A	Input B
INPUT A, DC, 50 Ω	+950 mV	+50 mV		
AC	+450 mV	-450 mV		
10X	+0.45 V	-0.45 V		
1 MΩ	>+0.45 V	<-0.45 V		

Table 2-6 *Input controls check.*

– Connect the generator to Input B.

– Press **MEAS FUNC → Freq → Freq (A) → B**

– Press **INPUT B** and select **DC** and **50** Ω.

– Press **EXIT/OK**.

– Check the V_{max} and V_{min} voltage levels on the display according to the first row in Table 2-6.

– Perform the rest of the settings in sequence, and read the corresponding V_{max} and V_{min} values.

Reference Oscillators

X-tal oscillators are affected by a number of external conditions like ambient temperature and supply voltage. Aging is also an important factor. Therefore it is hard to give limits for the allowed frequency deviation. The user himself must decide the limits depending on his application, and recalibrate the oscillator accordingly.

To check the accuracy of the oscillator you must have a calibrated reference signal that is at least five times more stable than the oscillator that you are testing. See Table 2-7 and the list of test equipment on page 2-2. If you use a non-10 MHz reference, you can use the mathematics in the timer/counter to multiply the reading.

– Recall the DEFAULT settings. See page 2-2

– Connect the reference to input A

– Check the readout against the accuracy requirements of your application.

■ Acceptance Test

Oscillator	Frequency Readout	Suitable Reference	P/F
Standard (PM6690/_1_)	10.00000000 MHz ± 150 Hz	908	
OCXO (PM6690/_5_)	10.00000000 MHz ± 1 Hz	909	
OCXO (PM6690/_6_)	10.00000000 MHz ± 0.25 Hz	909	

Table 2-7 *Acceptance test for oscillators.*

Table 2-7 can serve as an acceptance test and gives a worst case figure after 30 minutes warm-up time. All deviations that can occur in a year are added together.

Resolution Test

– Connect the pulse generator to a power splitter.

– Connect one side of the power splitter to Input A on the counter using a coaxial cable.

– Connect the other side of the power splitter to Input B on the counter.

Settings for the pulse generator:

– Amplitude = 2 V_{PP}, (high level +2V and low level 0 V)

– Period = approx. 1 µs

– Duration = approx. 50 ns

– Rise time = 2 ns

Restore the timer/counter's default settings and make the following changes:

– Function = **Time A-B**

– Press **STAT/PLOT** key to the right of the display.

– Settings for **INPUT A** and **INPUT B**:

50 Ω input impedance

MANual trigger level

Selected Function	Action	Display	P/F
FREQ A		10 MHz 2)	
FREQ B		10 MHz 2)	
FREQ C		- - - - - - - - - - - - - - 3)	
FREQ RATIO A/B		1.0000000	
FREQ RATIO C/B		0.0000000 3)	
PER SINGLE A		100 ns 2)	
PER SINGLE B		100 ns 2)	
PER AVERAGE A		100 ns 2)	
PER AVERAGE B		100 ns 2)	
PULSE POS A		50.000 ns 1)	
PULSE NEG A		50.000 ns 1)	
TIME INT A to B		0 ± 1 ns	
	Select NEG SLOPE B	50.000 ns 1)	
RISE TIME A	Select AUTO trigger	30.000 ns 2)	
FALL TIME A		30.000 ns 2)	
PHASE A rel B		180° or -180° 1)	
PHASE B rel A		180° or -180° 1)	
PHASE A rel A		0°	
DUTY POS A		0.500000 1)	
DUTY NEG A		0.500000 1)	
VOLT MAX A		+0.75 V 2)	
VOLT MIN A		-0.75 V 2)	

Table 2-8 *Measuring functions check*
1) Value depends on the symmetry of the signal.
2) Exact value depends on input signal.
3) If an RF option is installed.

Trig level = 0.5V

DC coupling

The standard deviation (**Std**) should be <100 ps.

Rear Inputs/Outputs

10 MHz OUT

– Connect an oscilloscope to the 10 MHz output on the rear of the counter. Use a coaxial cable and 50 Ω termination.

– The output voltage should be sinusoidal and above 1 V_{RMS} (2.8 V_{p-p}).

EXT REF FREQ INPUT

– Recall the DEFAULT settings.

– Connect a stable 10 MHz signal (e.g REF OUT from another counter) to input A.

– Connect a 10 MHz, 100 mV_{RMS}, (0.28 V_{P-P}) signal from the LF synthesizer to EXT REF IN.

– Select Ext Ref. by keying in the following sequence:
SETTINGS → Timebase Ref → Ext

– The display should show 10 MHz.

– Change the external reference frequency to 5 and 1 MHz.

– The counting should continue, and the display should still show 10 MHz.

EXT ARM INPUT

– Proceed from the test above.

– Select **MAN**ual trigger.

– Settings for the pulse generator:
single shot pulse, manual trigger,
amplitude TTL = 0 - 2 V_{PP}, and
duration = 10 ns.

– Connect the pulse generator to Ext Arm Input.

– Activate start arming by keying in the following sequence:
SETTINGS → Start Chan → E

– The counter does not measure.

– Apply one single pulse to Ext Arm Input.

– The counter measures once and shows 10 MHz on the display.

Measuring Functions

– Connect a 10 MHz sine wave signal with approx. 1 V_{RMS} amplitude into 50 Ω via a power splitter to Input A and Input B, e.g. from 10 MHz Out on the rear panel.

– Recall the DEFAULT settings.

Select the following settings for the timer/counter via **INPUT A** and **INPUT B**:

– **50** Ω impedance for A and B.

– **MAN**ual trigger.

– Check that the timer/counter performs the correct measurement by displaying the result as shown under the "Display" column in Table 2-8.
– Select function via **MEAS FUNC**

Check of HOLD OFF Function

– Recall the DEFAULT settings.
– Select **Period Single A**.

Select the following common timer/counter settings for both Input A and Input B via the hard menu keys **INPUT A** and **INPUT B**:

– **50** Ω impedance.
– **DC** coupling.
– **MAN**ual trigger, **x1** attenuation.
– Press **SETTINGS** and activate **Hold Off**. Select **Hold Off On** and set the **Trigger Hold Off** time to the minimum value 20 ns.
– Connect the rear panel output marked 10 MHz OUT to Input A.
– Increase the **Trigger Hold Off** time in steps by means of the **UP** cursor key and note the results:

If Trigger Hold Off time <100 ns the result is about 100 ns, i.e. the same value as without Hold Off.

If Trigger Hold Off time >100 ns the result is about 100 ns + Trig Hold Off time.

– Connect the signal to Input B, select **Period Single B** and repeat the tests above.

RF Options

Input C Check

To verify the specification of the different RF prescalers (Input C), use the following basic test setup:

– Connect the output of a signal generator covering the specified frequency range to the RF input of the counter.
– Connect the 10 MHz REF OUT from the generator to the EXT REF IN on the rear panel of the counter.
– Choose **Meas Ref** from the **SETTINGS** menu and select **External**.
– Choose **Freq C** from the **MEAS FUNC** menu.
– Generate a sine wave in accordance with the tables.
– Verify that the counter is counting correctly. (The last digits will be unstable)

Frequency	**Amplitude**		**P/F**
MHz	mV_{RMS}	dBm	
100-300	20	-21	
300-2500	10	-27	
2500-2700	20	-21	
2700-3000	40	-15	

Table 2-9 *RF input sensitivity, 3 GHz Option.*

Frequency	Amplitude		P/F
MHz	mV_{RMS}	dBm	
300-500	20	-21	
500-3000	10	-27	
3000-4500	20	-21	
4500-6000	40	-15	
6000-8000	80	-9	

Table 2-10 *RF input sensitivity, 8 GHz Option.*

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Chapter 3

Disassembly

The terms in the following figure are used in all descriptions in this manual.

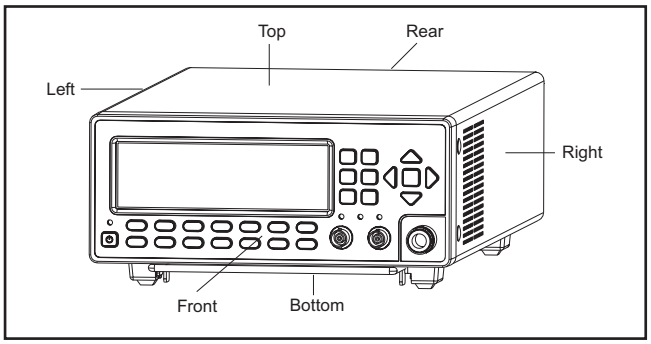

Figure 3-1 *Terms used in this manual.*

The PM6690 can be equipped with a number of options and accessories. Built-in timebase and prescaler options can be identified by pressing **USER OPT → About** on the front panel.

The following built-in options exist or are planned:

– Option PM6690/6__ 3 GHz RF Prescaler Input
– Option PM6690/7__ 8 GHz RF Prescaler Input
– Option PM6690/_5_ Very High Stability OCXO
– Option PM6690/_6_ Ultra-High Stability OCXO

The location of these optional parts is illustrated in Fig. 3-2 and Fig 3-3.

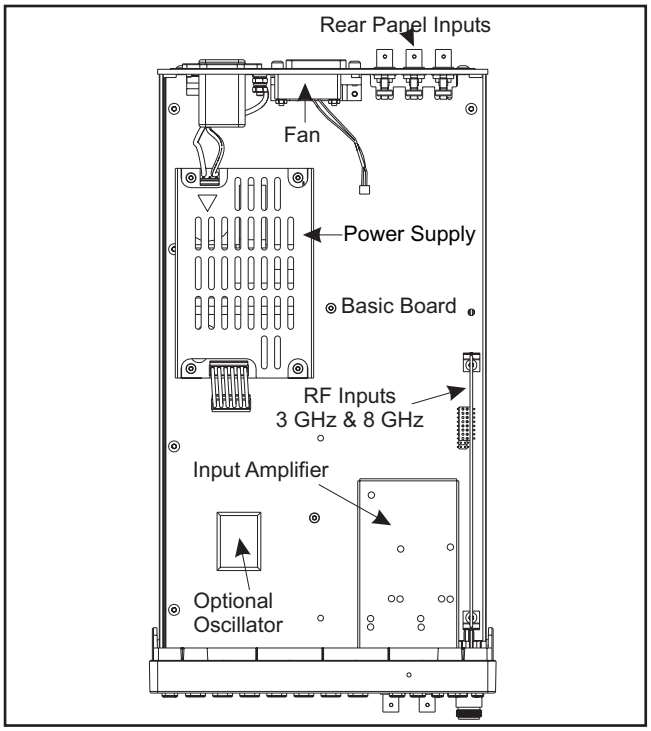

Figure 3-2 *Interior layout including 3 GHz or 8 GHz prescaler option.*

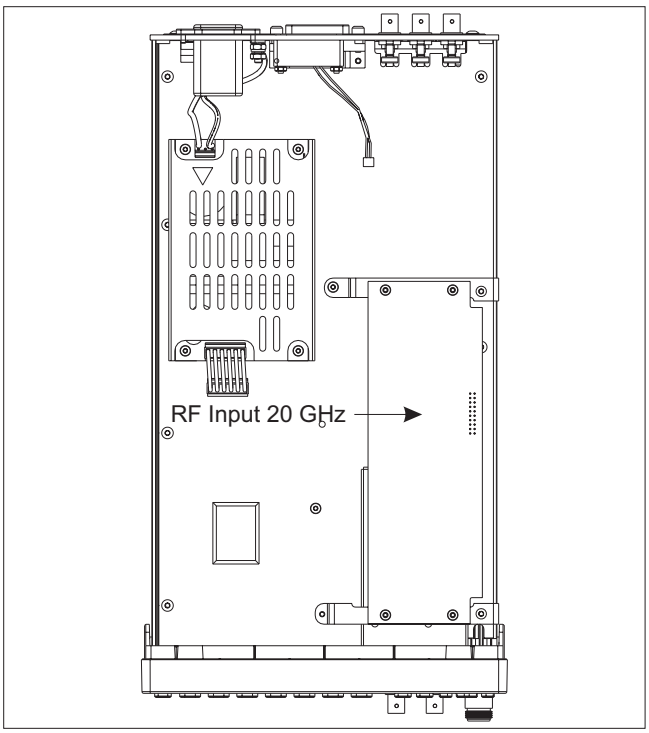

Figure 3-3 *Interior layout with 20 GHz prescaler option.*

Removing the Cover

WARNING: Do not perform any internal service or adjustment of this instrument unless you are qualifyed to do so.

WARNING: When you remove the cover you will expose live parts and accessible terminals which can cause death.

WARNING: Although the power switch is in the OFF position, line voltage is present inside the instrument. Use extreme caution.

WARNING: Capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

– Make sure the power cord is disconnected from the counter.
– Turn the counter upside down.
– Remove the two screws at the bottom and the two screws in the rear feet.
– Remove the four decorative plugs (C) that cover the four screw holes on the right and left side of the front panel.
– Grip the front panel and gently push at the rear.

– Pull the interior unit out of the cover.

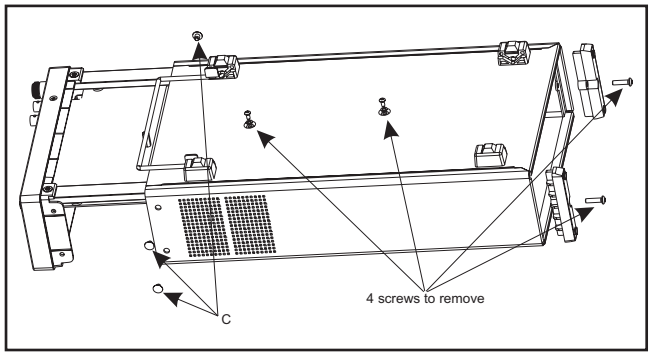

Figure 3-5 *Remove the screws and pull out the main PCB.*

Reinstalling the Cover

– Push the counter gently back into the cover.
– Turn it upside down
– Fit the two screws at the bottom.
– Fit the two rear feet with their screws to the rear panel.
– Fit the four decorative plugs.

Fan

– Disconnect the power cable.
– Remove the cover from the counter. See page 3-2.
– Remove the four screws, nuts and washers that fix the fan to the rear panel.
– Disconnect the fan power supply connector from the main PCB and remove the fan.
– When reinstalling the fan, make sure the air-flow arrow on the fan points to the rear of the counter and the black wire is oriented toward the rear panel.

Prescaler Options

– Disconnect the power cable.
– Remove the cover from the counter. See page 3-2.
– Disconnect the cable from the mini-coax connector on the RF input.
– Press the clips apart and lift the RF input PCA straight up and out.
– When installing the RF input, make sure the connector pins fit exactly in the holes of the connector housing.

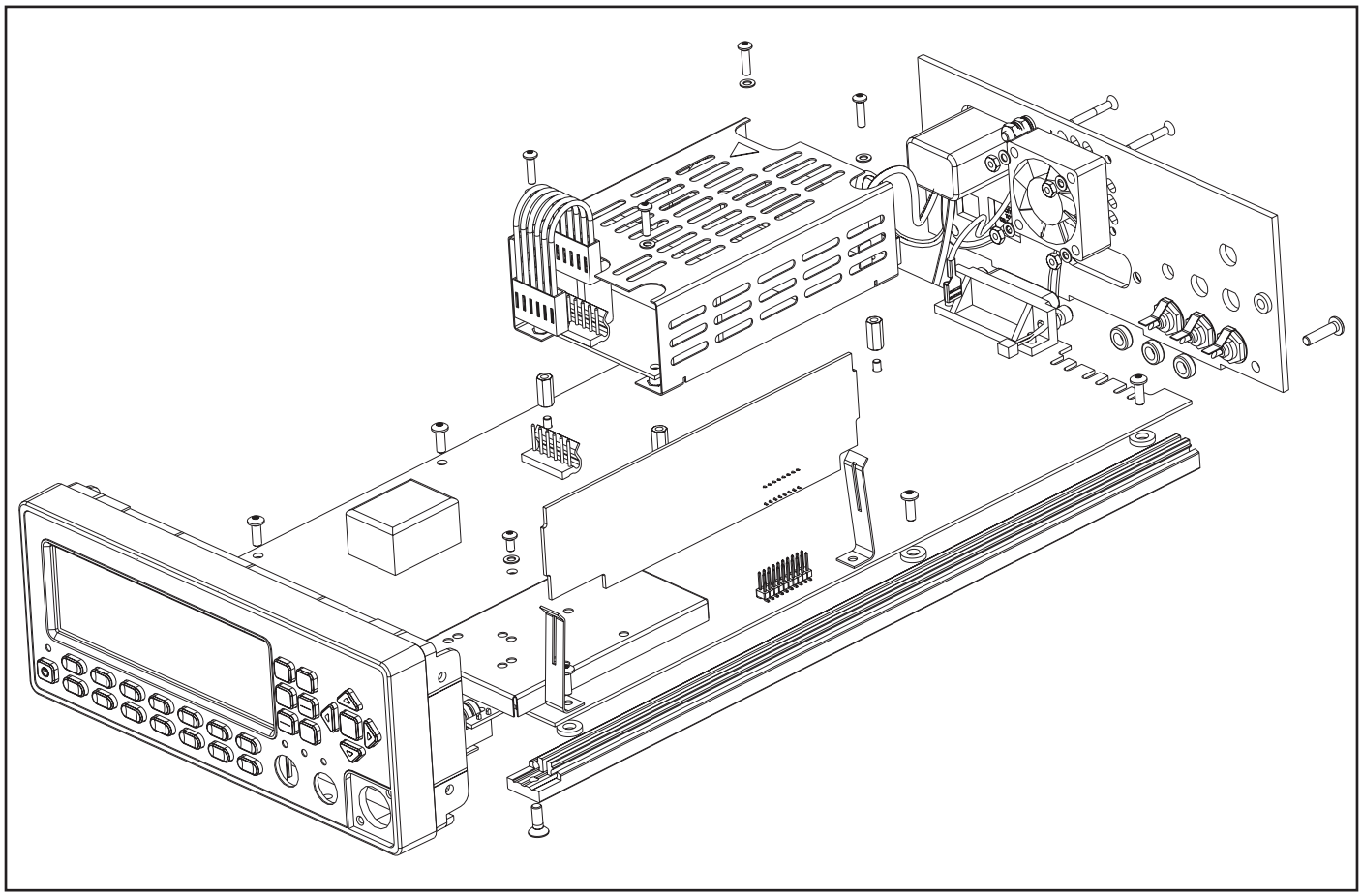

Figure 3-4 *The fan is fixed with four screws and nuts. The 3 GHz & 8 GHz prescalers are fixed with snap-in clips. The OCXO is soldered to the main board.*

– Reconnect the RF input cable.

OCXO Options

– Disconnect the power cable.
– Remove the cover from the counter. See page 3-2.
– Turn the instrument upside down.
– Locate the five solder joints and remove the OCXO with conventional desoldering technique for plated-through holes.

Chapter 4

Circuit Descriptions

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Version A

The descriptions in this section apply to instruments having a Triscend microprocessor.

See General Information on page III for details on relevant serial numbers etc.

Block Diagram Description

General

The PM6690 Timer/Counter consists of three main units:

– Front unit

– Main printed circuit board

– Rear panel unit

Several options exist:

– Prescalers on separate PCBs covering different frequency ranges (3 GHz and 8 GHz)

– Two OCXO timebases (very high & ultra-high stability)

– Rackmount kit

The chassis of the counter consists of a front piece molded in aluminum, an aluminum rear panel, and two extruded aluminum bars that hold the front and rear panels together. This unit can be slid into the aluminum cover of the instrument.

The main circuit board is fixed to the two bars. The display circuit board is fixed to the front piece. A detachable connector joins the electronics of the front unit and the main board, and the molded front piece is fixed with screws to the two aluminum bars. The rear panel is also fixed to the bars with screws.

The front unit contains all functions needed for the user communication: keyboard, display and input BNCs. All other electrical functions are on the main board. The rear panel has no PCB. The connectors here are all soldered directly to the main circuit board.

Block Diagram

Figure 4-1 contains a block diagram of the electrical functions of the counter. They are divided among the main circuit board, the display board, the rear panel and the optional prescaler board. See the schematic diagrams in Chapter 9 for complete information.

Most functions are placed on the main board:

– Input amplifiers with trigger level circuits

– Power supply

– Measurement logic

– Microcomputer circuitry

– GPIB interface

– USB interface

– External reference input

– External arming input

The rear panel unit is made of aluminum with a number of mounted connectors, a fan and a power line inlet with filter. Most connectors are soldered directly to the main board.

NOTE: Schematic diagrams in this chapter are simplified. For complete information, see Chapter 9.

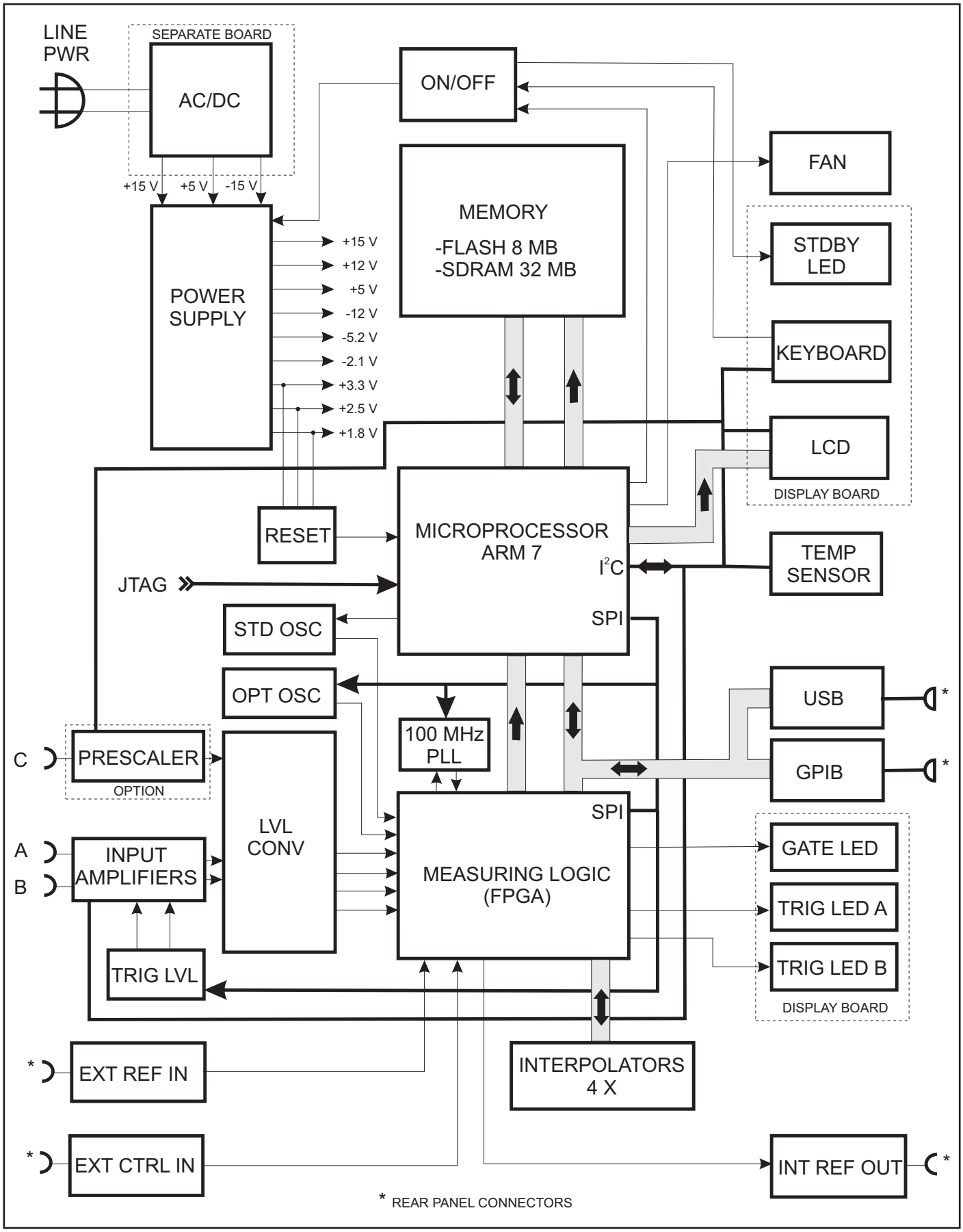

Figure 4-1 *Block diagram of the '90'.*

Hardware Functional Description

Front Unit

The front unit consists of a front piece in molded aluminum, a silicon rubber keypad with conducting contact surfaces, a graphic LCD with LED backlight, and a PCB having etched gold-plated keyboard contacts and a dedicated LCD power supply.

Display

The display is a 320*97 pixels graphical LCD with LED backlight. The LCD controller is part of the processor, and it sends data and control signals to the drivers in the LCD module. Display ON is controlled via the I^2C bus and the keyboard IC. The LCD voltages are generated by a DC/DC converter. Five different voltages are generated. A control signal from the processor switches the converter ON/OFF and also sets the contrast of the display.

The 4 LEDs on the display board are controlled from the measuring logic and the ON/OFF circuit.

Keyboard

The PCB covers the back of the front unit. The keys are laid out as a crosspoint switch matrix consisting of 25 regular push buttons plus a special power button. When one of the buttons is depressed, the dedicated keyboard IC U3 responds by sending an interrupt to the processor. The processor scans the keyboard over the I^2C bus to find out which button calls for attention. The power button differs from the others by having a dual function. In *Standby Mode* it turns on the ON/OFF circuit directly, but when the counter is ON, it is read as any other button. Then the processor turns off the counter. This arrangement is necessary since the processor is inactive in standby mode.

Main Board

Input Amplifiers

Input amplifiers A and B are identical with >300 MHz bandwidth. They are controlled by the processor with relays etc. The analog input signal is transformed to a digital signal. The output signals are LVPECL (+2.4 V and +1.2 V approximately) and fed to the measuring logic.

For a block diagram of the input amplifiers, see Figure 4-2.

■ Impedance Selector

This stage selects 1 MΩ or 50 Ω input impedance with a relay. In 50 Ω mode 11 resistors are used for dissipating the input power, up to a maximum of 2.9 W (12 V_{rms}).

■ Attenuator

This stage has two parts, a fixed preattenuator (approximate attenuation 2.5×) and a cascaded relay-operated 1×/10× step attenuator. The variable capacitors are used for adjusting the frequency response of the attenuators.

■ AC/DC

This stage selects AC or DC coupling with a relay.

■ Limiter

The voltage limiter protects the impedance converter against overvoltage. The ±5 V applied to the input BNC is divided to approximately ±2.1 V by the attenuator. The limiter clamps the voltage to approximately ±2.8 V.

■ Impedance Converter

Split-band technique is used for achieving good frequency response over a wide range. The HF signal is fed via an AC-coupled FET stage. The LF signal (bandwidth DC to approximately 10 kHz) goes via an operational amplifier. The signals are added together at the source of the FET. The output signal from the buffer stage (see below) is fed back to the operational amplifier. A trimmer potentiometer is used for equalizing the gain in the two signal paths (approximately ×0.9).

■ Filter

A lowpass RC filter with an approximate cutoff frequency of 100 kHz can be switched in via a transistor.

■ Buffer

Before the signal is fed to the *Crossover Switch*, it passes a current-amplifying buffer stage that can drive the following low impedance stages.

■ Crossover Switch

This stage uses relays to direct the signal to the two comparators. The following combinations are possible:

- IN A to COMP A and IN B to COMP B
- IN A to both COMP A and COMP B
- IN B to both COMP A and COMP B

■ Comparator

The comparator converts the analog signal to a binary logic signal, with ECL levels (-0.9 V and –1.7 V). The trigger point is set by a voltage from the trigger level circuitry. Temperature-compensated circuitry generates the voltages that control the hysteresis of the comparator. A trimmer potentiometer adjusts the hysteresis window.

■ Trigger Level Generation

Two 12-bit DACs in a single IC generate the two trigger levels for Channel A resp. Channel B. A 2.5 V DC reference IC supplies the reference voltage to the DACs. The DACs are controlled by the processor over the SPI bus. The ±5 V dynamic range at the BNC of the input amplifier is converted to approximately ±2.1 V at the comparator. This range must be covered by the DAC. The voltage step from the DAC is approximately 1.2 mV, corresponding to 2.9 mV per step at the BNC. *Closed Case Calibration* (CCC) is used for adjusting the trigger levels. A known reference level is applied to the BNC and the processor finds out the appropriate setting of the DAC to match the reference level.

■ Logic Level Conversion

The signals from the comparators must be converted from ECL levels to LVPECL levels. There are three converter circuits. One for Channel A , one for Channel B and one for the Set-Reset channel. The two main channels are fed to a Set-Reset flip-flop to make one-channel measurements with variable hysteresis possible. There is also a converter for the signal from an optional prescaler. It has PECL levels (+4.1 V and +3.4 V) that are converted to LVTTL levels (+2.4 V and 0 V).

Oscillator Circuits

The processor has a 32768 Hz crystal. An internal PLL in the processor uses the 32 kHz signal to make the internal processor clock, approximately 30 MHz. The USB IC has a 6 MHz crystal to make an internal clock and the GPIB IC has a 40 MHz crystal to make an internal clock.

The measurement reference oscillator (timebase) for the timer/counter is a 10 MHz crystal oscillator or an optional oven-controlled crystal oscillator (OCXO). Only one of these is mounted. The user can also select an external reference signal, connected to the *External Reference Input* BNC on the rear panel.

The standard oscillator consists of an inverter and a crystal. The processor controls the frequency of the oscillator with a PWM signal. The PWM signal is filtered to a DC level that controls the capacitance of a capacitance diode. The varying capacitance changes the frequency of the oscillator. The standard oscillator is adjusted with *Closed Case Calibration*. Apply a 10 MHz reference signal to Input A. The processor will find the correct PWM signal to make the internal reference frequency equal to the external reference frequency.

The optional oven-controlled oscillator is a complete oscillator in a small hermetic metal box. An internal accurate DC voltage is available for use as a reference for a 12-bit DAC. The filtered output voltage from the DAC sets the frequency of the oven oscillator. The processor controls the DAC via the SPI bus. The same *Closed Case Calibration* as for the standard oscillator is used. The oven oscillator is kept warm if the line power is connected to the timer/counter, even if it is switched off (in standby mode).

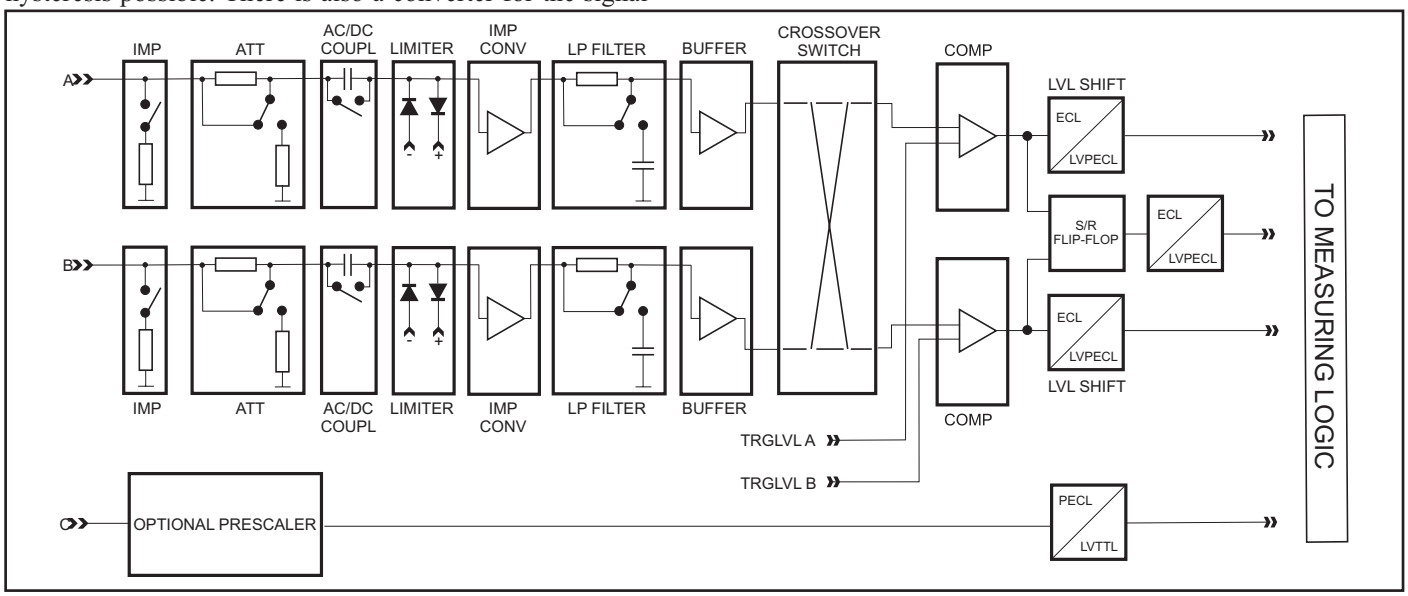

Figure 4-2 *Input amplifier block diagram.*

The 10 MHz reference signal is multiplied in a PLL to 100 MHz. The 100 MHz signal is used in the measuring logic as a reference. The processor controls the PLL IC with the SPI bus. A 100 MHz LC oscillator is used as the controlled element where part of the C is a variable capacitance diode. Its capacitance is controlled with a DC voltage from the PLL IC, thus changing the frequency. The 10 MHz reference signal is applied to the PLL IC as its reference and the 100 MHz output frequency is exactly 10 times the reference frequency.

External Reference Input

A 1, 2, 5 or 10 MHz reference signal can be connected to the rear panel BNC. After amplification in an operational amplifier narrow pulses are made in two D flip-flops, one narrow pulse for each input cycle. These pulses are fed to the 10 MHz crystal filter. After the filter a reconstructed 10 MHz signal is available. A variable capacitor is used for adjusting the filter.

Internal Reference Output

The selected 10 MHz reference signal (standard/oven oscillator or external reference) is available on the rear panel. The 10 MHz reference signal that is used internally by the dedicated counter circuit (FPGA) logic is also sent to an output pin on the FPGA. It is filtered to a sine wave and amplified in an output buffer stage having 50 Ω drive capability.

Measuring Logic

The measuring logic consists of an FPGA, four interpolators and an external control input on the rear panel. The FPGA core uses +1.8 V supply voltage and the I/Os use +3.3 V supply voltage.

The FPGA is controlled by the processor over a 16-bit microprocessor bus. Input signals (A, B, prescaler etc) and reference clock (internal 10 MHz oscillator or external reference) are selected inside the FPGA. The logic for all measuring functions and support functions (trigger indicators, start delay, pacing etc) are inside the FPGA. A 100 MHz reference clock is generated by a PLL circuit giving 10 ns basic measurement resolution. To increase the measurement resolution further, external interpolators are used. The measuring logic also controls three LEDs on the display board; a GATE LED indicating that a measurement is in progress, and two trigger indicators telling that the comparators are triggering on the input signals. A separate 32-bit bus is used for transferring measurement data from the FPGA to the processor. Some control signals to the hardware come from the FPGA due to a shortage of processor pins.

The four external interpolators are identical. Depending on the selected measurement function 0, 2, 3 or 4 interpolators are used. A pulse representing the time from an event on the input to the following rising edge of the 100 MHz reference is fed to the interpolator. During the pulse time a constant current is charging a capacitor. The voltage on the capacitor is measured with a 10-bit ADC. The capacitor is discharged and the interpolator is ready for a new measurement.

An external control input BNC is located on the rear panel. A signal applied to this connector can be used for controlling the start of a measurement, for instance. A comparator converts the analog input signal to a logic signal.

Processor Circuits

The processor is a Triscend A7S. It contains an ARM7 core and peripherals. It runs on a 30 MHz internal clock. The core uses 2.5 V supply voltage and the I/Os use 3.3 V supply voltage.

A separate memory bus communicates with a 16-bit 8 MByte flash memory and a 32-bit 32 MByte SDRAM. The flash memory contains the program, data for loading the FPGA, and stored data (calibration data etc.). At power-up the code is copied from the flash to the SDRAM. It is run from the SDRAM for faster execution.

The processor has a JTAG interface with a connector on the circuit board.

A reset IC monitors the three main logic supply voltages, +3.3 V, +2.5 V and + 1.8 V. If a supply voltage fails, the processor will be reset.

The regular 16-bit microprocessor bus is used for controlling the FPGA, the GPIB interface and the USB interface. A separate 32-bit bus is used for fetching measurement data from the measuring logic.

Two other buses are also used, an SPI bus and an I^2C bus. The SPI bus is an *output only* bus and the processor controls the 100 MHz PLL, the trigger level DACs, and the DAC for the optional oven oscillator. The I^2C bus is bidirectional and used for communication with the temperature measurement IC, the display board (keyboard + LCD), the prescaler (optional), and the relays and filters in the input amplifier.

The temperature reading over the I^2C bus is used for controlling the fan speed. A PWM output is utilized. The signal is filtered and the resulting DC voltage controls the fan.

Another PWM output is used for controlling the frequency of the standard crystal oscillator.

The LCD controller is a peripheral inside the processor. This controller sends signals and data to the driver circuits in the LCD on the display board.

The processor also controls the OFF switch. Only a signal from the processor can switch off the power. The OFF button on the front panel is read by the processor. ON is handled without the processor, since it cannot respond to external stimulus in standby mode.

Power Supply

This timer/counter has no primary power switch. If connected to line power there are live parts inside the cabinet, and some supply voltages are present on the main circuit board, even if

the secondary power switch on the front panel has been turned off (standby mode).

A semi-protected AC/DC module is placed on spacers over the main circuit board. It delivers three regulated DC voltages to the counter, + 15 V, + 5 V and –15 V. When the counter is connected to line power, these voltages are always present. There is a + 5 V trimmer potentiometer on the AC/DC module.

The ON/OFF circuit is active as soon as the counter is connected to line power. The instrument automatically powers up when line power is applied. Only the processor can switch the circuit to OFF state (standby mode). Then only the power button on the front panel can switch the instrument to ON. Once connected to line power and in OFF state (standby mode), supply voltage +12 VU is distributed to the oven oscillator to keep it warm. In standby mode a red LED is lit on the front panel. To keep the AC/DC module stable in this mode, a dummy load is connected to draw a quiescent current of 0.1 A at +5 V.

The three main voltages are +15 V, +5 V and –15 V from the AC/DC module. All other supply voltages are generated from them and are, except for +12 VU to the oven oscillator, switched off in standby mode.

Linear regulators are used for generating stable voltages with low noise and without spikes. Some of them have a resistor net at the input to dissipate part of the heat generated. Thus the regulator itself will run cooler. The following voltages are generated in this way:

+3.3 VA from +5 VU
-5.2 VA from -15 VU
-5.2 VI from -12 VA
-2.1 V from -12 VA
-12 VA from -15 VU
+12 VA from +15 VU
+12 VU from + 15 VU, to oven oscillator, not switched off in standby mode

For digital and general use supply voltages are generated by DC/DC converters:

+3.3 VD from +5 VU
+5 VD from +5 VU via a switch IC
+15 VD from +15 VU via a switch transistor
+2.5 V from +5 VU
+1.8 V from +5 VU

Communication Interfaces

Both a GPIB and a USB interface are available for communication with external bus controllers. The connectors are located on the rear panel.

The GPIB consists of an IC. Only 8 bits of the 16-bit microprocessor bus is used. Due to different supply voltages for the processor (+3.3 V) and the GPIB circuit (+5 V), a buffer IC is used for isolating the +5 V GPIB IC from the processor bus. A 40 MHz crystal is used for generating a local clock.

The USB consists of an IC. It communicates with the processor over the 16-bit microprocessor bus. A 6 MHz crystal is used for generating a local clock.

Rear Panel Unit

The rear panel is made of aluminum. A number of connectors mounted on this unit are accessible to the user, see Figure 4-3.

I/O:

– GPIB communication connector.
– USB communication connector

INPUTS:

– External reference (BNC)
– External arming (BNC)
– Power supply inlet including EMI filter

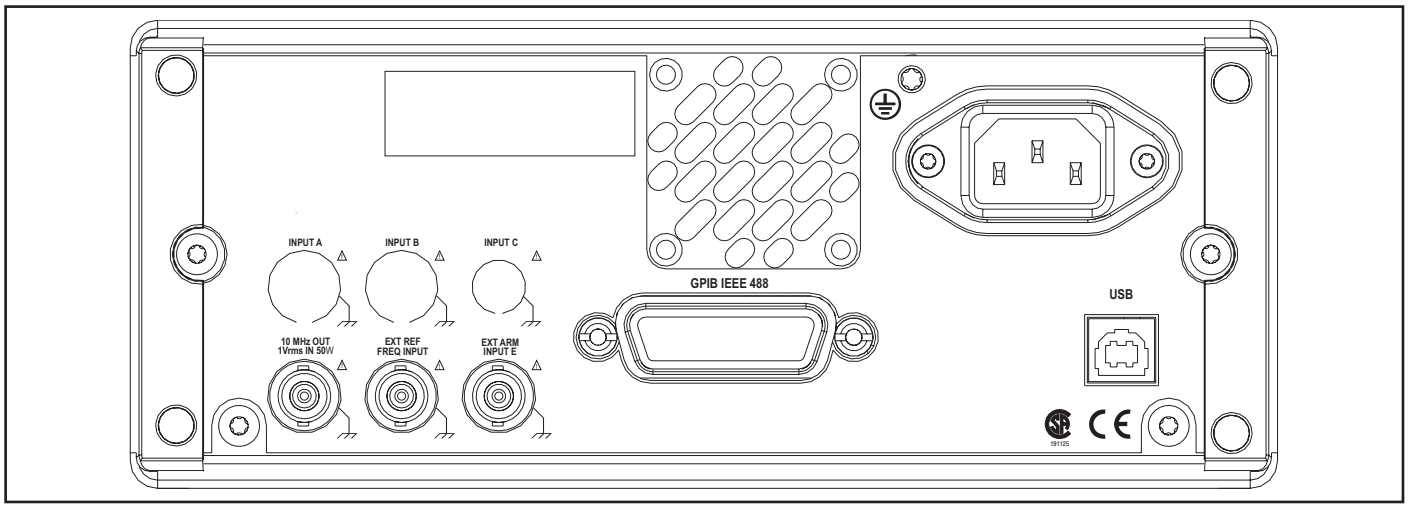

Figure 4-3 *Rear panel, PM6690.*

– Optional main inputs replacing corresponding front panel inputs

OUTPUTS:

– Internal reference 10 MHz (BNC)

Prescaler Circuit Board

There are several different optional prescalers available with different frequency ranges. The prescaler is located on a separate circuit board that is connected to the main circuit board with a PCB connector.

A typical prescaler consists of a limiter, an amplifier, a frequency divider, and a detector. The limiter and the amplifier condition the input signal so that the amplitude to the divider is constant. The divider scales the input signal so that it can be handled by the measuring logic on the main circuit board. A detector switches off the output signal from the divider if the input level is too low for the divider to work correctly (dividers often oscillate without input signal).

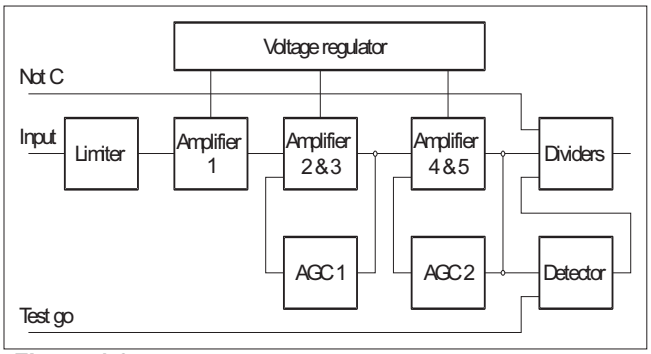

Figure 4-6 *Typical prescaler option, block diagram*

Test Routines

Built-in Test Routines

The test routines are those accessible via the USER OPT key.

– Press USER OPT → Test → Test Mode

– Choose one of the five alternatives:

1. All - Perform the four basic tests below in sequence
2. Memory - Test RAM and ROM
3. Logic - Test measuring logic circuits
4. Display - Test the graphic LCD display
5. Interface - Test the two standard interfaces, GPIB and USB

Power-On Tests

Certain tests are automatically performed at power-up. Errors, if any, are reported on the display.

Version B

The descriptions in this section apply to instruments having a Sharp microprocessor.

See General Information on page III for details on relevant serial numbers etc.

Block Diagram Description

General

The PM6690 Timer/Counter consists of three main units:

– Front unit
– Main printed circuit board
– Rear panel unit

Several options exist:

– Prescalers on separate PCBs covering different frequency ranges (3 GHz and 8 GHz)
– Two OCXO timebases (very high & ultra-high stability)
– Rackmount kit

The chassis of the counter consists of a front piece molded in aluminum, an aluminum rear panel, and two extruded aluminum bars that hold the front and rear panels together. This unit can be slid into the aluminum cover of the instrument.

The main circuit board is fixed to the two bars. The display circuit board is fixed to the front piece. A detachable connector joins the electronics of the front unit and the main board, and the molded front piece is fixed with screws to the two aluminum bars. The rear panel is also fixed to the bars with screws.

The front unit contains all functions needed for the user communication: keyboard, display and input BNCs. All other electrical functions are on the main board. The rear panel has no PCB. The connectors here are all soldered directly to the main circuit board.

Block Diagram

Figure 4-7 contains a block diagram of the electrical functions of the counter. They are divided among the main circuit board, the display board, the rear panel and the optional prescaler board. See the schematic diagrams in Chapter 9 for complete information.

Most functions are placed on the main board:

– Input amplifiers with trigger level circuits
– Power supply
– Measurement logic
– Microcomputer circuitry
– GPIB interface
– USB interface
– External reference input
– External arming input

The rear panel unit is made of aluminum with a number of mounted connectors, a fan and a power line inlet with filter. Most connectors are soldered directly to the main board.

NOTE: Schematic diagrams in this chapter are simplified. For complete information, see Chapter 9.

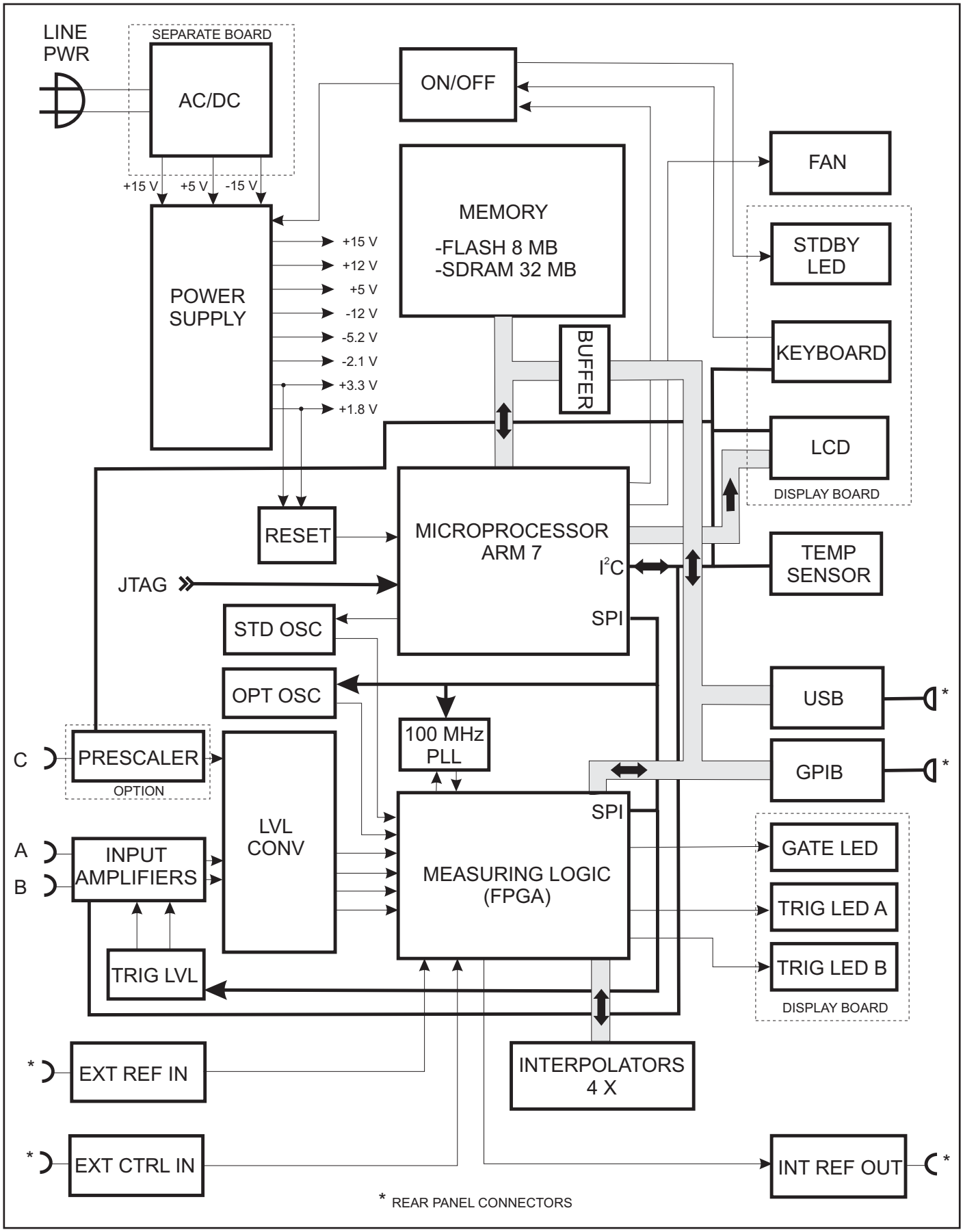

Figure 4-7 *Block diagram of the '90'.*

Hardware Functional Description

Front Unit

The front unit consists of a front piece in molded aluminum, a silicon rubber keypad with conducting contact surfaces, a graphic LCD with LED backlight, and a PCB having etched gold-plated keyboard contacts and a dedicated LCD power supply.

Display

The display is a 320*97 pixels graphical LCD with LED backlight. The LCD controller is part of the processor, and it sends data and control signals to the drivers in the LCD module. Display ON is controlled via the I^2C bus and the keyboard IC. The LCD voltages are generated by a DC/DC converter. Five different voltages are generated. A control signal from the processor switches the converter ON/OFF and also sets the contrast of the display.

The 4 LEDs on the display board are controlled from the measuring logic and the ON/OFF circuit.

Keyboard

The PCB covers the back of the front unit. The keys are laid out as a crosspoint switch matrix consisting of 25 regular push buttons plus a special power button. When one of the buttons is depressed, the dedicated keyboard IC U3 responds by sending an interrupt to the processor. The processor scans the keyboard over the I^2C bus to find out which button calls for attention. The power button differs from the others by having a dual function. In *Standby Mode* it turns on the ON/OFF circuit directly, but when the counter is ON, it is read as any other button. Then the processor turns off the counter. This arrangement is necessary since the processor is inactive in standby mode.

Main Board

Input Amplifiers

Input amplifiers A and B are identical with >300 MHz bandwidth. They are controlled by the processor with relays etc. The analog input signal is transformed to a digital signal. The output signals are LVPECL (+2.4 V and +1.2 V approximately) and fed to the measuring logic.

For a block diagram of the input amplifiers, see Figure 4-8.

■ Impedance Selector

This stage selects 1 MΩ or 50 Ω input impedance with a relay. In 50 Ω mode 11 resistors are used for dissipating the input power, up to a maximum of 2.9 W (12 V_{rms}).

■ Attenuator

This stage has two parts, a fixed preattenuator (approximate attenuation 2.5×) and a cascaded relay-operated 1×/10× step attenuator. The variable capacitors are used for adjusting the frequency response of the attenuators.

■ AC/DC

This stage selects AC or DC coupling with a relay.

■ Limiter

The voltage limiter protects the impedance converter against overvoltage. The ±5 V applied to the input BNC is divided to approximately ±2.1 V by the attenuator. The limiter clamps the voltage to approximately ±2.8 V.

■ Impedance Converter

Split-band technique is used for achieving good frequency response over a wide range. The HF signal is fed via an AC-coupled FET stage. The LF signal (bandwidth DC to approximately 10 kHz) goes via an operational amplifier. The signals are added together at the source of the FET. The output signal from the buffer stage (see below) is fed back to the operational amplifier. A trimmer potentiometer is used for equalizing the gain in the two signal paths (approximately ×0.9).

■ Filter

A lowpass RC filter with an approximate cutoff frequency of 100 kHz can be switched in via a transistor.

■ Buffer

Before the signal is fed to the *Crossover Switch*, it passes a current-amplifying buffer stage that can drive the following low impedance stages.

■ Crossover Switch

This stage uses relays to direct the signal to the two comparators. The following combinations are possible:

- IN A to COMP A and IN B to COMP B
- IN A to both COMP A and COMP B
- IN B to both COMP A and COMP B

■ Comparator

The comparator converts the analog signal to a binary logic signal, with ECL levels (-0.9 V and –1.7 V). The trigger point is set by a voltage from the trigger level circuitry. Temperature-compensated circuitry generates the voltages that control the hysteresis of the comparator. A trimmer potentiometer adjusts the hysteresis window.

■ Trigger Level Generation

Two 12-bit DACs in a single IC generate the two trigger levels for Channel A resp. Channel B. A 2.5 V DC reference IC supplies the reference voltage to the DACs. The DACs are controlled by the processor over the SPI bus. The ±5 V dynamic range at the BNC of the input amplifier is converted to approximately ±2.1 V at the comparator. This range must be covered by the DAC. The voltage step from the DAC is approximately 1.2 mV, corresponding to 2.9 mV per step at the BNC. *Closed Case Calibration* (CCC) is used for adjusting the trigger levels. A known reference level is applied to the BNC and the processor finds out the appropriate setting of the DAC to match the reference level.

■ Logic Level Conversion

The signals from the comparators must be converted from ECL levels to LVPECL levels. There are three converter circuits. One for Channel A , one for Channel B and one for the Set-Reset channel. The two main channels are fed to a Set-Reset flip-flop to make one-channel measurements with variable hysteresis possible. There is also a converter for the signal from an optional prescaler. It has PECL levels (+4.1 V and +3.4 V) that are converted to LVTTL levels (+2.4 V and 0 V).

Oscillator Circuits

The processor has an 11.2896 MHz crystal. An internal PLL in the processor uses the signal to make the internal processor clock, approximately 50.8 MHz. The USB IC has a 6 MHz crystal to make an internal clock and the GPIB IC has a 40 MHz crystal to make an internal clock.

The measurement reference oscillator (timebase) for the timer/counter is a 10 MHz crystal oscillator or an optional oven-controlled crystal oscillator (OCXO). Only one of these is mounted. The user can also select an external reference signal, connected to the *External Reference Input* BNC on the rear panel.

The standard oscillator consists of an inverter and a crystal. The processor controls the frequency of the oscillator with a PWM signal. The PWM signal is filtered to a DC level that controls the capacitance of a capacitance diode. The varying capacitance changes the frequency of the oscillator. The standard oscillator is adjusted with *Closed Case Calibration*. Apply a 10 MHz reference signal to Input A. The processor will find the correct PWM signal to make the internal reference frequency equal to the external reference frequency.

The optional oven-controlled oscillator is a complete oscillator in a small hermetic metal box. An internal accurate DC voltage is available for use as a reference for a 12-bit DAC. The filtered output voltage from the DAC sets the frequency of the oven oscillator. The processor controls the DAC via the SPI bus. The same *Closed Case Calibration* as for the standard oscillator is used. The oven oscillator is kept warm if the line power is connected to the timer/counter, even if it is switched off (in standby mode).

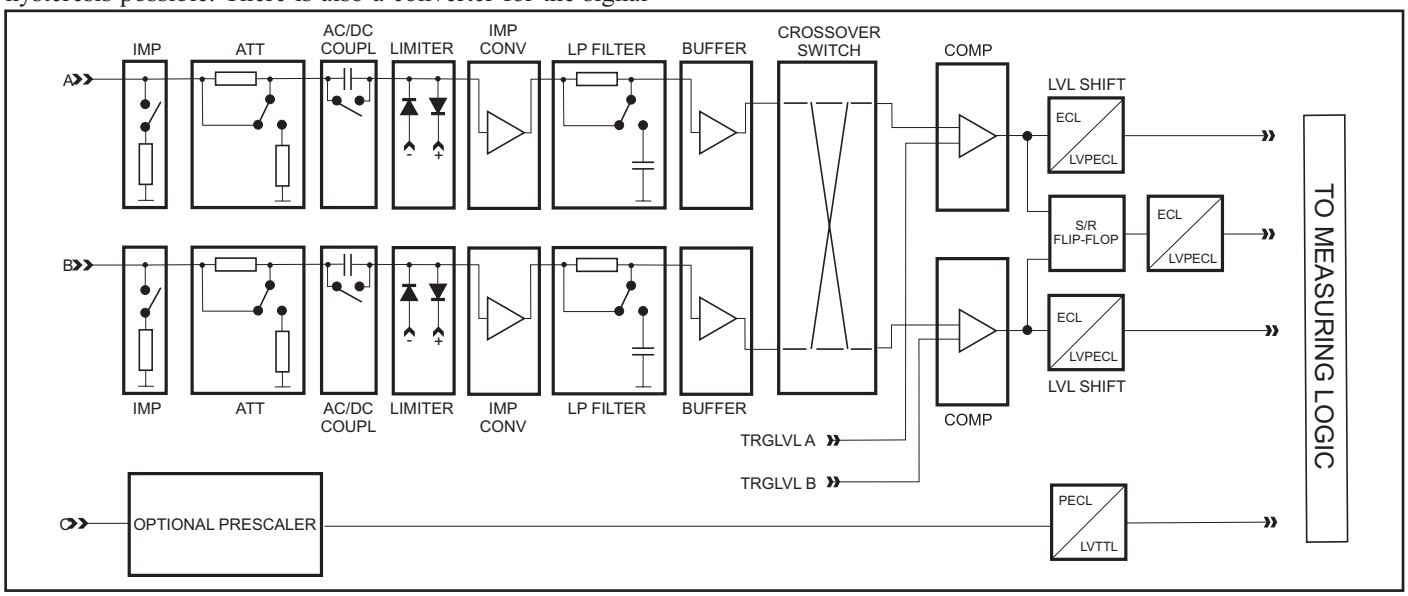

Figure 4-8 *Input amplifier block diagram.*

The 10 MHz reference signal is multiplied in a PLL to 100 MHz. The 100 MHz signal is used in the measuring logic as a reference. The processor controls the PLL IC with the SPI bus. A 100 MHz LC oscillator is used as the controlled element where part of the C is a variable capacitance diode. Its capacitance is controlled with a DC voltage from the PLL IC, thus changing the frequency. The 10 MHz reference signal is applied to the PLL IC as its reference and the 100 MHz output frequency is exactly 10 times the reference frequency.

External Reference Input

A 1, 2, 5 or 10 MHz reference signal can be connected to the rear panel BNC. After amplification in an operational amplifier narrow pulses are made in two D flip-flops, one narrow pulse for each input cycle. These pulses are fed to the 10 MHz crystal filter. After the filter a reconstructed 10 MHz signal is available. A variable capacitor is used for adjusting the filter.

Internal Reference Output

The selected 10 MHz reference signal (standard/oven oscillator or external reference) is available on the rear panel. The 10 MHz reference signal that is used internally by the dedicated counter circuit (FPGA) logic is also sent to an output pin on the FPGA. It is filtered to a sine wave and amplified in an output buffer stage having 50 Ω drive capability.

Measuring Logic

The measuring logic consists of an FPGA, four interpolators and an external control input on the rear panel. The FPGA core uses +1.8 V supply voltage and the I/Os use +3.3 V supply voltage.

The FPGA is controlled by the processor over a 32-bit microprocessor bus. Input signals (A, B, prescaler etc) and reference clock (internal 10 MHz oscillator or external reference) are selected inside the FPGA. The logic for all measuring functions and support functions (trigger indicators, start delay, pacing etc) are inside the FPGA. A 100 MHz reference clock is generated by a PLL circuit giving 10 ns basic measurement resolution. To increase the measurement resolution further, external interpolators are used. The measuring logic also controls three LEDs on the display board; a GATE LED indicating that a measurement is in progress, and two trigger indicators telling that the comparators are triggering on the input signals.

The four external interpolators are identical. Depending on the selected measurement function 0, 2, 3 or 4 interpolators are used. A pulse representing the time from an event on the input to the following rising edge of the 100 MHz reference is fed to the interpolator. During the pulse time a constant current is charging a capacitor. The voltage on the capacitor is measured with a 10-bit ADC. The capacitor is discharged and the interpolator is ready for a new measurement.

An external control input BNC is located on the rear panel. A signal applied to this connector can be used for controlling the start of a measurement, for instance. A comparator converts the analog input signal to a logic signal.

Processor Circuits

The processor is a Sharp LH79524. It contains an ARM7 core and peripherals. It runs on a 50.8 MHz internal clock. The processor that uses 3.3 V supply voltage has an internal circuit that generates 1.8 V for the core. The I/Os use 3.3 V.

The 32-bit microprocessor bus communicates with a 16-bit 8 MByte flash memory and a 32-bit 32 MByte SDRAM. The flash memory contains the program, data for loading the FPGA, and stored data (calibration data etc.). At power-up the code is copied from the flash to the SDRAM for faster execution.

Buffers isolate the memory part of the microprocessor bus from the rest of the bus. Outside the buffers are the FPGA, the GPIB interface and the USB interface.

The processor has a JTAG interface with a connector on the circuit board.

A reset IC monitors the two main logic supply voltages, +3.3 V and + 1.8 V. If a supply voltage fails, the processor will be reset.

Two other buses are also used, an SPI bus and an I^2C bus. The SPI bus is an *output only* bus and the processor controls the 100 MHz PLL, the trigger level DACs, and the DAC for the optional oven oscillator. The I^2C bus is bidirectional and used for communication with the temperature measurement IC, the display board (keyboard + LCD), the prescaler (optional), and the relays and filters in the input amplifier.

The temperature reading over the I^2C bus is used for controlling the fan speed. A PWM output is utilized. The signal is filtered and the resulting DC voltage controls the fan.

Another PWM output is used for controlling the frequency of the standard crystal oscillator.

The LCD controller is a peripheral inside the processor. This controller sends signals and data to the driver circuits in the LCD on the display board.

The processor also controls the OFF switch. Only a signal from the processor can switch off the power. The OFF button on the front panel is read by the processor. ON is handled without the processor, since it cannot respond to external stimulus in standby mode.

Power Supply

This timer/counter has no primary power switch. If connected to line power there are live parts inside the cabinet, and some supply voltages are present on the main circuit board, even if the secondary power switch on the front panel has been turned off (standby mode).

A semi-protected AC/DC module is placed on spacers over the main circuit board. It delivers three regulated DC voltages to the counter, + 15 V, + 5 V and –15 V. When the counter is connected to line power, these voltages are always present. There is a + 5 V trimmer potentiometer on the AC/DC module.

The ON/OFF circuit is active as soon as the counter is connected to line power. The instrument automatically powers up when line power is applied. Only the processor can switch the circuit to OFF state (standby mode). Then only the power button on the front panel can switch the instrument to ON. Once connected to line power and in OFF state (standby mode), supply voltage +12 VU is distributed to the oven oscillator to keep it warm. In standby mode a red LED is lit on the front panel. To keep the AC/DC module stable in this mode, a dummy load is connected to draw a quiescent current of 0.1 A at +5 V.

The three main voltages are +15 V, +5 V and –15 V from the AC/DC module. All other supply voltages are generated from them and are, except for +12 VU to the oven oscillator, switched off in standby mode.

Linear regulators are used for generating stable voltages with low noise and without spikes. Some of them have a resistor net at the input to dissipate part of the heat generated. Thus the regulator itself will run cooler. The following voltages are generated in this way:

+3.3 VA from +5 VU
-5.2 VA from -15 VU
-5.2 VI from -12 VA
-2.1 V from -12 VA
-12 VA from -15 VU
+12 VA from +15 VU

+12 VU from + 15 VU, to oven oscillator, not switched off in standby mode

For digital and general use supply voltages are generated by DC/DC converters:

+3.3 VD from +5 VU
+5 VD from +5 VU via a switch IC
+15 VD from +15 VU via a switch transistor
+1.8 V from +5 VU

Communication Interfaces

Both a GPIB and a USB interface are available for communication with external bus controllers. The connectors are located on the rear panel.

The GPIB consists of an IC. Only 8 bits of the 32-bit microprocessor bus is used. Due to different supply voltages for the processor (+3.3 V) and the GPIB circuit (+5 V), a buffer IC is used for isolating the +5 V GPIB IC from the processor bus. A 40 MHz crystal is used for generating a local clock.

The USB consists of an IC. It communicates with the processor over the 32-bit microprocessor bus, but only 16 bits are used. A 6 MHz crystal is used for generating a local clock.

Rear Panel Unit

The rear panel is made of aluminum. A number of connectors mounted on this unit are accessible to the user, see Figure 4-9.

I/O:

– GPIB communication connector.
– USB communication connector

INPUTS:

– External reference (BNC)
– External arming (BNC)
– Power supply inlet including EMI filter
– Optional main inputs replacing corresponding front panel inputs

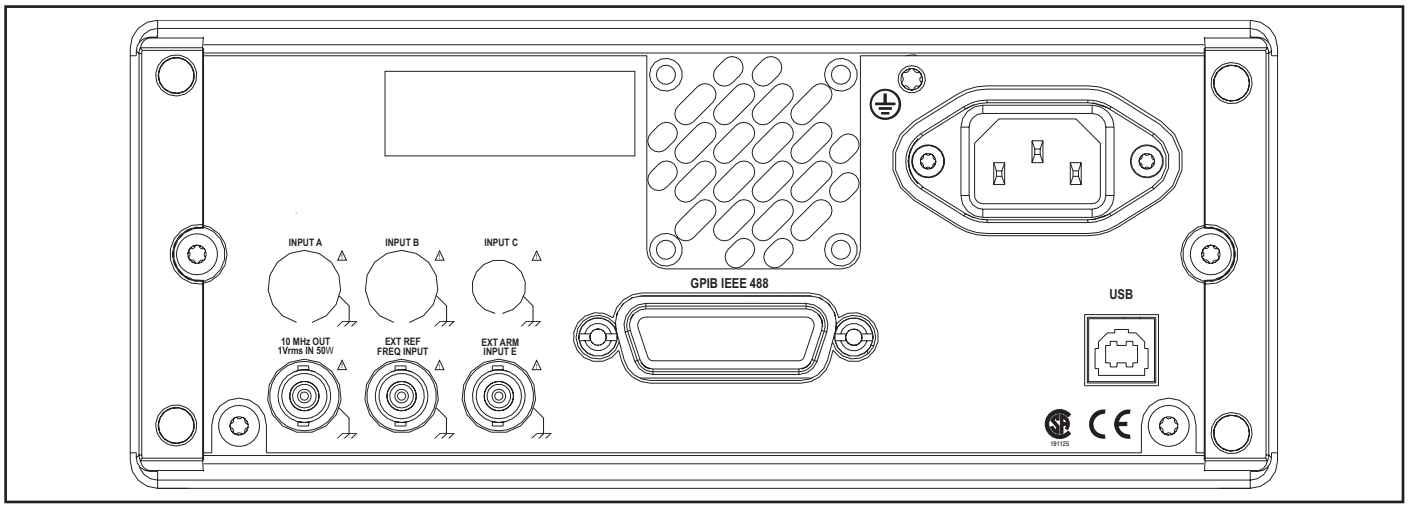

Figure 4-9 *Rear panel, PM6690.*

OUTPUTS:

– Internal reference 10 MHz (BNC)

Prescaler Circuit Board

There are several different optional prescalers available with different frequency ranges. The prescaler is located on a separate circuit board that is connected to the main circuit board with a PCB connector.

A typical prescaler consists of a limiter, an amplifier, a frequency divider, and a detector. The limiter and the amplifier condition the input signal so that the amplitude to the divider is constant. The divider scales the input signal so that it can be handled by the measuring logic on the main circuit board. A detector switches off the output signal from the divider if the input level is too low for the divider to work correctly (dividers often oscillate without input signal).

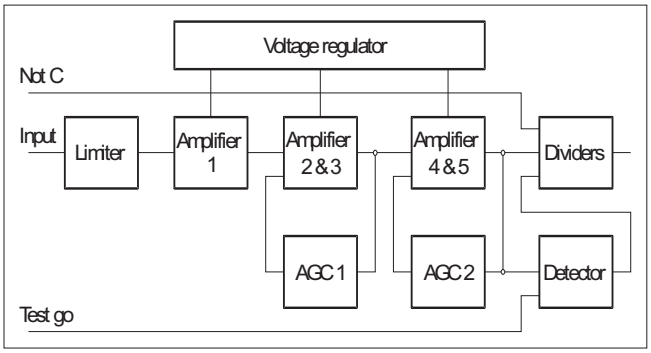

Figure 4-10 *Typical prescaler option, block diagram*

Test Routines

Built-in Test Routines

The test routines are those accessible via the USER OPT key.

– Press USER OPT → Test → Test Mode

– Choose one of the five alternatives:

1. All - Perform the four basic tests below in sequence
2. Memory - Test RAM and ROM
3. Logic - Test measuring logic circuits
4. Display - Test the graphic LCD display
5. Interface - Test the two standard interfaces, GPIB and USB

Power-On Tests

Certain tests are automatically performed at power-up. Errors, if any, are reported on the display.

Chapter 5

Corrective & Preventive Maintenance

Introduction

This chapter contains information about measures to be taken for keeping the instrument in operative condition, or in other words, what you can do to maintain the measurement accuracy, improve certain characteristics and prevent a breakdown.

Traditional troubleshooting is described in Chapter 6 - Repair.

Calibration

The single most important factor for maintaining the high performance of your instrument is calibration on a regular basis. A timer/counter is mainly used for time/frequency-related measurements, so knowing the characteristics of your timebase reference is vital to reliable results.

Scheduled calibration of the built-in timebase reference is highly recommended in applications where external, more accurate, frequency references are not available. Suitable calibration intervals depend on the chosen timebase option and the acceptable inaccuracy, but once a year is often a good starting point.

The '90' has also limited voltage measurement capabilities, and when these features are utilized, the voltage reference should also be calibrated, preferably at the same time as the frequency reference.

Both frequency and voltage calibration can be performed without removing the cover, and the procedures are described in Chapter 7, where you can also find information about calculating calibration intervals for different timebase references.

Instructions for Firmware Upgrade

The firmware is stored in a FLASH PROM, so it is possible to upgrade via one of the standard instrument interfaces (GPIB or USB) without opening the case. USB is standard on most PCs, but GPIB communication requires a special controller board and dedicated SW from NI or CEC. A 'readme.txt' file contains information not covered by these instructions. The relevant files are available through the service organization.

– Make sure the National Instruments NI-VISA 3.2 or later is installed with USB support, even though you are going to use the GPIB interface for the upgrade.
– Establish a communication link between your PC and the instrument over GPIB or USB by using a dedicated application program, for instance NIMax from National Instruments. No other instruments should be connected to the same bus. Firmware upgrade over USB works with firmware version V1.07 or above installed in the instrument.
– Send *IDN? to the instrument and watch the response. If the ID string is OK you can exit the communication program and start the upgrading procedure.
– Download the latest firmware file (example name: CNT_90_109_csl.hex) and the latest loader SW (example name: Loader.exe) to a common directory on your PC.
– Start the Loader.exe program.
– Press "Load" to open the firmware file. Follow the instructions on screen. The update is automatic, and process information can be seen on the PC screen as well as on the instrument display. Do not interrupt the process too early as it may take between a few minutes up to an hour, mostly depending on different possible hardware combinations. A thermometer indicator on the PC monitor gives status reports. The crucial part of the process is when the message "FLASH updating (uninterruptible)" is displayed. Do not under any circumstances interrupt the loader while this message is visible. If the process fails during this part, it may be impossible to control the instrument from the bus as well as from the front panel. Then you have to load new firmware over the JTAG connection to the processor, a method that only the factory can apply.
– After a successful update, the counter is reset (if previous firmware is V1.01 and above). The message "Firmware update complete. Loader is trying to connect to the counter again" is displayed on the PC monitor. Confirm by pressing OK.
– Press OK again when the message "Counter found" is displayed.
– Press EXIT to leave the loader program.
– If the counter is not reset by the Loader program, turn the counter off and on when the update is complete.

NOTE 1: With some firmware revisions and GPIB cards the Loader gives an error message:
"Counter I/O error. Loader shutting down" after the successful update. This is a loader fault and does not harm the upgrade process.

– To remove the SRQ indicator on the front panel, which might be present in such cases, start a GPIB communication tool and send the command "*PSC 1" and run a full power cycle (OFF/ON).

NOTE 2: Some firmware revisions need a full power cycle to resume proper operation. If the instrument does not measure correctly after firmware upgrade, turn the instrument OFF and ON to initialize the hardware properly.

– After the update, enter the calibration menu (password 62951413) and run "Calibrate internals".

Utility Program

Purpose

This service tool is used for configuring the timer/counter, whenever information stored in firmware about serial number and oscillator type etc. has been lost, for example after replacement of the main PCB. It is also used for defining a new factory calibration.

Availability and System Requirements

The utility program can be obtained from the manufacturer or your local service organization free of charge and can be run on any PC with Windows 2K or XP equipped with a GPIB interface from National Instruments. It is distributed as a compressed file called *PM6690.zip* containing all the necessary installation and data files including a *readme.txt* file with additional information.

Installation

– Unpack the *zip* file in an empty directory by using *Winzip*.
– Delete the original *zip* file if you want to save memory space.
– Run the *setup.exe* program and follow the on-screen instructions.

Running the Application

After installation you can start the utility application by running the program *PM6690 Utility.exe* from the chosen directory. Refer to the *readme.txt* file for closer information on topics not covered by the application user interface.

Fan Replacement

This instrument is equipped with a speed-controlled fan as standard to sustain the specified operating temperature range. If your instrument is operating in a 24 h/day system, you should replace the fan every second year to maintain maximum reliability. For part-time applications and where low ambient temperatures prevail, an extended service interval is acceptable.

Follow the instructions on page 3-3 to replace the fan.

Other Important Information

There are no batteries of any kind in this instrument, so in general it is only necessary to remove the cover when the fan is to be replaced, or when a real fault calls for traditional troubleshooting.

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Chapter 6

Repair

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Version A

The descriptions in this section apply to instruments having a Triscend microprocessor.

See General Information on page III for details on relevant serial numbers etc.

Troubleshooting

General

The '90' is a highly integrated Timer/Counter in which a dedicated FPGA counter circuit handles the signal processing, and a microcontroller does the postprocessing and supervising jobs. A number of additional functional units support these basic tasks, for instance power supply, reference oscillator, wideband input amplifiers, comparators, memory (RAM & ROM), digital/analog converters, etc.

The units are treated from a troubleshooting point of view in this chapter, which means that units described earlier should be considered faultless before troubleshooting on units described later.

WARNING: Live parts and accessible terminals which can be dangerous to life are always exposed inside the unit when it is connected to the line power. Use extreme caution when handling, testing or adjusting the counter.

Where to Start

After reading the safety instructions, continue with this chapter for troubleshooting and repair instructions. When you have fixed the instrument, always do the Safety Inspection and Test after Repair, as described later in this Chapter. Then do the checks in Chapter 2, Performance Check. Recalibrate if required by following the adjustment instructions in Chapter 7, Calibration Adjustments.

	Positive ECL	Negative ECL	CMOS	TTL
Supply voltage	+5 V	-5 V	+5 V	+5 V
Signal ground	0 V	0 V	0 V	0 V
Input voltage				
High, VIH	>+3.9 V	>-1.1 V	>+4 V	>+2 V
Low, VIL	<+3.5 V	<-1.5 V	<+1 V	<+0.8 V
Output voltage				
High, VOH	>+4 V	>-1 V	>+4.9 V	>+2.7 V
Low, VOL	<+3.3 V	<-1.7 V	<+0.05 V	<+0.4 V
Bias ref. voltage, VBB	+3.7 V	-1.3 V	-	-

Table 6-1 *Logic levels.*

Logic Levels

The '90' contains logic of different families. The levels of the standard families are listed in Table 6-1. In addition to these families there is also low-level logic requiring lower supply voltages, e.g. +3.3 V, +2.5 V and +1.8 V.

Required Test Equipment

To be able to test the instrument properly using this manual you will need the equipment listed in Table 2-1. The list contains the critical parameter specifications.

Operating Conditions

Power voltage must be between 90 V_{AC} and 260 V_{AC}. The instrument adapts automatically to the applied voltage.

Basic Functional Units

These are the units that are described in this chapter with reference to the page where the section starts:

Power Supply

The DC voltages needed in the instrument are generated from the three main voltages of the AC/DC module.

The instrument has only a secondary power switch, i.e. the AC/DC module is always operating if line power is applied. The three output DC voltages (+5 V, +15 V, -15 V) from the module are present on the main circuit board. When switched off, the instrument is in the standby mode. In this mode only

the ON/OFF circuitry and the optional oven oscillator are powered.

The AC/DC module should not be repaired. Not even the built-in fuse should be replaced. Built-in circuits protect against external overloads, so a blown fuse indicates that a severe internal fault has occurred. Replace the complete module instead.

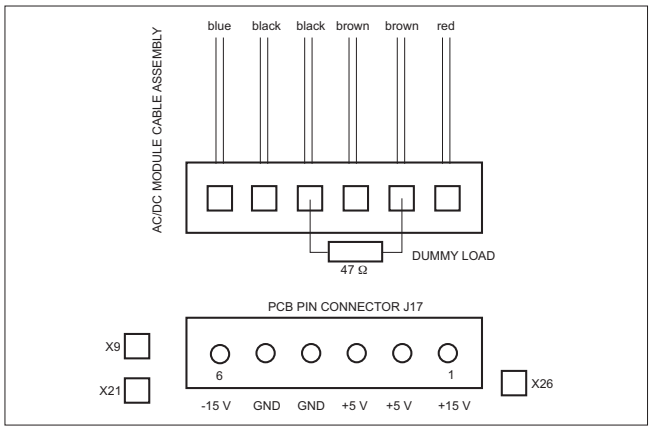

Figure 6-2 *Dummy load connection.*

Test the AC/DC module by measuring the three DC voltages in TP9 (+5.1 ± 0.05 V), TP21 (-15 ± 1 V) and TP26 (+15 ± 1 V) on the main circuit board. See Figure 6-2. Note that there is a +5 V trimmer on the module. If the +5 V is not correct, disconnect the cable to J17 on the main circuit board. Put a 47 Ω 1 W resistor on the connector according to Figure 6-2. Measure on the connector +5.1 ± 0.05 V, +15 ± 1 V and -15 ± 1 V.

It can be difficult to measure the resistance in the supply connector J17 on the main circuit board, because charges are kept by capacitors some time after line power is removed. Remove the cable from the AC/DC module. The resistance between +5 V and ground should be approximately 700 Ω. See Figure 6-2. In a timer/counter with all capacitors uncharged, +15 V and -15 V should be at least MΩ.

Another way to test J17 is to connect 3 DC voltages from a separate bench power supply directly to J17 (suitable connector MOLEX 09-91-0600). See Figure 6-2. The currents drawn from the different supply voltages depend on options installed. Before making this measurement, you should remove any prescaler option.

A timer/counter without options gives the following typical results:

+5 V	0.7 A
+15 V	0.25 A
- 15 V	0.4 A

The oven oscillator increases the + 15 V current between 0.35 A (cold) and 0.1 A (warm).

A block diagram of the secondary power supply is shown in Figure 6-1. All secondary voltages are switched off in standby mode except +12 VU for the optional oven oscillator.

The ON/OFF circuitry controls the ON and OFF of the secondary voltages. Its own supply voltage is always ON, as long as the instrument is connected to line power. See Figure 6-6.

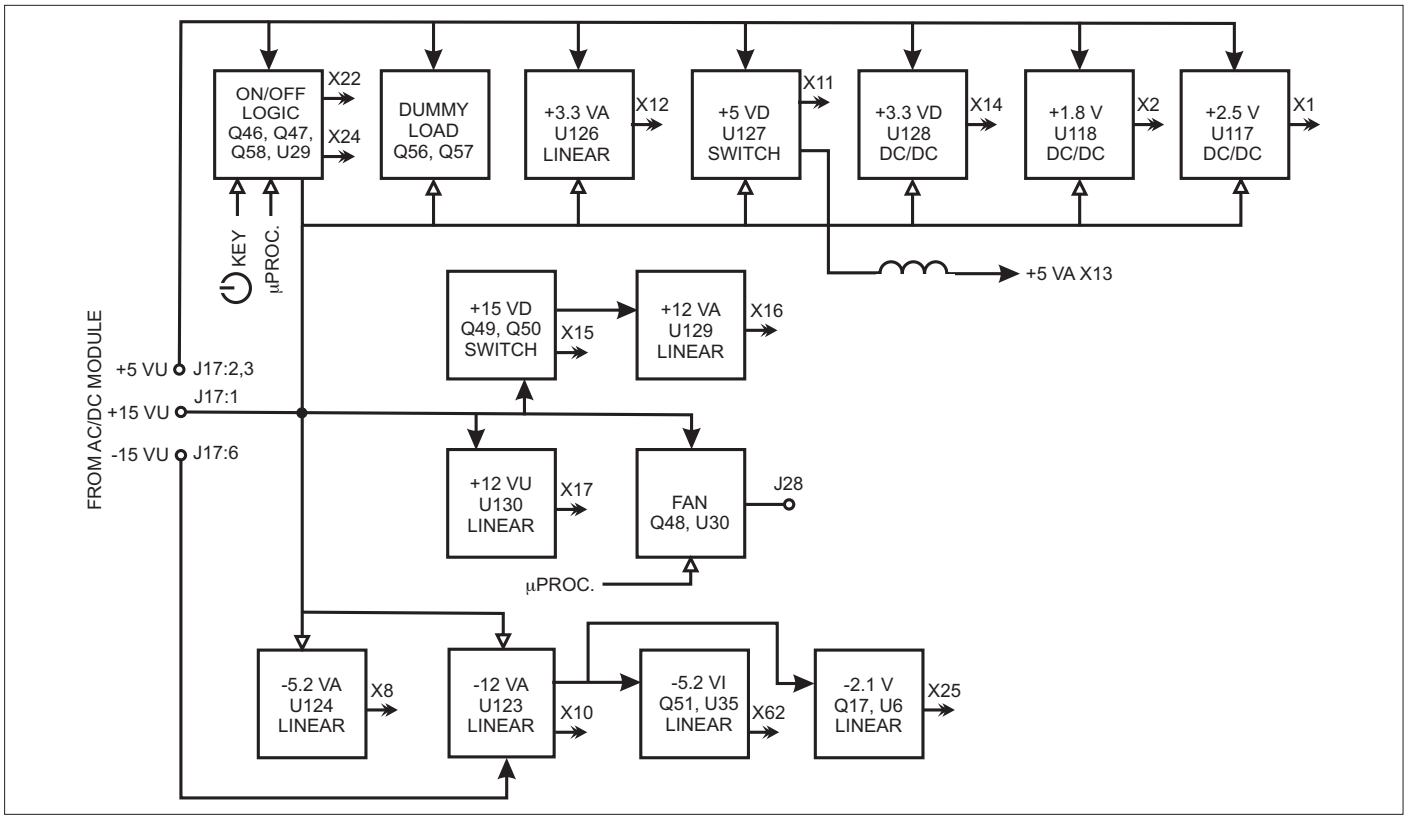

Figure 6-1 *Power distribution*

On connection of line power, R478 and C389 keep the RESETN input of the flip-flop U29 low. This sets the QN output of U29 high. Via Q47 (output signal low) and Q58 (output signal high) the secondary power supply will be set in ON mode. To switch to the standby mode, the processor sets the SETN input of U29 low. This results in the QN output being low and the secondary power supply being set to standby mode via Q47 (output signal high) and Q58 (output signal low). In standby mode a bleeder circuit on +5 VU is connected. It draws approximately 100 mA to stabilize the AC/DC module. The standby LED on the front panel is switched on. To switch to ON mode from standby mode, a negative pulse, generated by pressing the ON/OFF key on the front panel, is connected to the RESETN input of U29.

Linear regulators are used for some voltages to ensure minimum noise. Check the TPs below:

TP12: +3.3 VA (from +5 VU)
TP8: -5.2 VA (from -15 VU)
TP10: -12 VA (from -15 VU)
TP62: -5.2 VI (from -12 VA)
TP25: -2.1 V (from -12 VA)
TP16: +12 VA (from +15 VD)

TP17: +12 VU (from +15 VU) (to oven oscillator, not switched off in standby mode)

For digital and general use some voltages are generated by DC/DC converters. Check the following TPs:

TP14: +3.3 VD (from +5 VU)
TP1: +2.5 V (from +5 VU)
TP2: +1.8 V (from +5 VU)

Some voltages derived directly from the AC/DC module are used as secondary supply voltages without further regulation, and they have semiconductor switches in series to make it possible to shut them off in standby mode. Check the TPs below:

TP15: +15 VD (from +15 VU)
TP11: +5 VD (from +5 VU)
TP13: +5 VA (from +5 VD)

These 13 secondary voltages are used all over the instrument. All secondary supply voltage lines are segmented into branches with ferrite beads. See the schematics. This makes it easier to isolate short circuits by removing ferrite beads temporarily.

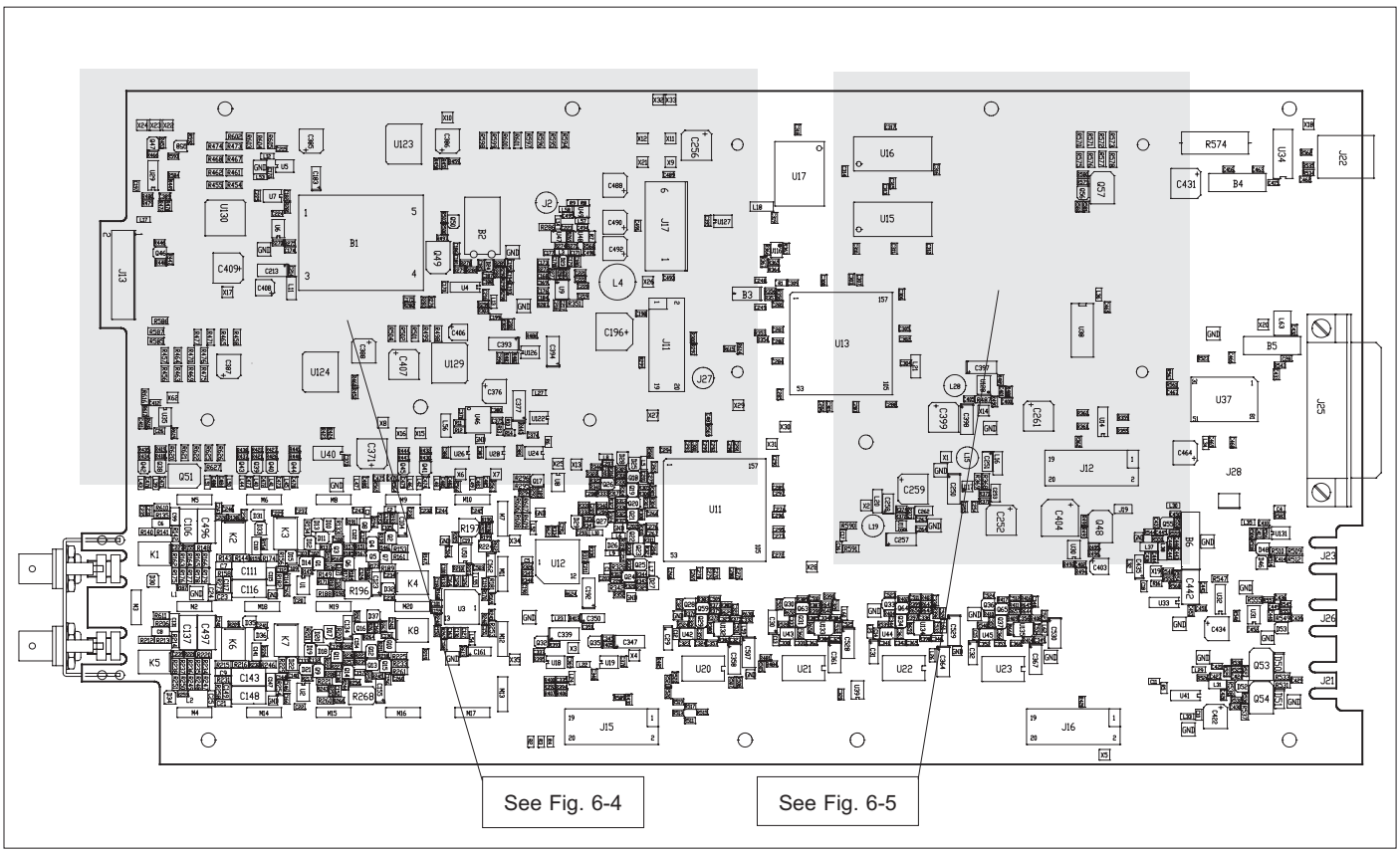

Figure 6-3 *PCB1 survey*

Fan Control

The fan is connected to +15 VU over a speed control circuit. It is only ON if a control signal from the processor is present. The first 8 minutes after power-up the fan will run at a fixed speed, fed with +8.3 V. After that the fan is temperature controlled. The processor reads the temperature from U39 via the I^{2}C bus. Depending on the temperature, the fan is fed with a DC voltage between 8 and 13.5 V. The processor uses a PWM signal that is filtered to control the fan.

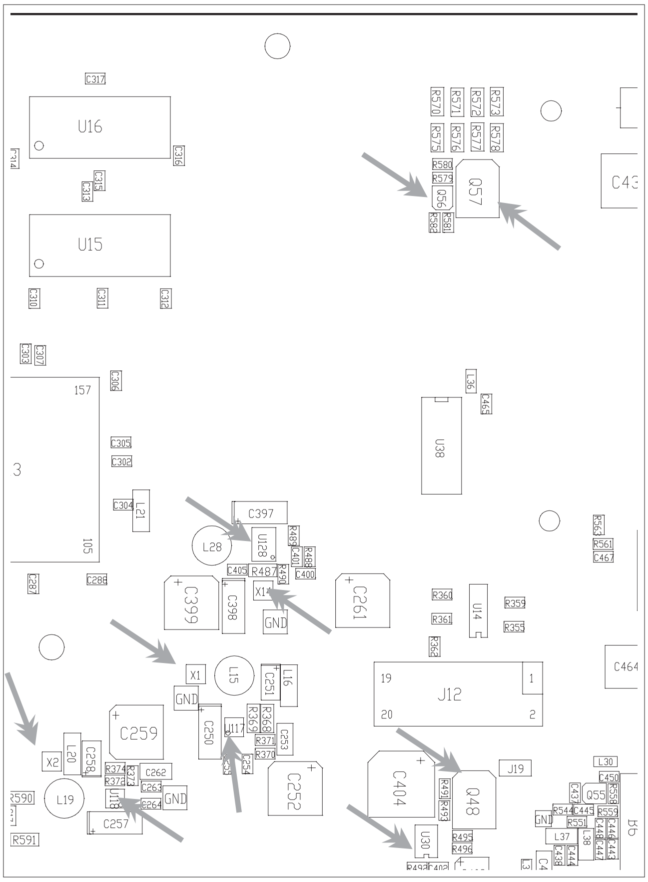

Figure 6-5 *Important power supply locations #2.*

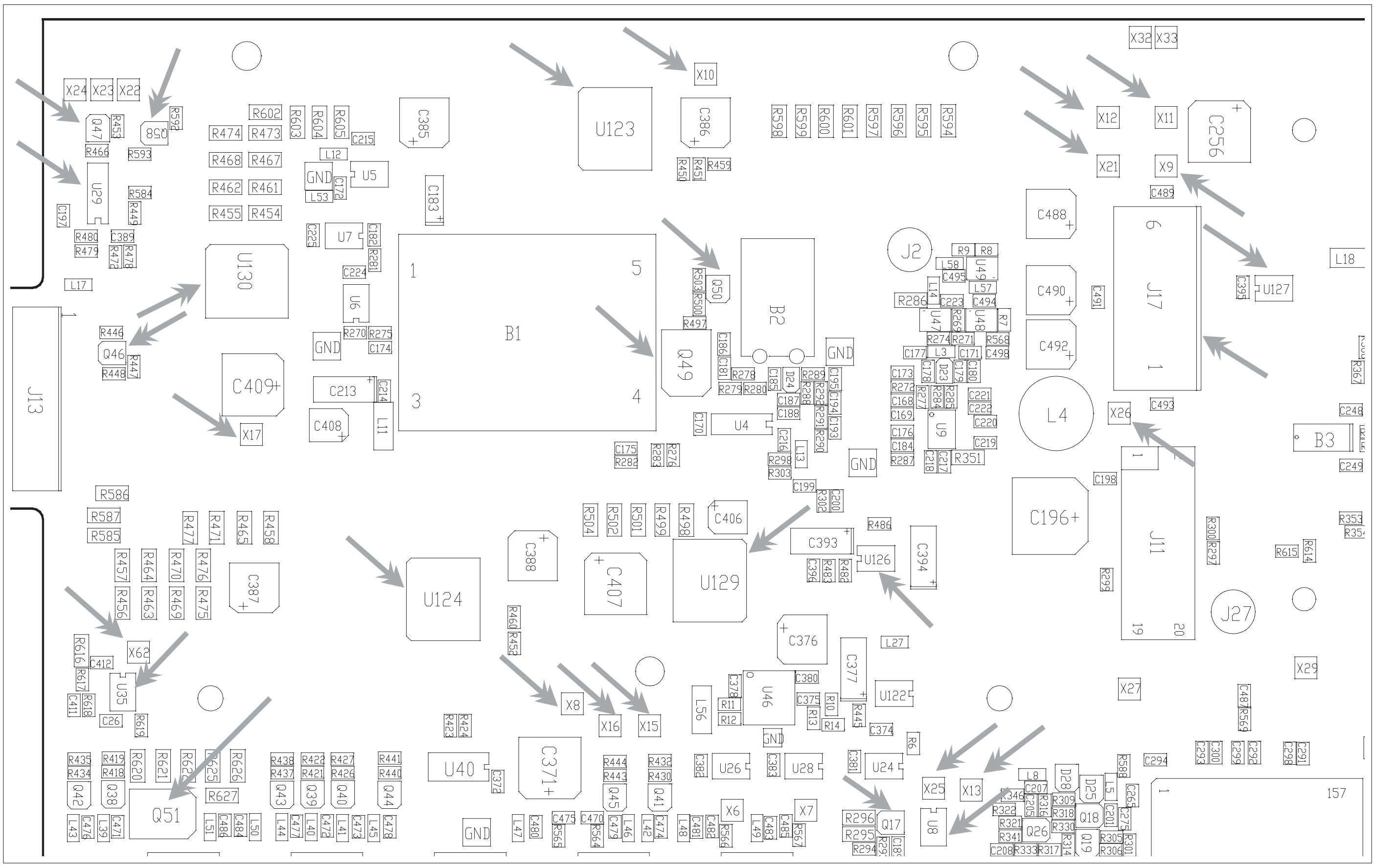

Figure 6-4 *Important power supply locations #1.*

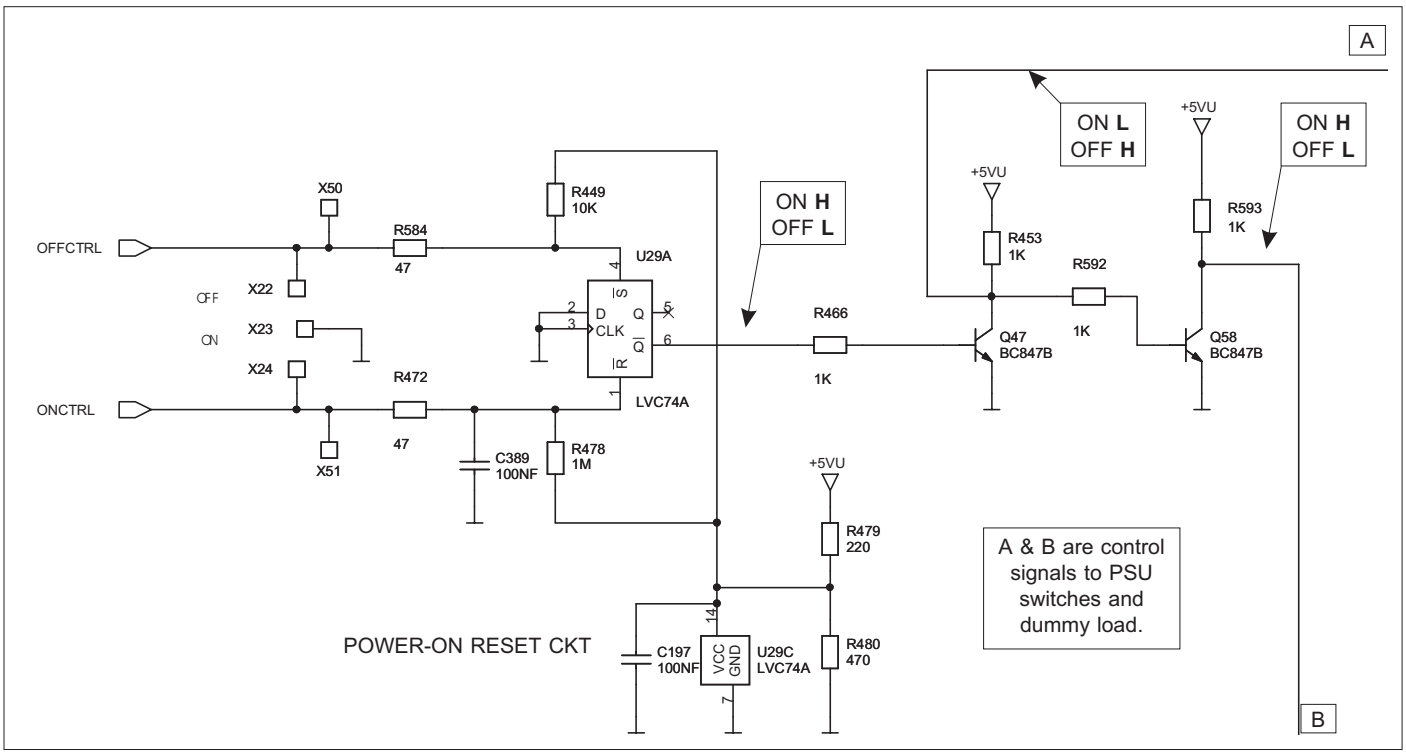

Figure 6-6 *ON/OFF logic*

Input Amplifiers

The input amplifiers for Channel A and Channel B are identical. A trigger level circuit belongs to each amplifier. The trigger level is adjusted to match the hardware during the voltage calibration procedure, see Chapter 7. Note that the input amplifiers must be adjusted according to Chapter 7 (step response, sensitivity etc). The description refers to both channels (Channel B information within parentheses).

Recall the timer/counter default setting. Select the measurement function *Time A-B*. Set both input channels to DC, Man Trig = 0.000 V. No signals connected.

The RF shield must be removed before measuring on the input amplifiers. It is soldered to two of the shield clips. Don't forget to put the shield back afterwards and secure it by resoldering.

First measure some DC values. U3 pin 9 (pin 13) should be near 0.000 V. The same applies to the trigger level, U3 pin 10 (pin 12). The voltage to ground at the point where R171 (R243) and R172 (R244) are connected should be approximately -0.8 V.

Connect a 1 kHz square wave with amplitude 1 V_{pp} in 1 MΩ to Input A (Input B). Measure at the following points (see also figure cc) and use the ground pads that are distributed over the PC board:

Test Points	Approximate Voltage
R140 to R141 (R212 to R213)	1.00 V_{pp}
R156 to C109 (R229 to C140)	0.40 V_{pp}
U1 pin 2 (U2 pin 2)	0.20 V_{pp}
U1 pin 3 (U2 pin 3)	0.20 V_{pp}
U1 pin 6 (U2 pin 6)	-1.00 V_{dc}
R151 to R157 (R223 to R230)	0.40 V_{pp}
U3 pin 9 (U3 pin 13)	0.40 V_{pp}
R309 and R314 (R313 and R315)	ECL levels -1.0 V and -1.7 V
R301 both sides (R304 both sides)	LVPECL levels 1.6 V and 2.6 V

Test the trigger level by manually setting the following trigger levels. Check the voltage at X6 (X7) and U3 pin 10 (pin 12).

Set Level	Approximate Voltage
+1 V	+0.41 V
+4 V	+1.65 V
-4 V	-1.65 V
-1 V	-0.41 V

Set the timer/counter to default. Select the measuring function single period. Connect the 1 kHz square wave to channel A (B). Measure with oscilloscope at X6 (X7). See figure dd for a typical signal.

If any repair work has been done on the input amplifiers, both adjustment and voltage calibration must be performed afterwards. If any repair work has been done on the trigger level circuits, at least voltage calibration must be performed afterwards. See Chapter 7.

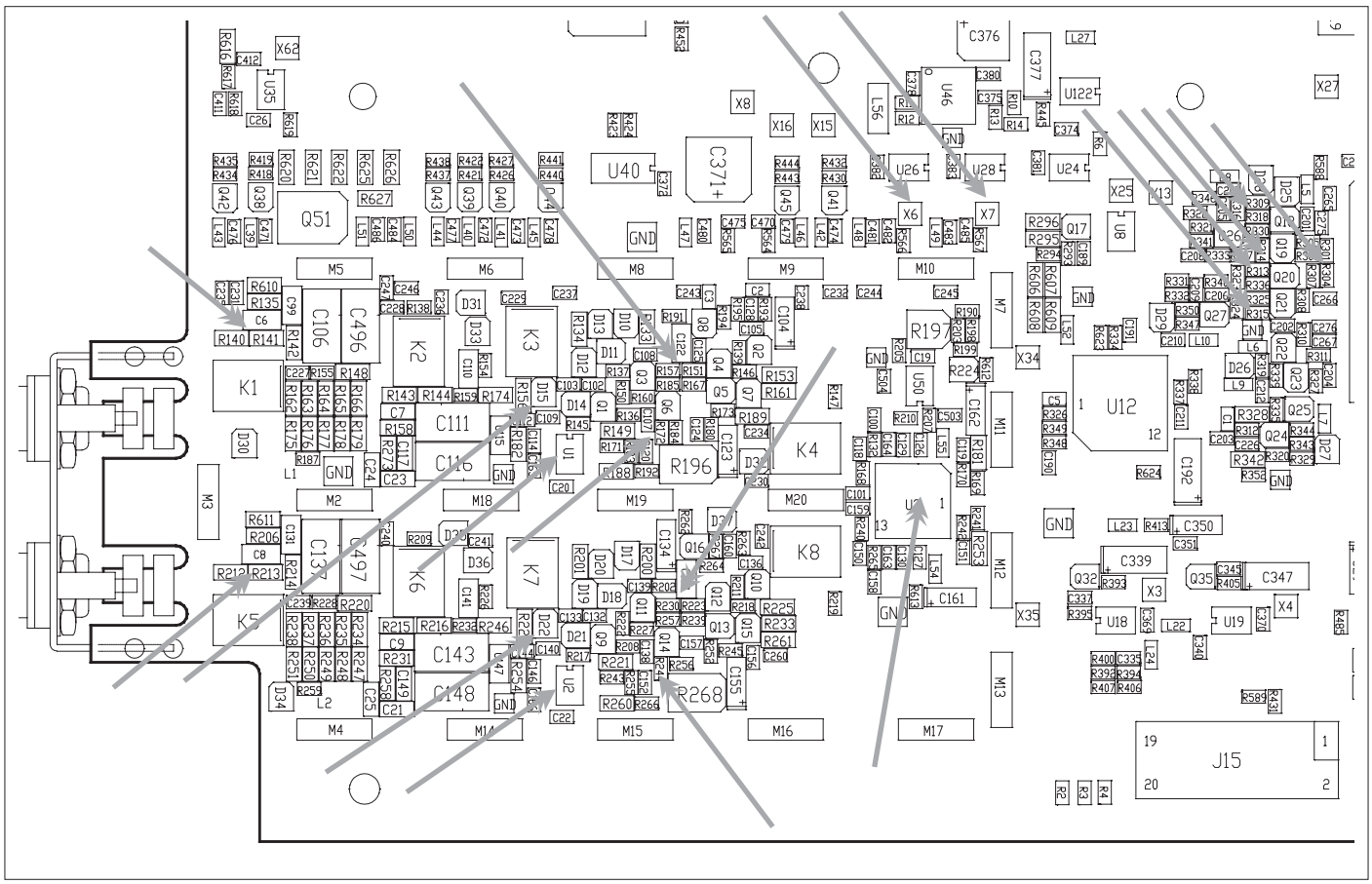

Figure 6-7 *Test points for troubleshooting the input amplifiers.*

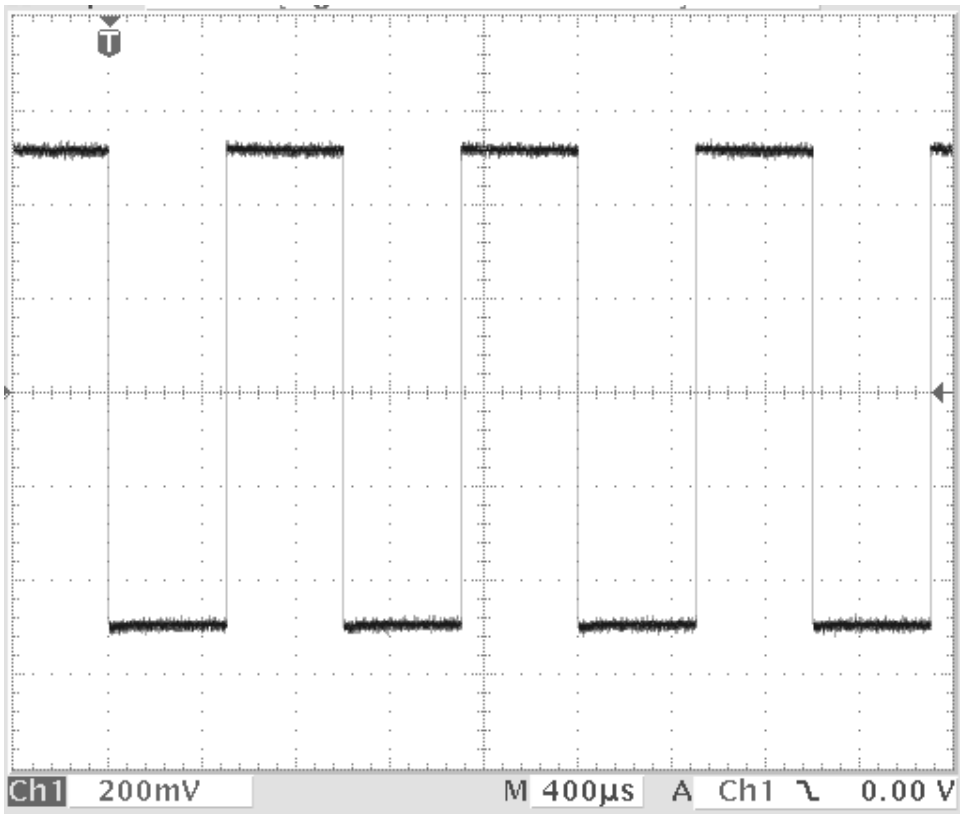

Figure 6-8 *Oscillogram showing the signal at the interconnection of R140 (R212) and R141 (R213).*

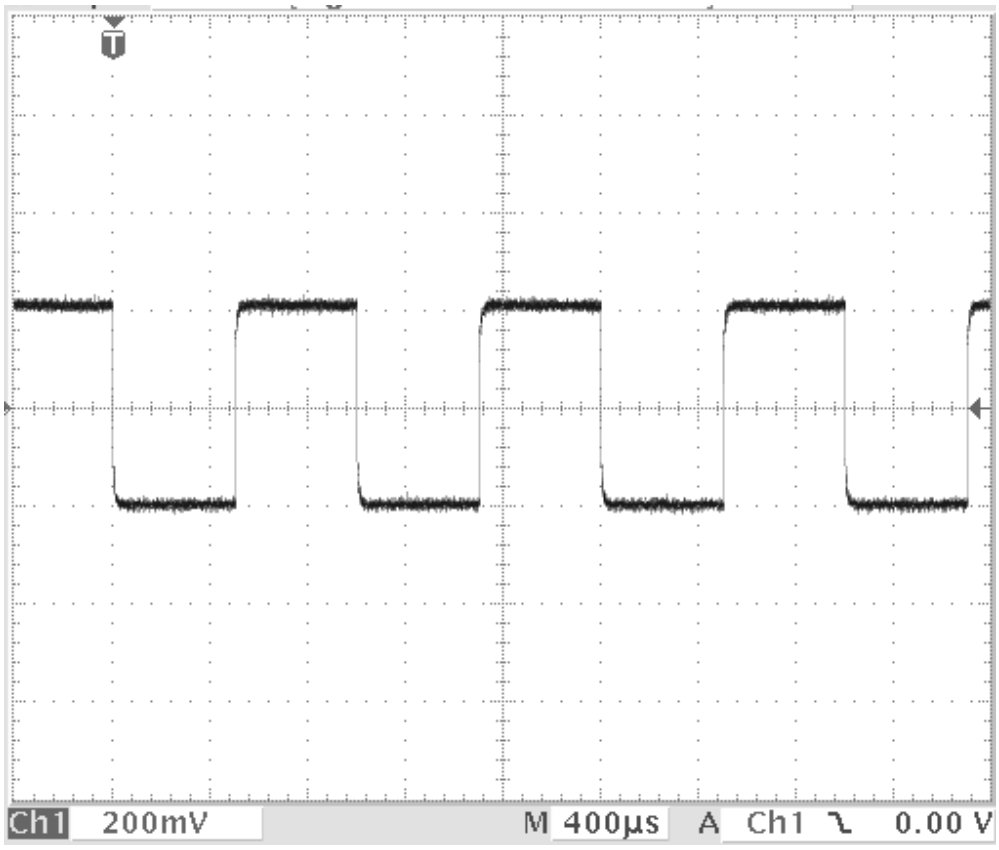

Figure 6-9 *Oscillogram showing the signal at the interconnection of R156 (R229) and C109 (C140).*

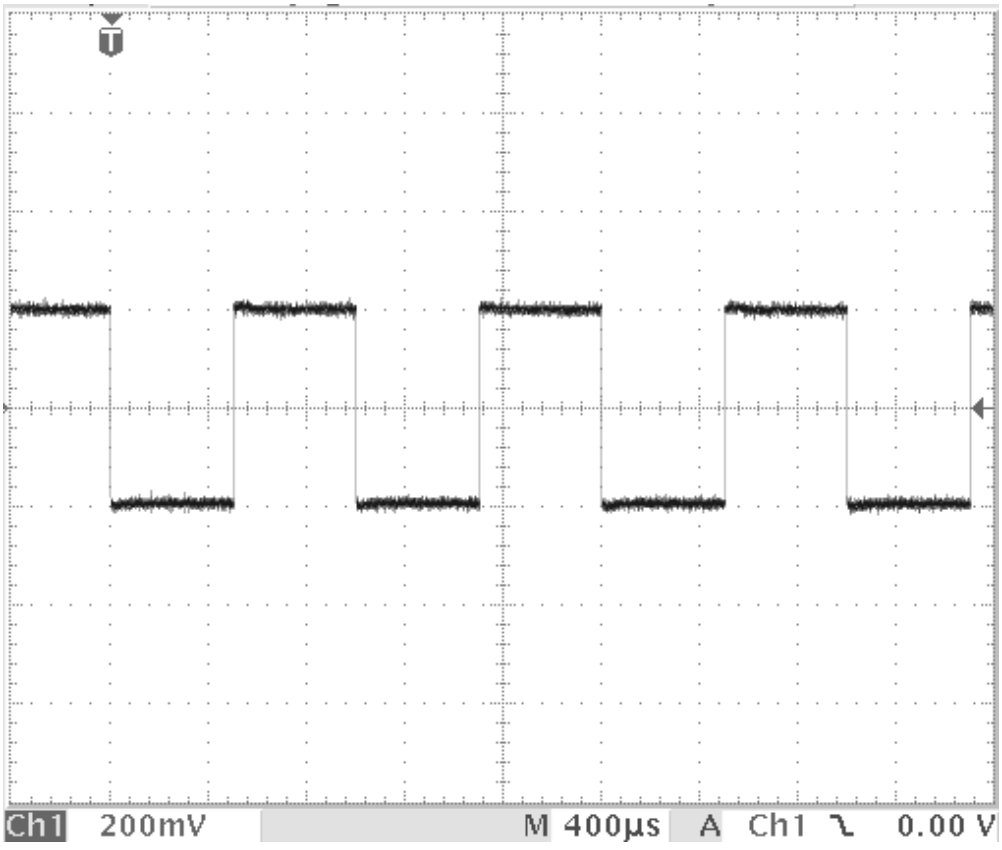

Figure 6-10 *Oscillogram showing the signal at U3:9 (U3:13).*

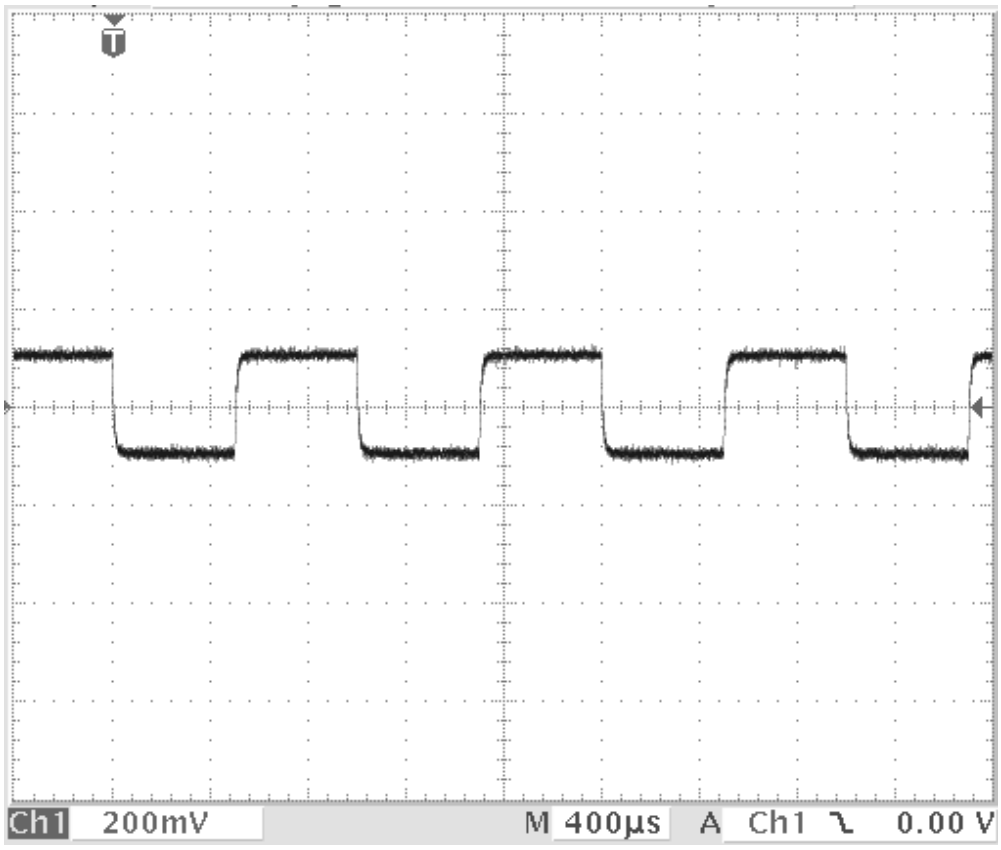

Figure 6-11 *Oscillogram showing the signal at U1:2 (U2:2).*

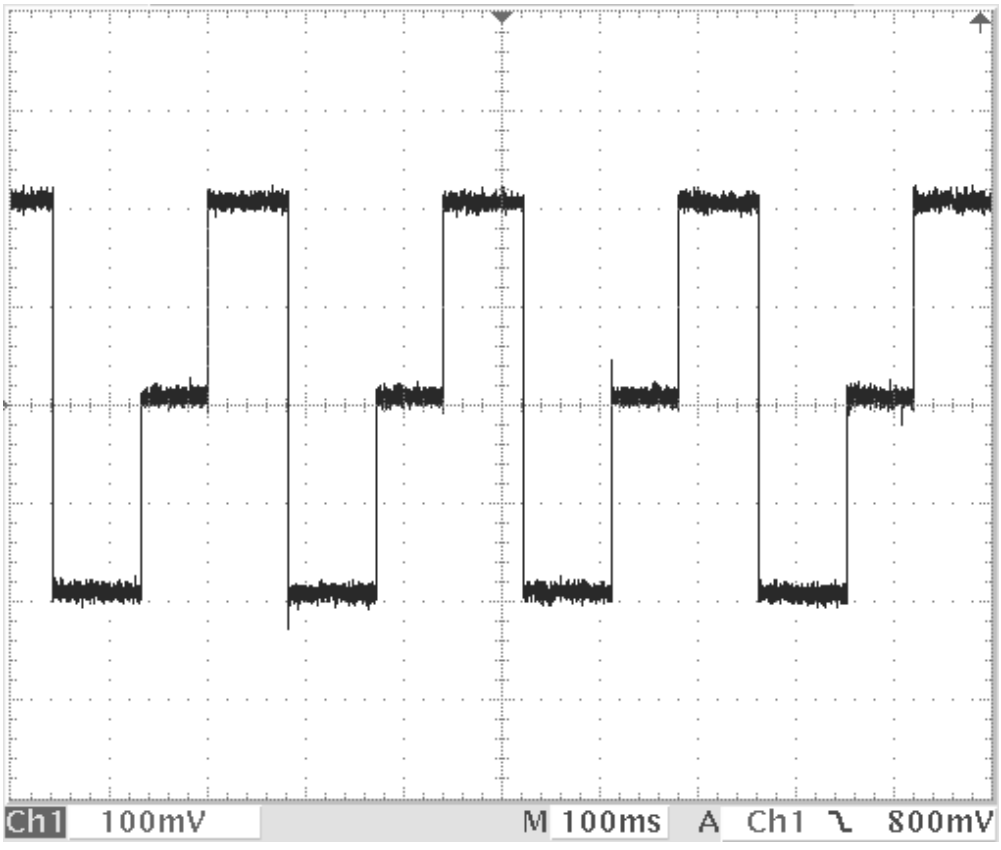

Figure 6-12 *Oscillogram showing the signal at X6, Period Single A.*

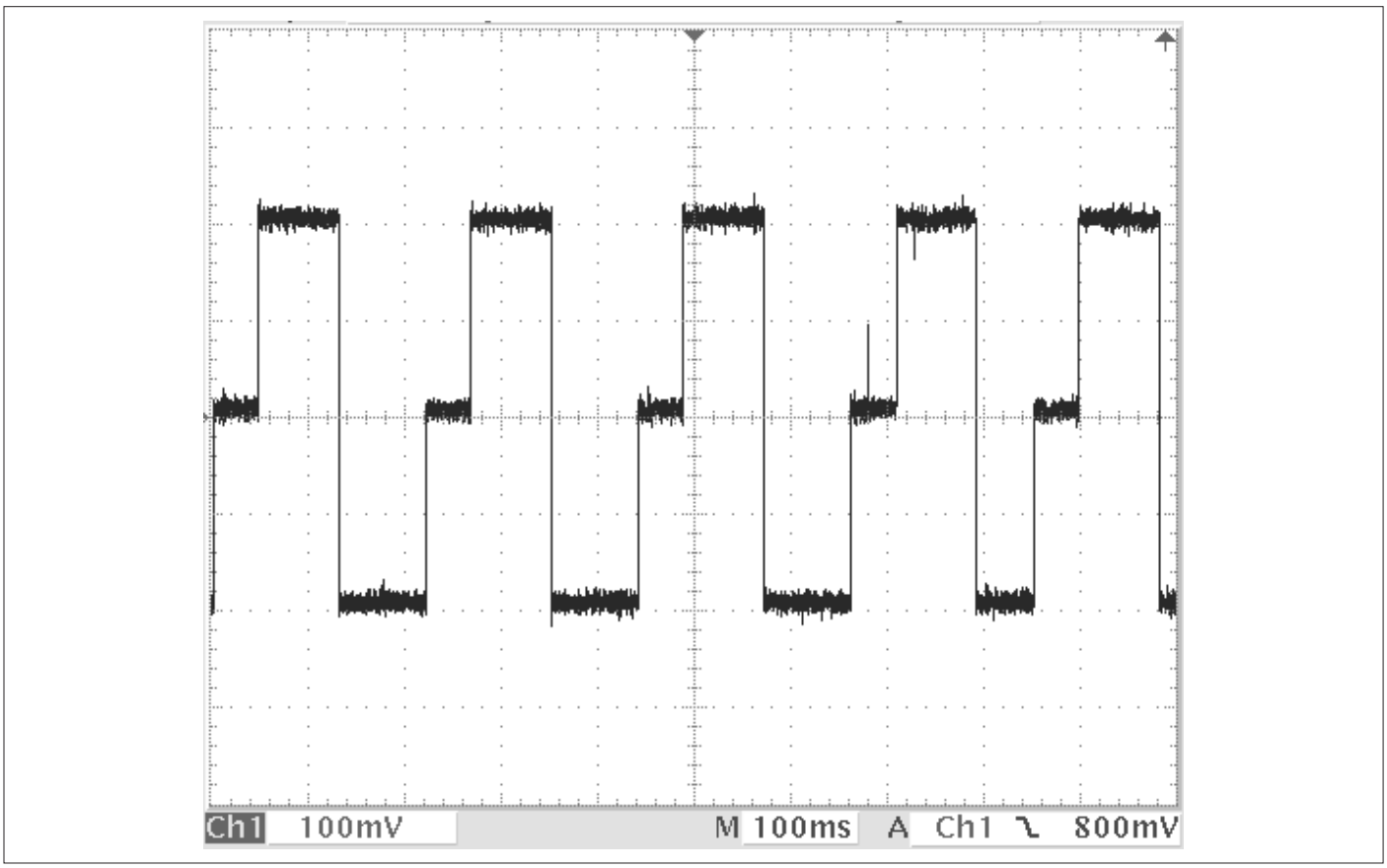

Figure 6-13 *Oscillogram showing the signal at X7, Period Single B.*

Timebase Reference Circuits

The measurement reference is either a 10 MHz signal from an internal oscillator (standard crystal oscillator or optional oven-controlled crystal oscillator) on the main circuit board or a signal from the external reference input that accepts the following frequencies: 1, 5 and 10 MHz. A frequency multiplier transforms the external signal to 10 MHz. The selected 10 MHz reference is always available at the internal reference output. See Figure 6-14.

The main PCB is prepared for both types of internal timebase, but only one of them is mounted. The selection is made at the factory. You have to run the utility program (see page 5-3), if the oscillator is to be changed. *Closed Case Calibration* is used for adjusting the oscillator. On power-up the processor outputs the setting that is stored as the correct one for 10.000000 MHz. It will take some time for the oven oscillator to reach the correct frequency. A calibration must be performed if the adjusting voltage should move during operation, not only on power-up.

The selection between the on board oscillator and the external reference is made in the FPGA. The 10 MHz signal from the other source is switched off.

Connect a 10 MHz signal to the external reference input. Use the **SETTINGS** menu to alternate between internal and external oscillator. Check for correct signals at U4:6 for the standard oscillator, at U4:8 for ther oven oscillator and at U33:3 for the external reference. Check also that the selected timebase reference is present at the internal reference output BNC connector on the rear panel.

Standard Oscillator

See Figure 6-14 and Figure 6-16.

The control signal (U4:1) must be high. The frequency is controlled by a PWM signal from the processor. After filtering the resulting DC voltage changes the capacitance of D24. A DC level between 0 V and +3.3 V at R289 should somewhere within the adjustment range give 10.000000 MHz. Check the output signal and frequency at U4:6.

If the standard oscillator is repaired, a new calibration must be performed. See Chapter 7. A new factory calibration by means of the utility program should also be performed.

Optional Oven Oscillator

See Figure 6-14, Figure 6-15 and Figure 6-16.

The oven oscillator is a self-contained unit, enclosed in a metal box and soldered to the main circuit board. It cannot be repaired and must be replaced with a new oscillator if it is faulty.

Let the oven oscillator warm up 10 minutes before starting measurements. The 12 V supply voltage can be checked at

X17. The oven oscillator should be powered also in standby mode.

The oven oscillator outputs a 10 MHz signal if powered. It should be 1.3 V_{pp} measured at R282. If not selected, a gate (U4) stops the signal, the control signal (U4:9) is then low. The frequency is controlled by a DAC (U5). Its reference voltage is derived from the oscillator, approximately +5 V (C174). The polarity of the reference voltage is reversed in an op amp (U6), and the voltage at U5:1 should be -5 V. The output voltage from the DAC should be between 0 and V_{ref}, measured at R281. The DAC is controlled by the processor via the SPI bus.

The frequency adjustment range should be wide enough to allow for more than 10 years of oscillator aging. The oscillator must be replaced if the normal control voltage range cannot make the oscillator output 10.000000 MHz.

As a last resort to exclude external causes of malfunction, desolder the oven oscillator from the main circuit board. Place it upside down and connect +12 V and ground according to Figure x. A cold oven oscillator draws approximately 0.30 - 0.35 A. During heating the current consumption varies. After 10 minutes it should stabilize on less than 0.1 A. The output V_{ref} should be approximately +5 V and the 10 MHz sinewave output signal should have an amplitude of more than 2.5 V_{pp} measured with a 1 MΩ, 10x probe. The control input has an internal bias to keep the output frequency in the middle of the range. Adjust the control voltage between 0 V and +5 V and check the output frequency range with a frequency counter. The minimum trimming range should be ±5 Hz. 10.000000 MHz must be reached somewhere between 0 V and +5 V.

If the oven oscillator circuitry is repaired, a new calibration must be performed. See Chapter 7. A new factory calibration by means of the utility program should also be performed.

External Reference Input

See Figure 6-14 and Figure 6-17.

The input signal is amplified in U31. The output signal from the amplifier should be a square wave with logic levels, reproducing the timing characteristics of the input signal. Check the signal at U32:11. U32 generates a short pulse (approximately 40 ns) for each input cycle, check at U32:9. These pulses generate a broad spectrum of harmonics, and the following high-Q 10 MHz crystal filter allows only a 10 MHz sinewave to pass. Measure at X19. Note that the trimmer C442 is used for maximizing the amplitude at X19. Check that the amplitude is not less than 1 V_{pp}. If external reference is not selected, the gate U33 stops the 10 MHz signal. The control signal on U33:1 is then low.

100 MHz Multiplier

See Figure 6-14 and Figure 6-16.

100 MHz is used in the measuring logic, mainly as a reference clock, but also for other purposes. A PLL is used for multiplying the 10 MHz reference to 100 MHz. On power-up the processor sets up the PLL IC (U9) via the SPI bus. An output signal, PLL LOCK, tells the processor if the loop is locked (high level). A VCO, consisting of an inverter (U47) and an LC circuit in the feedback loop, is controlled by the PLL IC. The DC voltage from U9:2 is filtered and controls a capacitance diode. The VCO frequency changes with the capacitance. The loop can handle the switching of 10 MHz reference, from internal to external and vice versa. There is no need for a new setup. If external reference is selected and no such signal is connected to the instrument, the PLL will be un-

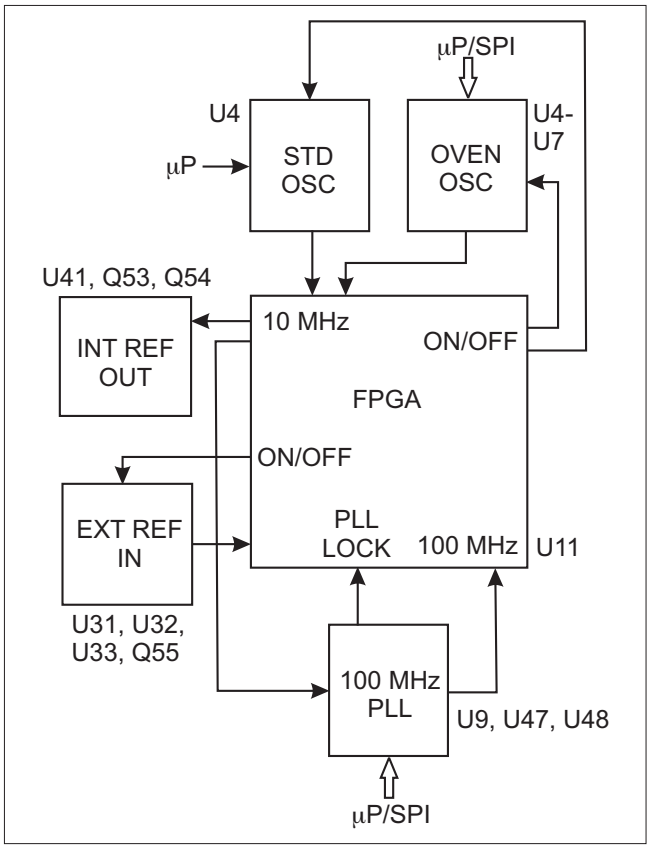

Figure 6-14 *Timebase reference system.*

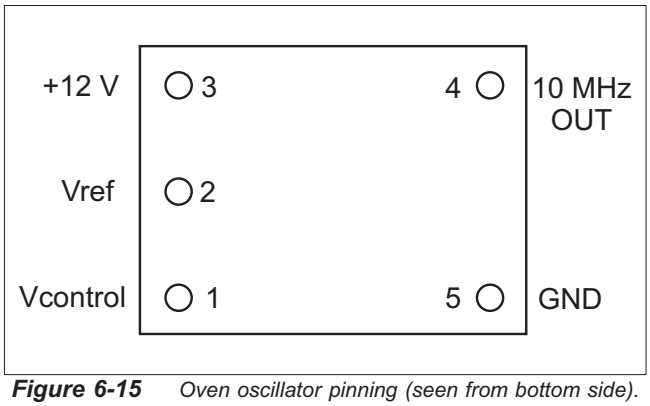

Figure 6-15 *Oven oscillator pinning (seen from bottom side).*

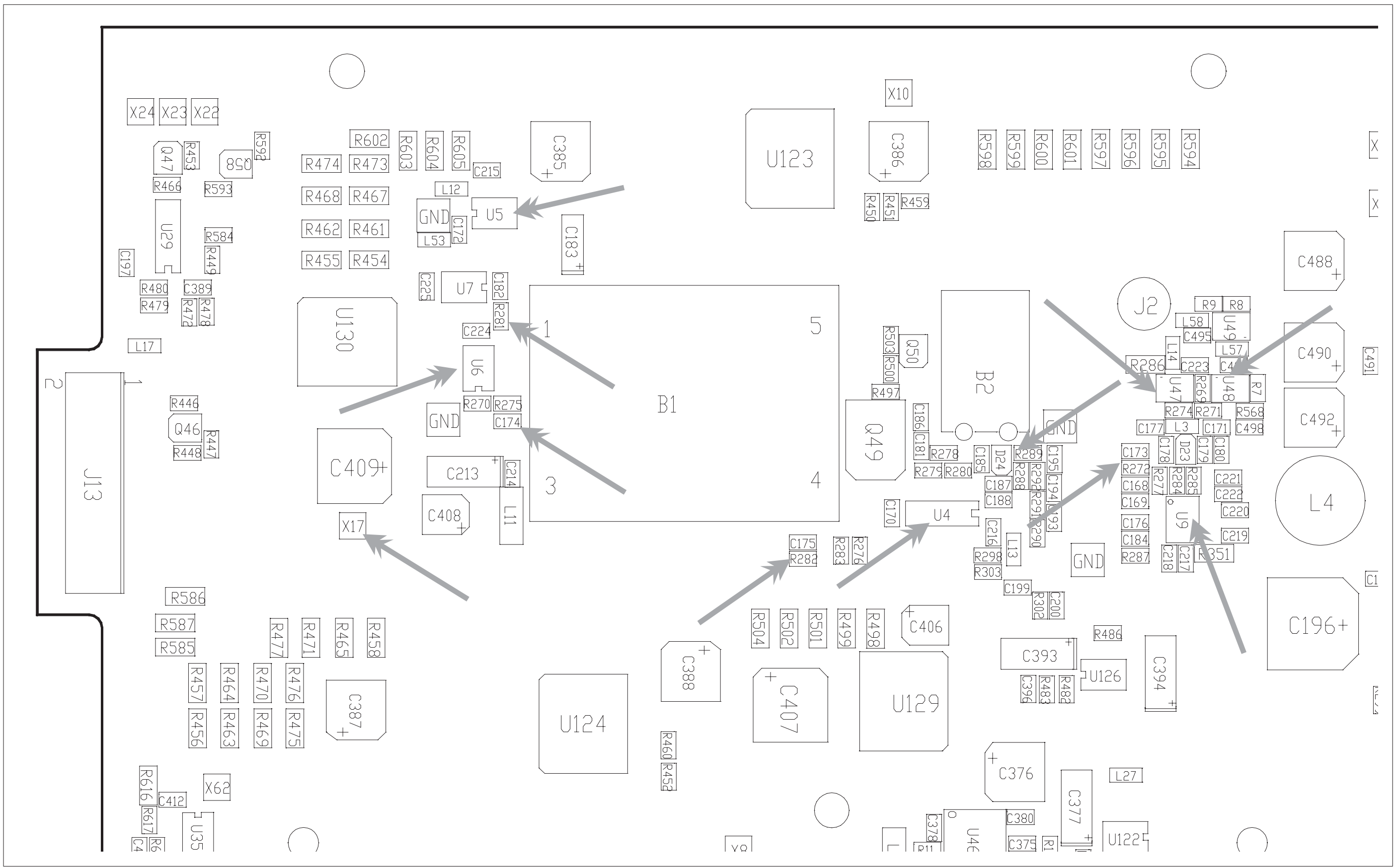

Figure 6-16 *Important locations in the internal timebase reference circuits.*

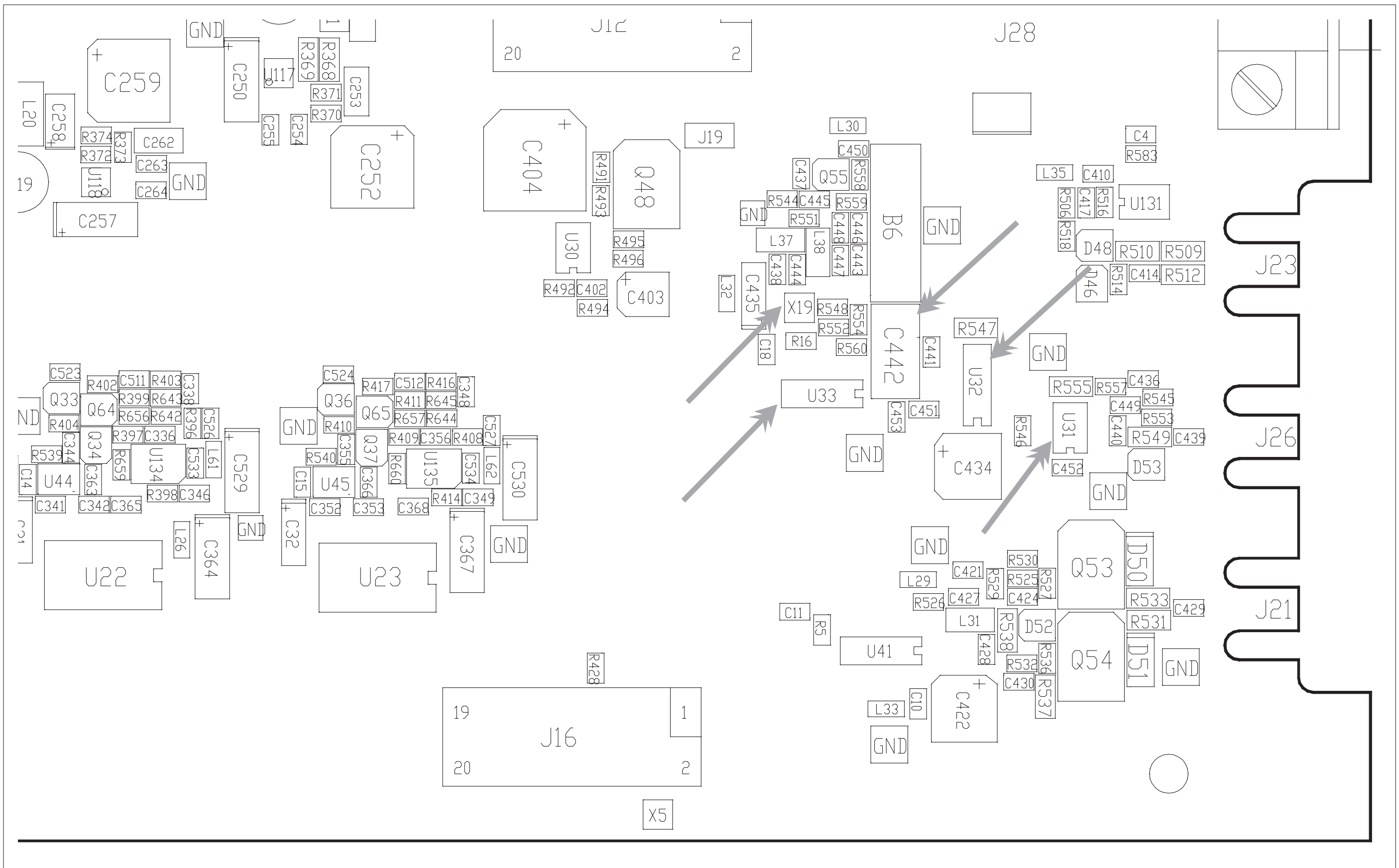

Figure 6-17 *Important locations in the external timebase reference circuits.*

locked, and the VCO will go to one of the extremes. The typical range of the VCO is 95 to 105 MHz, thus giving an error of typically 5 % in the measuring results.

Check the loop voltage (DC) at R272. It should be 1.6 - 2.2 V. Check the 100 MHz signal at U48:4. It should be locked to the incoming 10 MHz at U9:8. Check the lock condition with a 2-channel oscilloscope. Trigger on the 10 MHz channel. Then the signal on the other channel shall be fixed, i.e. not moving along the time axis. Check the PLL LOCK signal at U9:14 (lock is high).

Prescalers

The optional prescalers are not to be repaired. The faulty unit should be sent to the factory, and an exchange unit will be returned.

The best way to isolate the fault is to use another, functioning, timer/counter with the same prescaler. Interchange the prescalers and see if the problem follows the prescaler or the timer/counter.

First measure with Channels A and B and check that the result is OK. Select the function *Frequency C*. Connect a signal according to Table 6-2 to Input C. Check the following pins on the prescaler connector J15 on the main circuit board.

Pin 1 +5 V supply
Pin 5 +12 V supply
Pin 7 ON/OFF, ON is 0 V
Pin 11 test signal, should be 0 V
Pin 12 code 0, see Table 6-2
Pin 14 code 1, see Table 6-2
Pin 16 code 2, see Table 6-2
Pin 4 prescaler output signal, PECL levels (+4.1 V and +3.4 V)

	OPTION		
	3 GHz	8 GHz	14 GHz
Frequency (GHz)	1	1	5
Level (dBm)	0	0	0
Division Factor	16	256	128
Code 0	0	0	1
Code 1	1	0	0
Code 2	0	1	1

Table 6-2 *Prescaler characteristics.*

Measure with oscilloscope and probe at pin 4. The output frequency should be the input frequency divided by the factor in the table. Check with a frequency counter.

Note: The 3 GHz option has a sensitivity trimmer. See page 7-14 for information on how to adjust it.

Microprocessor & Memories

Startup Process

The processor in this instrument is a 32-bit ARM7TDMI. It is housed in an IC (U13) together with peripheral units (SRAM, timers, I^2C bus interface, SPI bus interface, LCD controller etc). The complete IC is a Triscend design and of type A7S20.

A separate memory bus on the processor is connected to one 16-bit Flash PROM (U17) and two 16-bit SDRAMs (U16 and U15). The two SDRAMs are connected to form a 32-bit wide memory.

A Reset IC (U116) monitors +3.3 VD, +2.5 V and +1.8V. The reset signal is active low and kept low for approximately 160 to 180 ms after the voltages are OK. Measure at X33. The ramp-up time for +3.3 VD is approximately 2 ms, for 2.5 V approximately 4 ms and for 1.8 V approximately 3 ms.

The rising edge of the reset signal marks the start of the boot sequence. All I/Os on the processor are set high with a weak (high-ohmic) pull-up. The fan will run at full speed (R492). The memory controller in the processor is set up. The processor reads in the Flash PROM for the initialization data at certain addresses. Check CE0 at U13 pin 16. When the data is found, the processor loads it inside the processor IC. The I/Os will be set up. The fan will stop running because the pin is set low. The 32 kHz oscillator will start running (check at R357) and an internal PLL will generate 30 MHz internal and external clock, check X29.

After the initialization the processor starts executing code from address 0 in the Flash PROM. The program copies the code from the Flash PROM to the SDRAM. When done it starts executing from the SDRAM. Check SDCE0 at U13:26. The Flash is not used for executing code after this, only occasionally for storing data that should be non-volatile.

See Figure 6-21 to Figure 6-23 for a survey of a typical instrument startup.

The LCD is switched on. The LCD controller in the processor generates the control signals for the LCD. See Figure 6-24 to Figure 6-29. Note the different timing for the signals. The I^2C bus is used for switching the LCD on. The ON signal can be checked at R34 on the display board. It should be high. The LCD voltages must also be switched on. It is done by a control signal from the processor. Check the signal at R33 on the display board. It should be high. Negative pulses on this signal are used for adjusting the contrast of the LCD, i.e. the LCD voltages. The range is 14.9 V to 17.5 V measured at X1 on the display board. Set the contrast so X1 is 16.2 V. Check the LCD voltages at X2 (14.7 V), X3 (13.3 V), X4 (2.9 V) and X5 (1.5 V). See Figure 6-19.

The FPGA (U11) has to be programmed. The I^2C bus is used for controlling the loading of the FPGA, the pins PROGN (U40:9) INITN (U40:7) and DONE (U40:8) are used. The clock (U11:155) and data (U11:153) are controlled by the

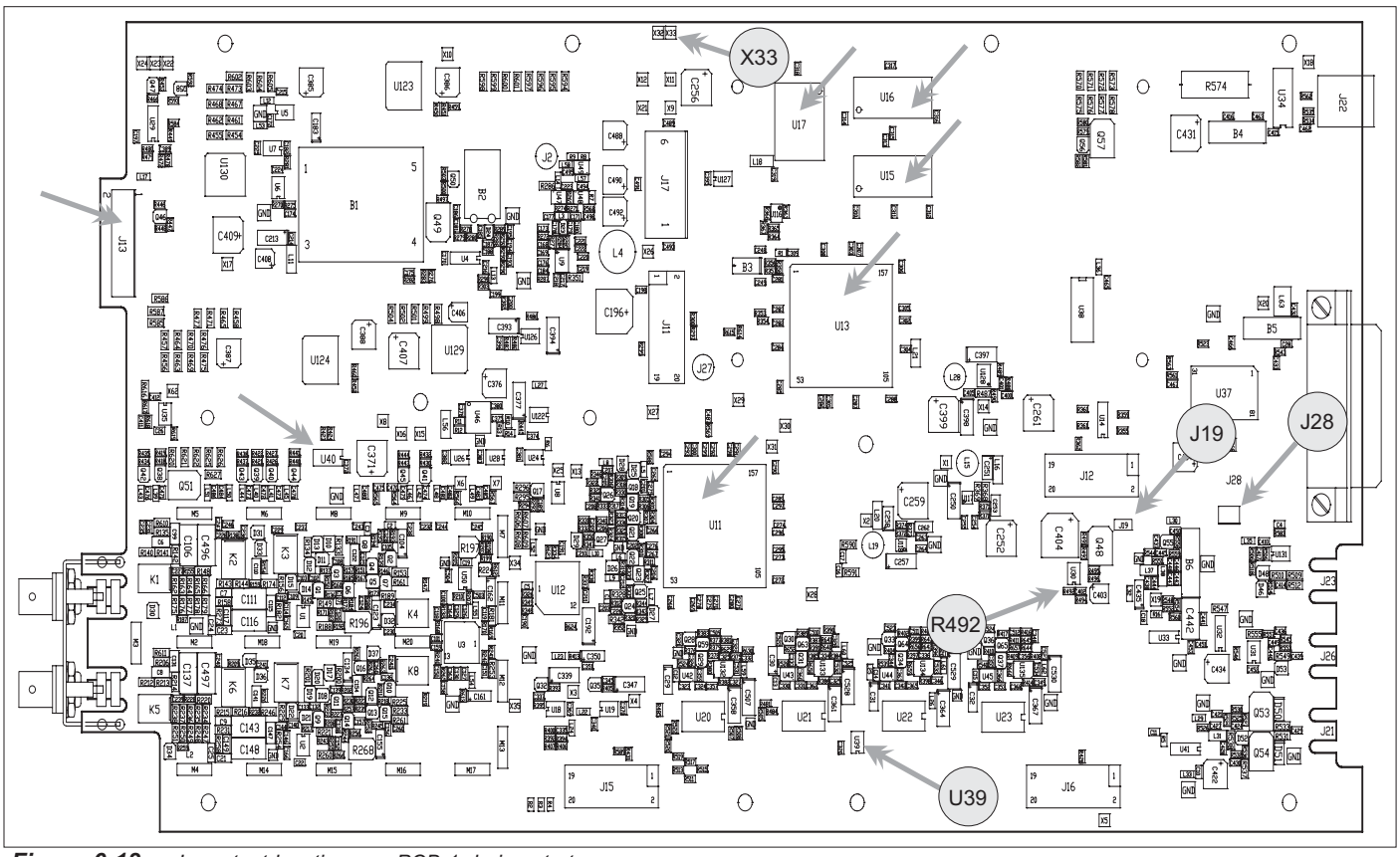

Figure 6-18 *Important locations on PCB 1 during startup.*

processor. See Figure 6-22. The loading starts when PROGN is set low. The FPGA responds with a negative pulse on INITN and setting DONE low. After loading 1442016 bits, which takes approximately 2.2 s, the FPGA sets DONE high if the loading was successful. If an error is detected, INITN is set low. One clock pulse after DONE is set high all I/Os on the FPGA are defined. If the loading of the FPGA is not successful, the program just goes on with the rest of the startup procedure.

The fan is set to 8.4 V. See Figure 6-23. Measure on J19 or J28. The input amplifiers are initialized and a "click" from the relays is heard. The I^2C bus is used for controlling the relays.

Note: The I^2C bus is of the utmost importance for the start of the instrument. The FPGA, the LCD and the relays in the input amplifiers all need a faultless I^2C bus to work properly.

Note: If the Flash PROM is exchanged, it must be replaced by a preprogrammed Flash PROM. Voltage and timebase calibration must be performed anew. The utility program must be used for transferring the calibration results to new factory calibrations. The serial number and the oscillator option must also be programmed by the utility program.

The fan is kept at +8.4 V for the first 8.3 minutes. After that the fan is temperature controlled. The processor reads the temperature via the I^2C bus every 10th second. IC U39 measures the temperature.

The keys on the display board are read over the I^2C bus. If a key is pressed, the I^2C bus circuit U3 notices that and sends an interrupt to the processor. Check at J13:9; low is interrupt. The processor then scans the keys via the I^2C bus to find the depressed key. See Figure 6-30. During the scanning there may appear some extra interrupts. This is not an error condition.

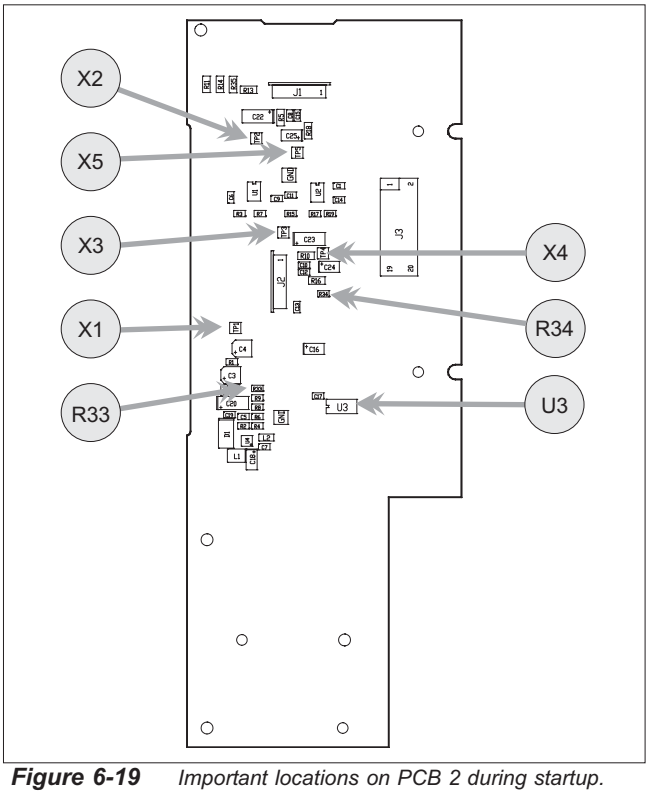

Figure 6-19 *Important locations on PCB 2 during startup.*

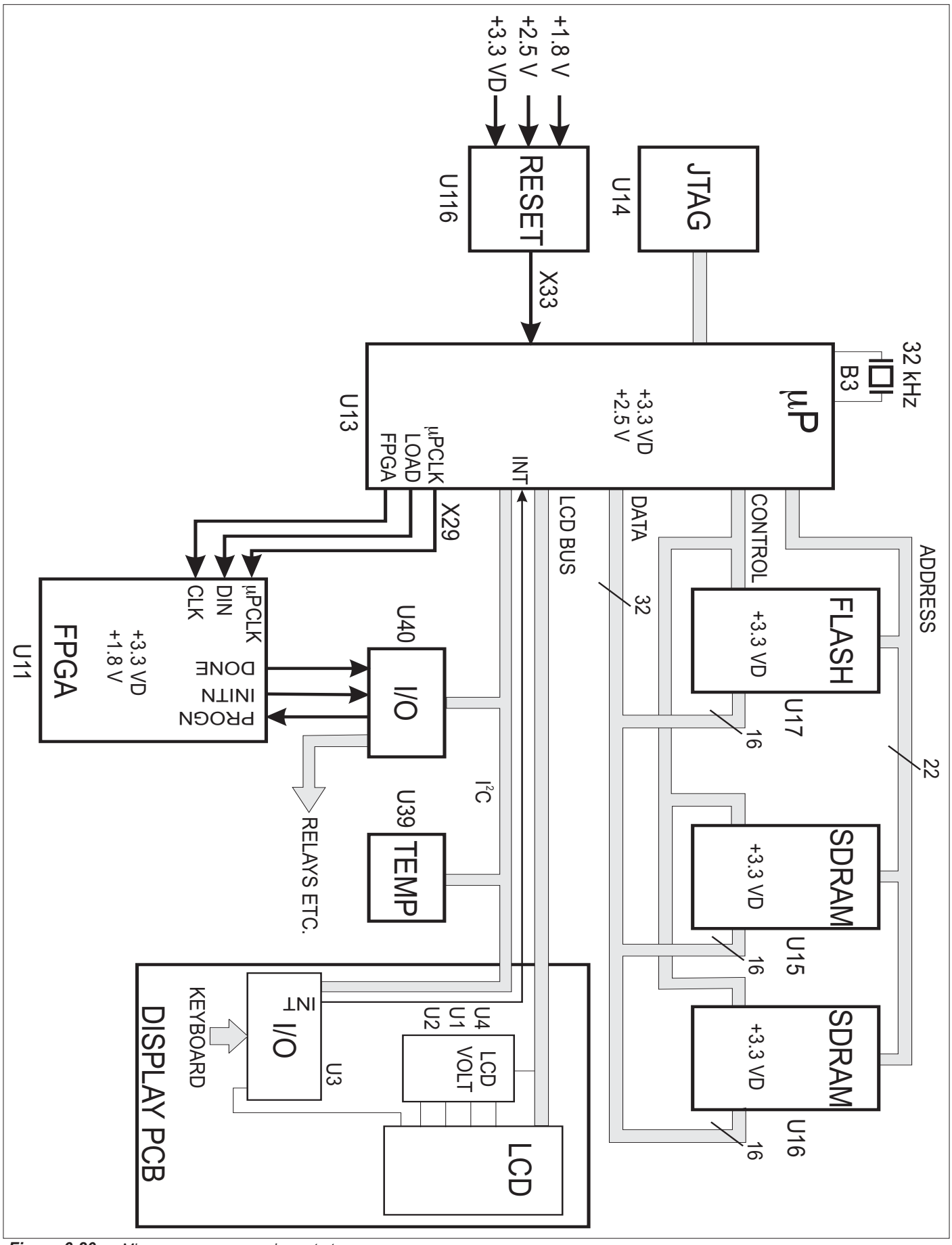

Figure 6-20 *Microprocessor, memories - startup.*

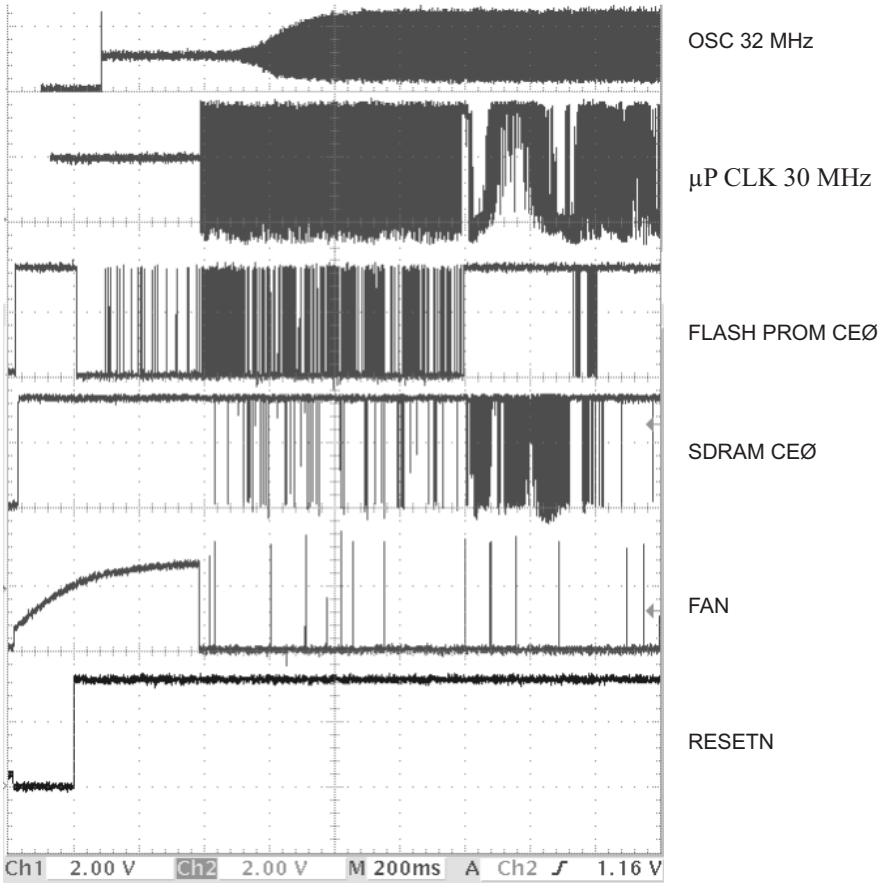

Figure 6-21 *Startup timing - processor, memories, fan.*

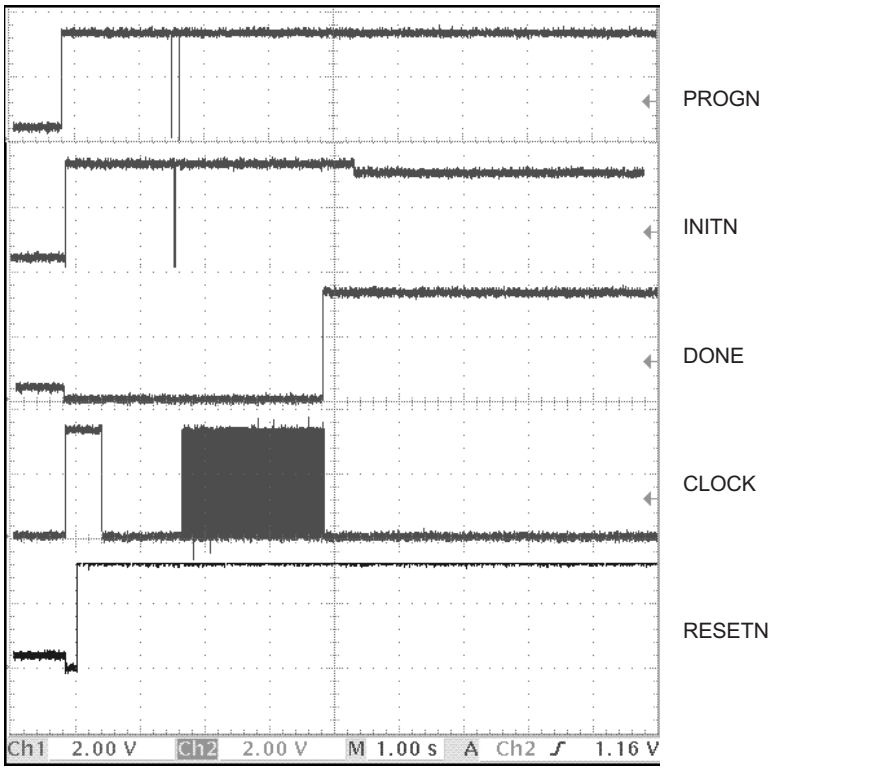

Figure 6-22 *FPGA loading.*

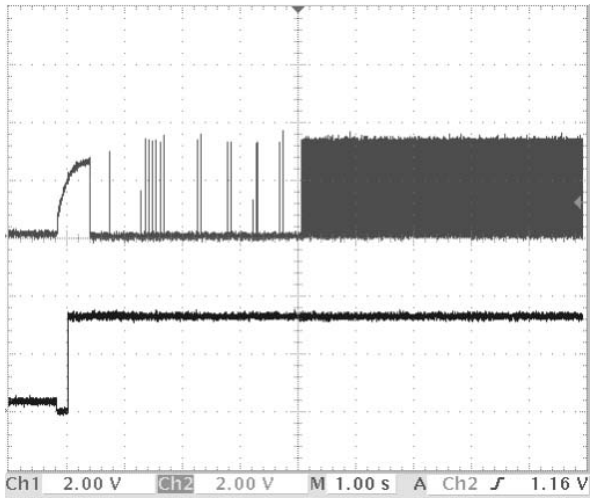

Figure 6-23 *Fan startup - extended timescale.*

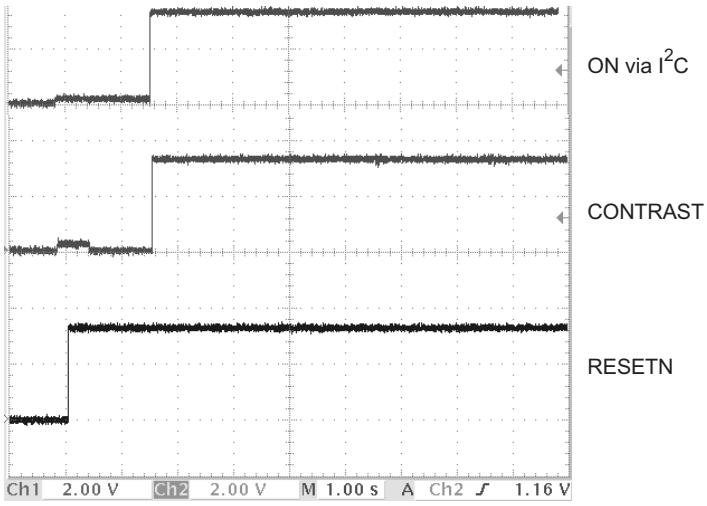

Figure 6-24 *LCD control signals, ocillogram #1.*

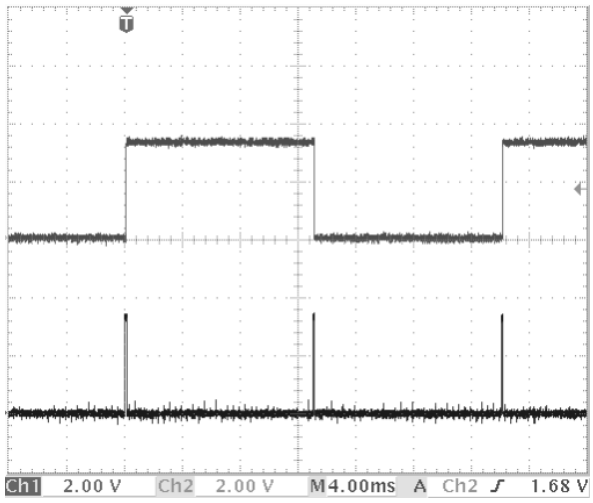

Figure 6-25 *LCD control signals, oscillogram #2.*

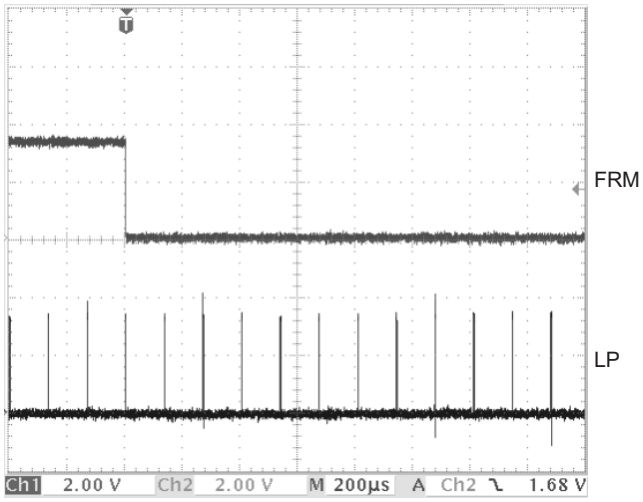

Figure 6-26 *LCD control signals, oscillogram #3.*

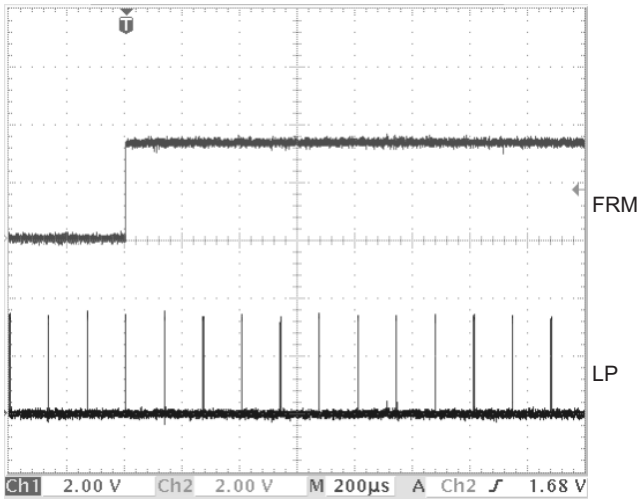

Figure 6-27 *LCD control signals, oscillogram #4.*

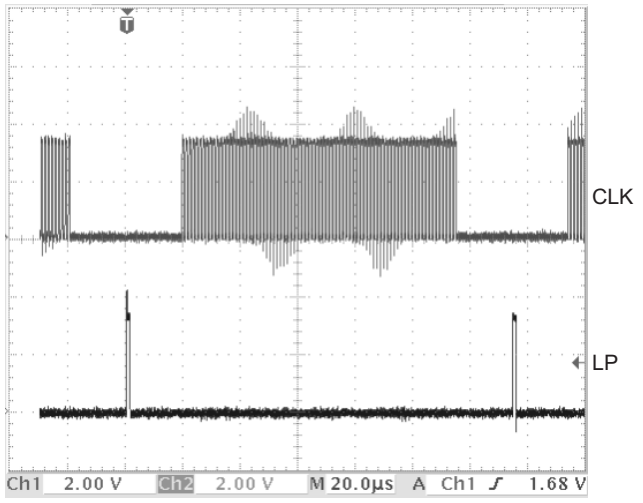

Figure 6-28 *LCD control signals, oscillogram #5.*

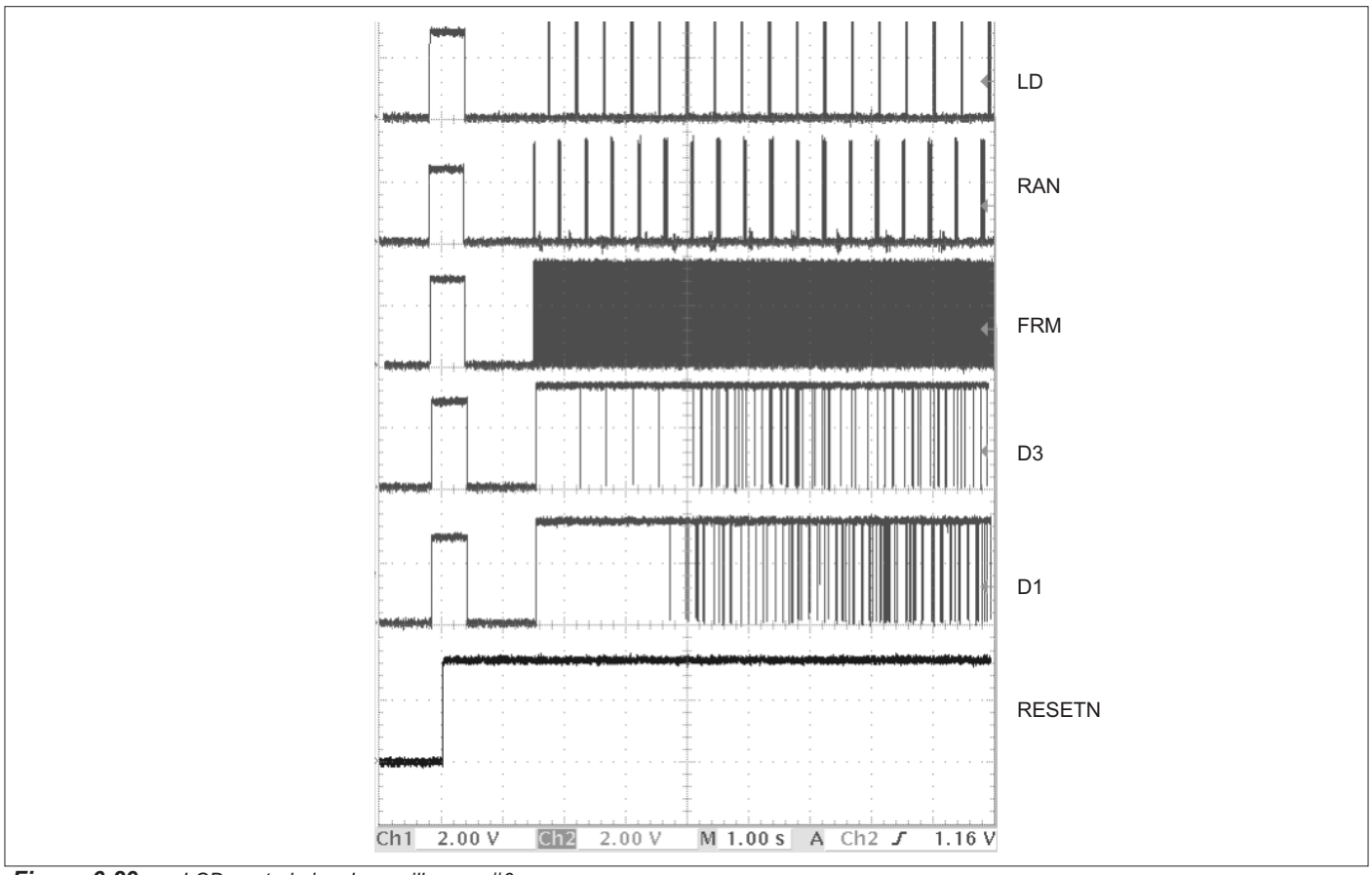

Figure 6-29 *LCD control signals, oscillogram #6.*

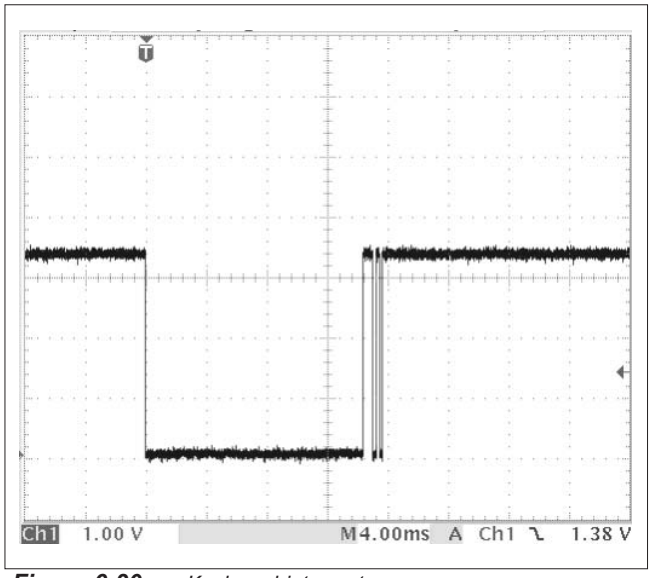

Figure 6-30 *Keyboard interrupt.*

Microprocessor Bus & Interfaces

The instrument has a conventional 16-bit microprocessor bus with 16 bits bidirectional data signals, 5 bits address signals, Chip Selects and wrn and rdn signals. It connects the processor to the FPGA, the GPIB and the USB. See Figure 6-34.

The FPGA connection has 16 data bits, 5 address bits, chip select, wrn and rdn. The FPGA is controlled by the processor via the bus. Measuring functions are selected, for instance. The FPGA is controlled between each measurement or block of measurements. An interrupt signal from the FPGA is connected to the processor. See Figure 6-36 for a typical timing diagram.

The connection to the USB has 16 data bits, 1 address bit, chip select, wrn and rdn. An interrupt signal from the USB IC is connected to the processor. See Figure 6-38 for a typical timing diagram. The USB IC is a complete USB unit. It is not powered from the USB bus. The USB IC (U34) has a 6 MHz oscillator. Check at C416.

The connection to the GPIB has 8 bits, 5 address bits, chip select, wrn, rdn and a special control signal for the level shifting IC (U38). U38 is a buffer between the logic level of +3.3 V for the processor and the logic level of +5 V for the GPIB IC (U37). An interrupt signal from the GPIB IC is connected to the processor. See figure ee for a typical timing diagram. The GPIB IC is a complete GPIB unit. The GPIB IC (U37) has a 40 MHz oscillator. Check at TP20.

Only the selected interface is involved in communication on the microprocessor bus.

Since both interfaces consist of only one IC each, troubleshooting is fairly simple. Check that the oscillator (40 MHz or 6 MHz) is running. Check that the processor communicates with the selected IC. Make sure the external controller (GPIB or USB) and the interconnection cable used are OK.

There is a separate bus for transfer of the measurement result data from the FPGA to the processor. This bus is 32 bits wide and has a clock of its own, FCLK (U11:101). A signal from the processor, FEMPTY (X28), indicates to the FPGA that a new packet of 8 words of 32 bits can be transferred. This is done with the FWR signal (X30) together with the FCLK. The FPGA can call for attention via an interrupt request signal, FFIQ (X31). This is done when the FPGA would like to transfer a packet to the processor. See Figure 6-41 for a typical timing diagram.

Another bus from the microprocessor is the SPI bus. It is a serial bus with one data signal and one clock signal that are common for all ICs connected to the bus. A separate load signal for each IC controls the loading of the data. Connected to the SPI bus are (See Figure 6-42 to Figure 6-45):

- The 100 MHz PLL IC (U9). The SPI bus is used only for initialization after power on.
- The optional oven oscillator IC (U5). The SPI bus is used for initialization after power on and during a timebase calibration.
- The trigger levels IC (U46).

The last bus is the I^2C bus. It is also a serial bus with two signals, SDA and SCL. Each connected IC has a unique address. The message sent includes the address, and only the addressed IC will listen to the message and respond by sending an acknowledge to the master. Then it will react accordingly.

Introduction to the I^2C Bus

The I^2C bus is a 2-line serial bus for the communication between the ICs. The microprocessor controls the communication by means of the clock line SCL. One or more slaves can read or write on the data line SDA.

The SDA and SCL are high at standby. All ICs connected to the bus can sink SDA to low as they are interconnected via open collector outputs. The microprocessor starts and stops the communication by sending terms of start and stop:

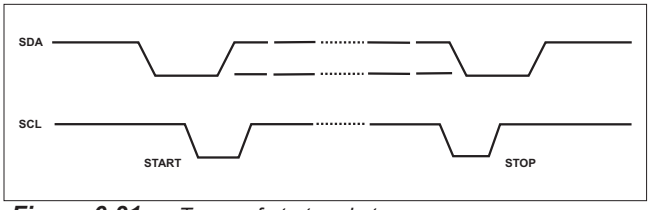

Figure 6-31 *Terms of start and stop.*

During transmission the SDA can be changed only when the SCL is low.

The microprocessor always begins to send the address information. The format of this address information is seven address bits, one read/write bit, and one acknowledge bit.

The addressed slave accepts by keeping the SDA line low while the acknowledge bit (ACKN in) is sent by the microprocessor.

Example of addressing (address 30H):

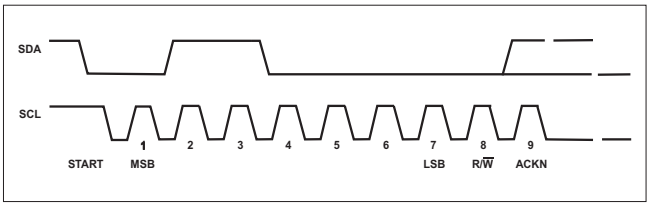

Figure 6-32 *Addressing.*

The read/write bit R/$\overline{W}$ has the following meaning:

R/$\overline{W}$ = 1 means information from the slave to the µprocessor
R/$\overline{W}$ = 0 means information from the µprocessor to the slave.

The data information is sent after the address information. The format of the data information is eight data bits followed by one acknowledge bit. The reciever accepts by keeping the SDA line low while the acknowledge bit (ACKN in) is sent.

Example of data transmission (data 9BH):

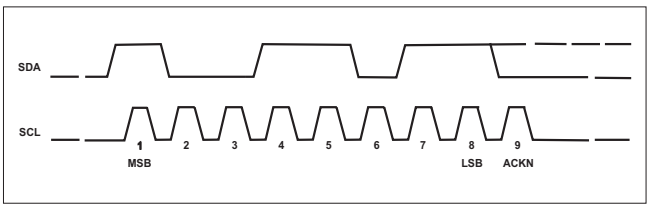

Figure 6-33 *Data transmission.*

The processor is the Master on the I^2C bus. Slaves on the bus are:

- The digital I/O IC U40 with address 20hex. It controls the loading of the FPGA at initialization after power on, it controls the relays and filters in the input amplifiers, and it reads the prescaler code at initialization after power on.
- The temperature measuring IC U39 with address 48hex.
- The digital I/O IC U3 with address 21hex. It switches the LCD display on after power-on initialization, it scans the keyboard on the display circuit board.

The bus is connected to the prescaler connector J15 for future use.

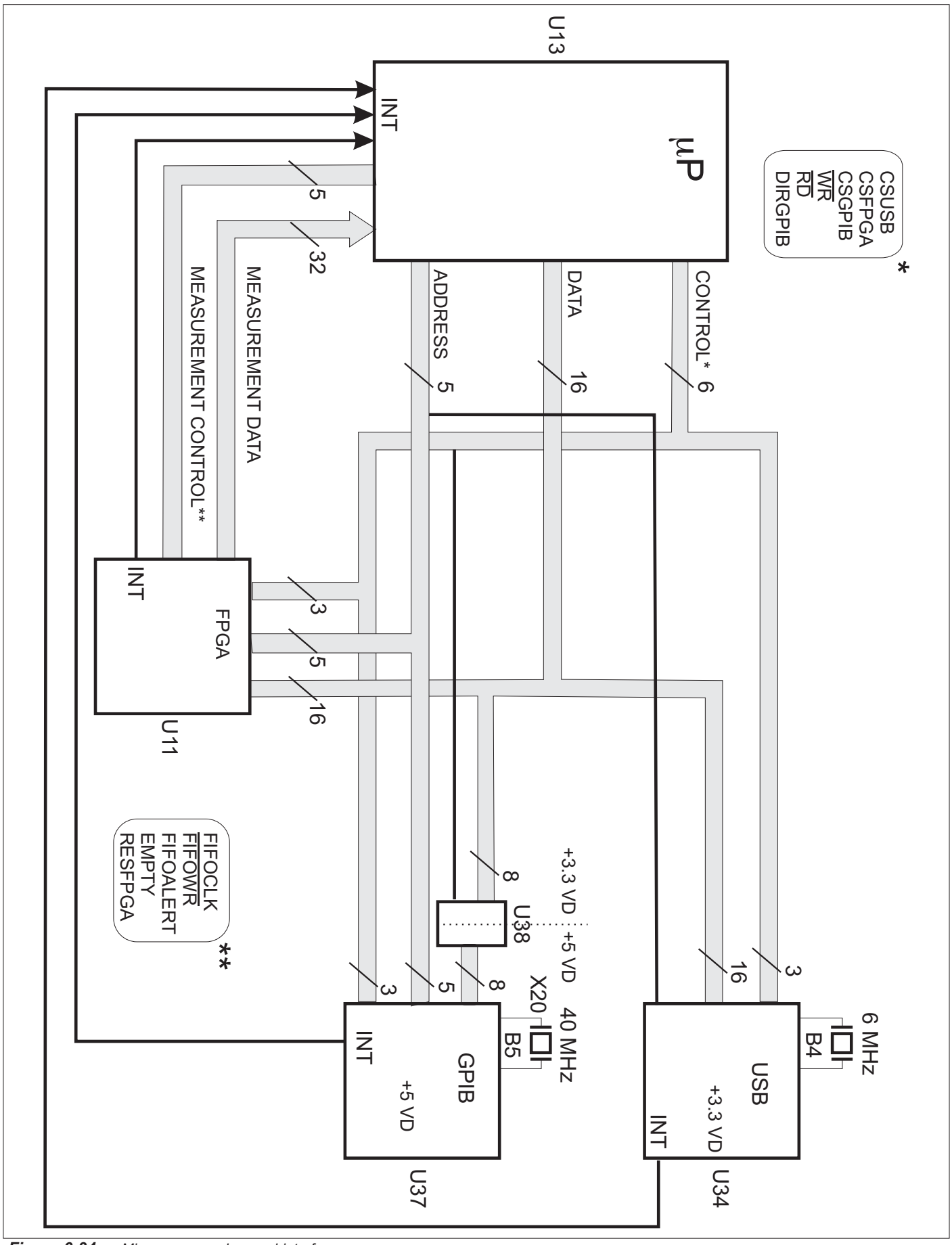

Figure 6-34 *Microprocessor bus and interfaces.*

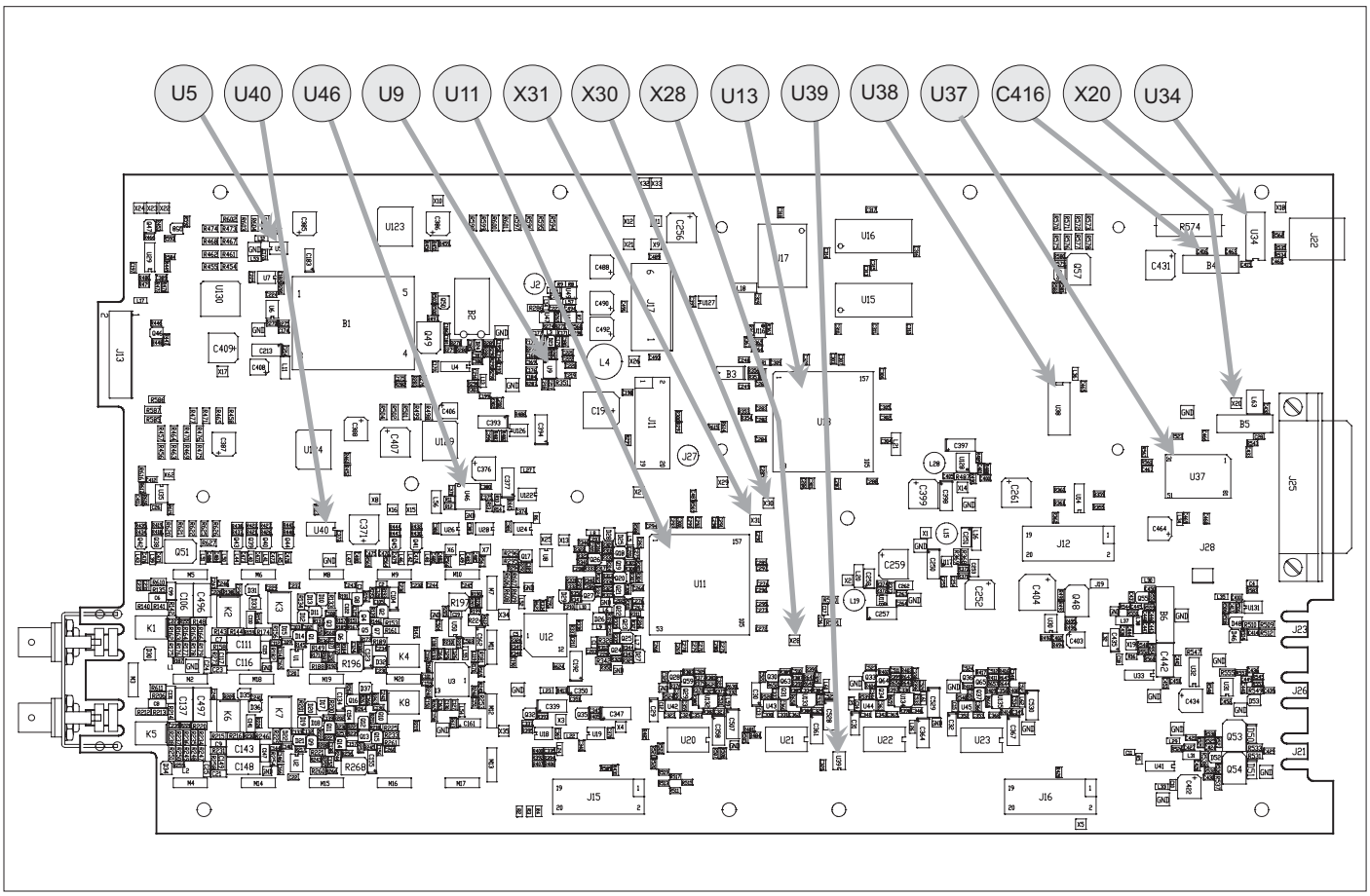

Figure 6-35 *Important locations for the microprocessor and its buses and interfaces.*

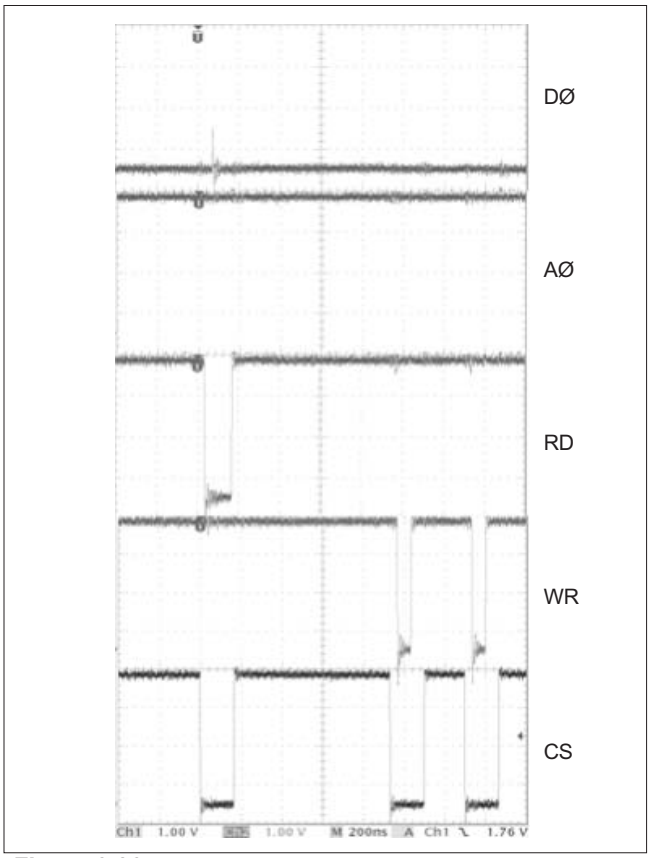

Figure 6-36 *Microprocessor bus - FPGA timing - Single Period.*

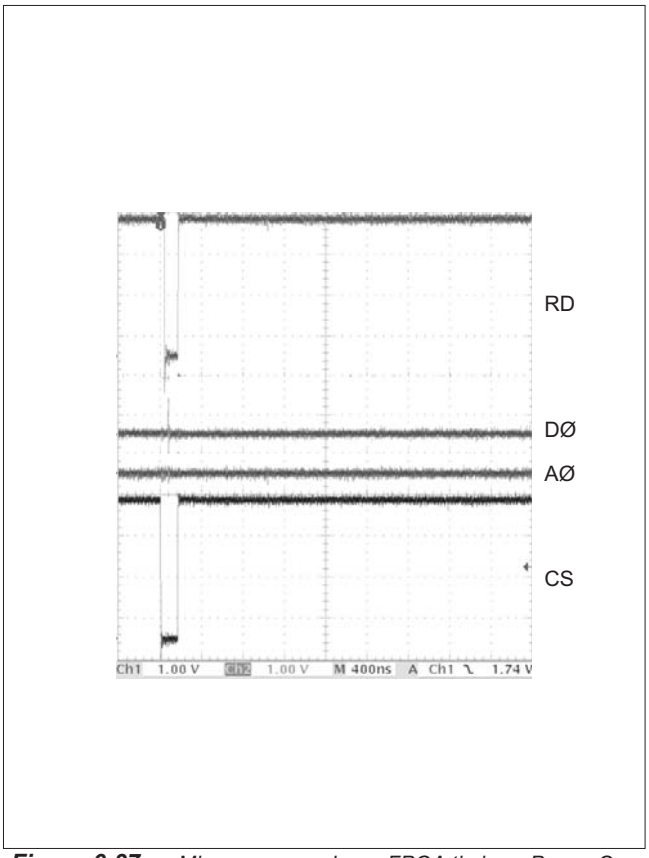

Figure 6-37 *Microprocessor bus - FPGA timing - Power On.*

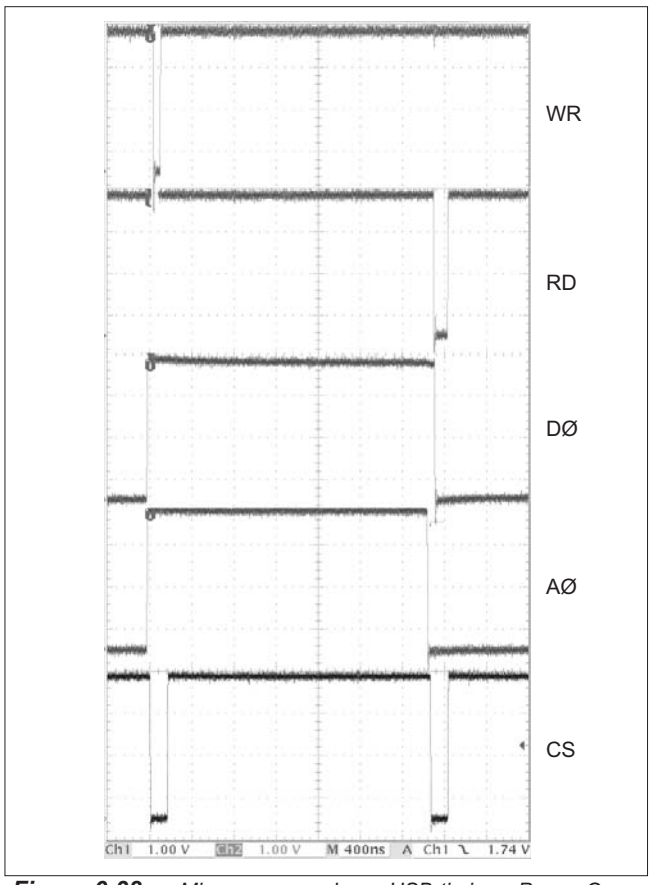

Figure 6-38 *Microprocessor bus - USB timing - Power On.*

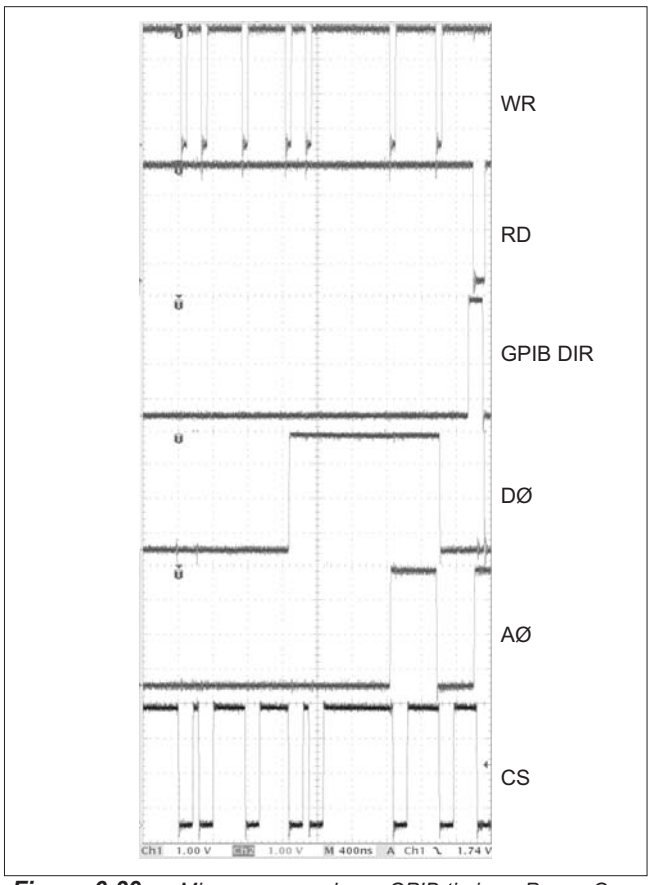

Figure 6-39 *Microprocessor bus - GPIB timing - Power On.*

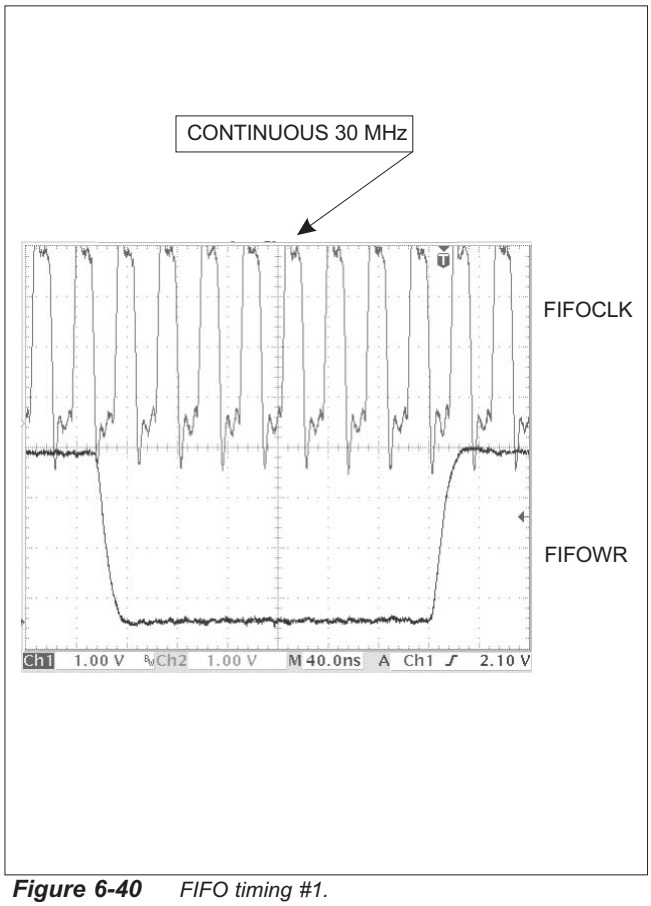

Figure 6-40 *FIFO timing #1.*

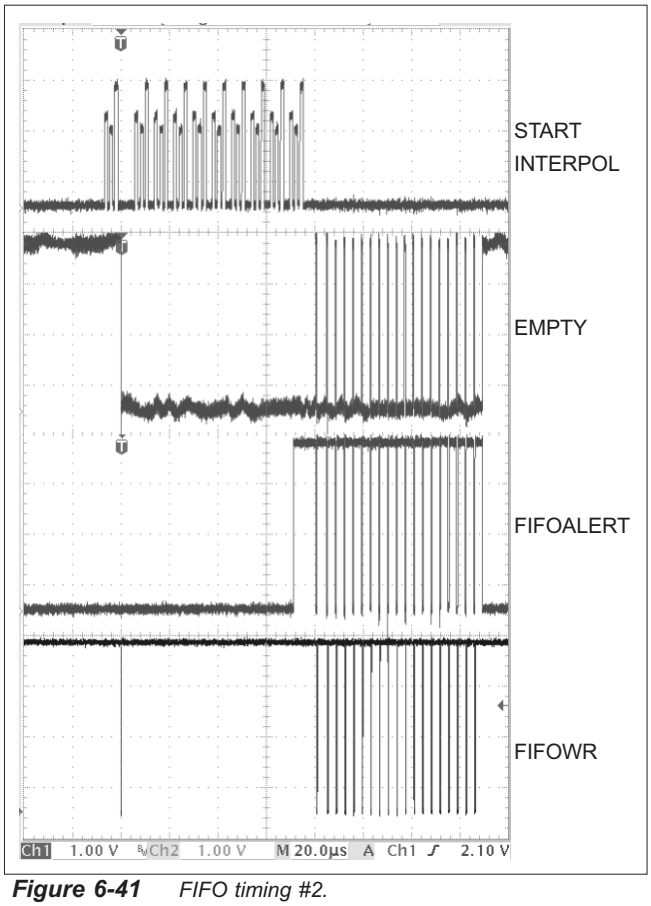

Figure 6-41 *FIFO timing #2.*

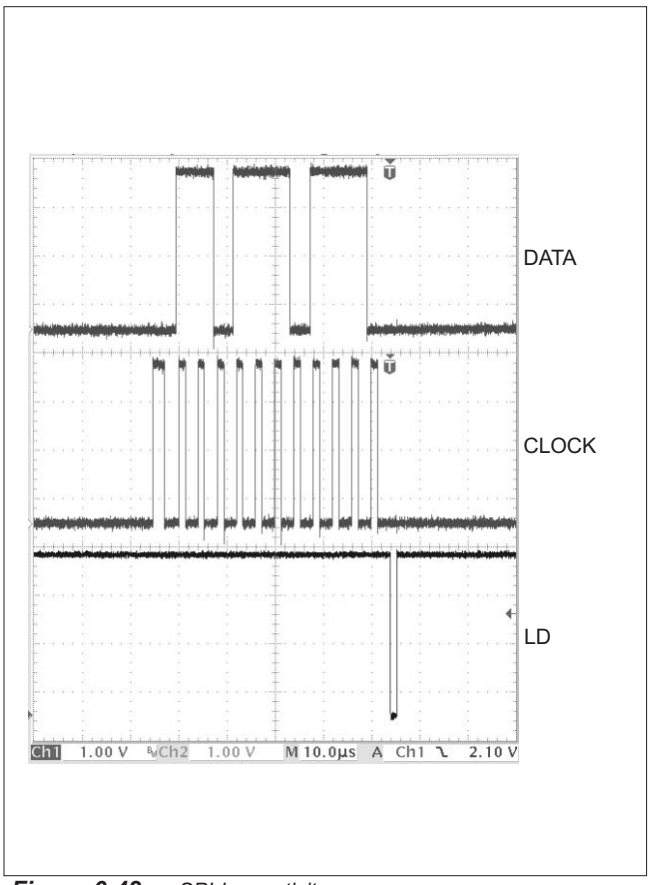

Figure 6-42 *SPI bus activity - oven.*

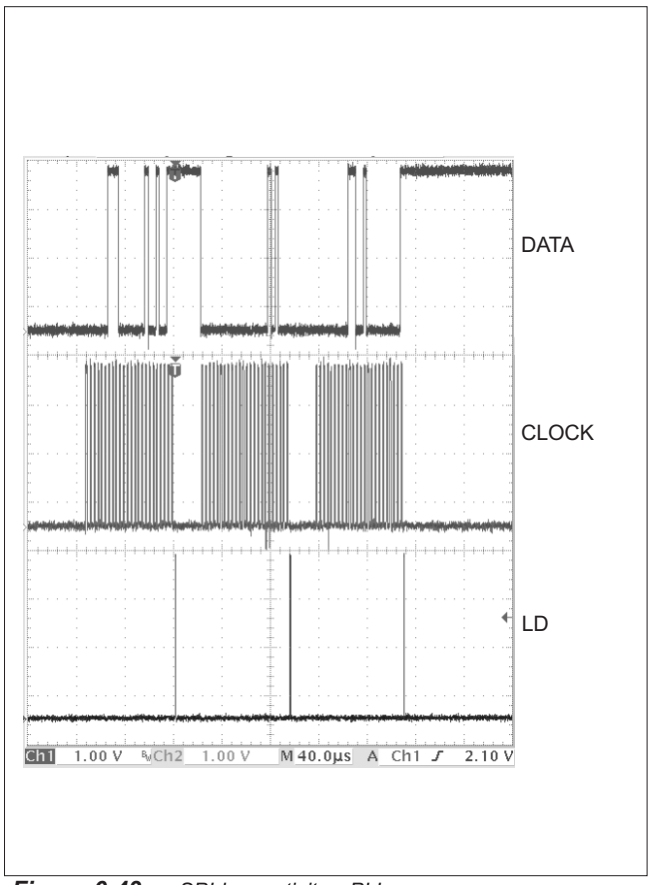

Figure 6-43 *SPI bus activity - PLL.*

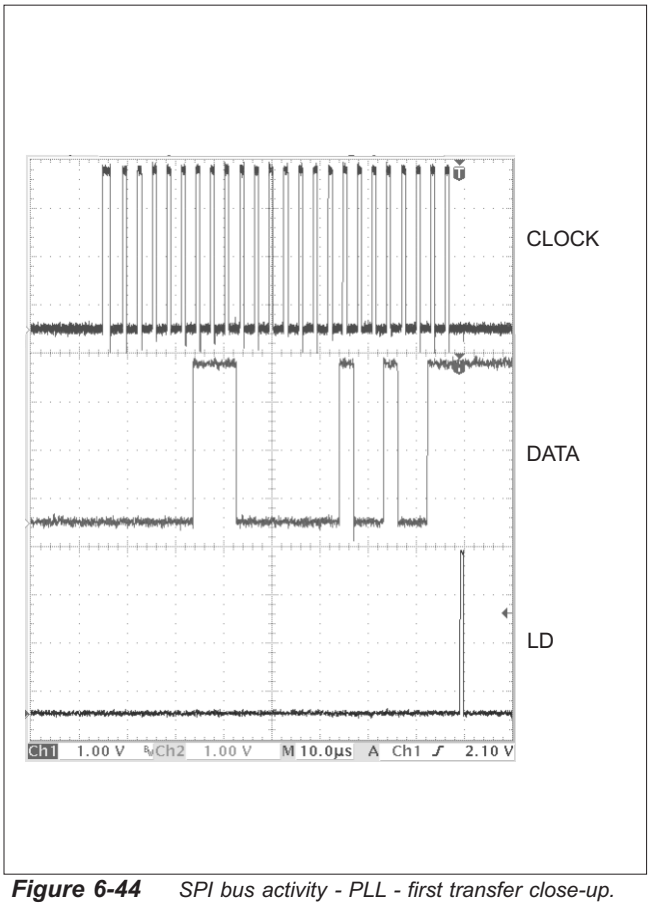

Figure 6-44 *SPI bus activity - PLL - first transfer close-up.*

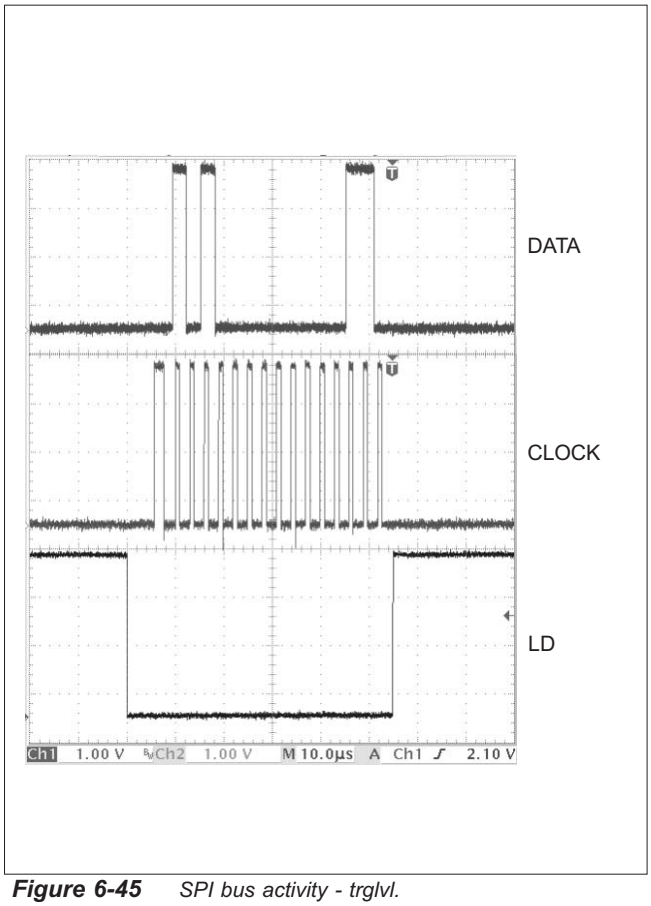

Figure 6-45 *SPI bus activity - trglvl.*

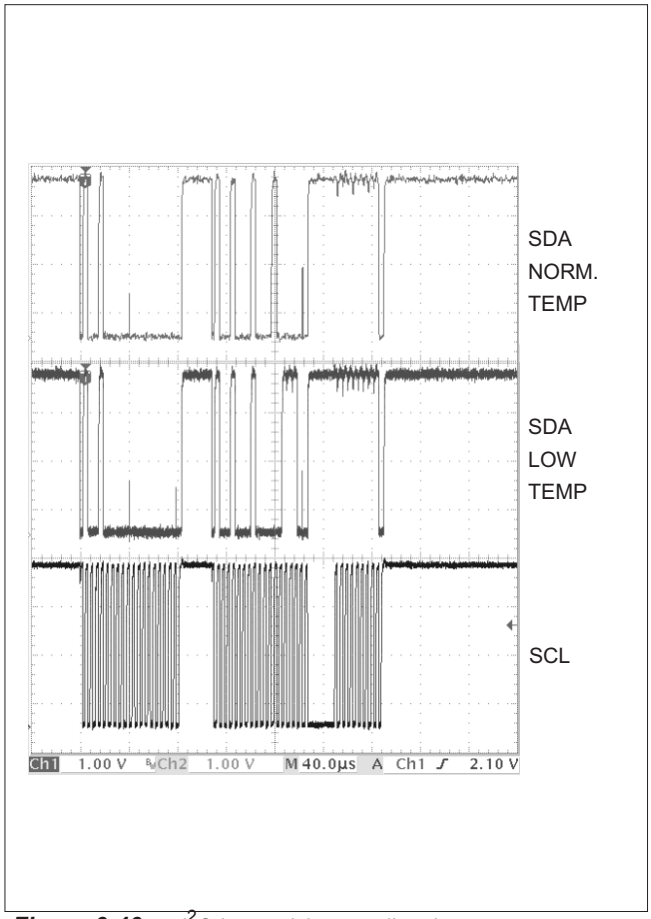

Figure 6-46 *I^2C bus activity - reading the temperature.*

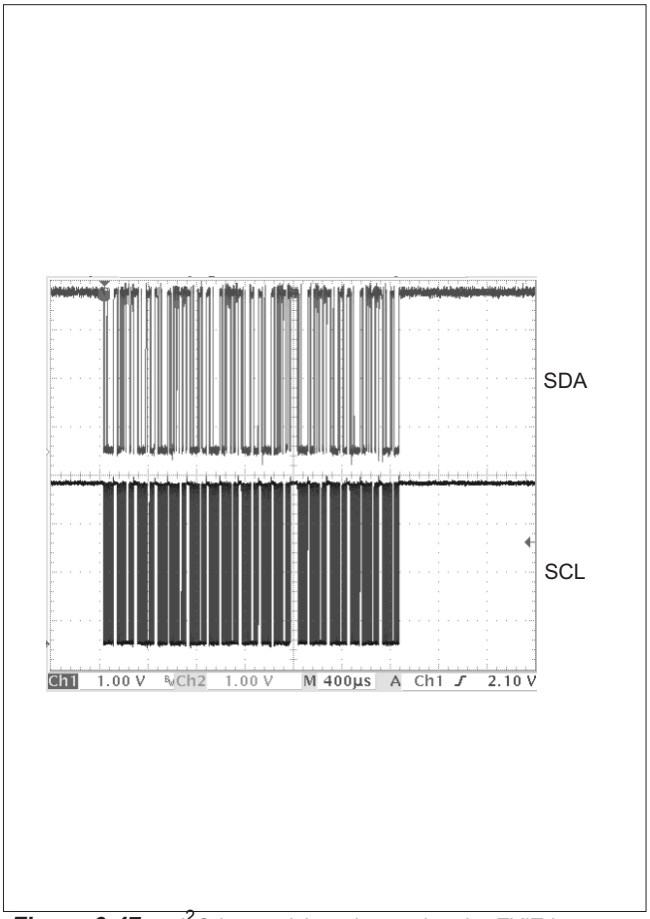

Figure 6-47 *I^2C bus activity - depressing the EXIT key.*

Measuring Logic

The measurements are made in the FPGA. Only four interpolators are external to the FPGA. They increase the basic measurement resolution from 10 ns (100 MHz measurement clock) to less than 100 ps. Different combinations of interpolators are used for different measurement functions; two, three or four in conjunction. The input signals come from the input amplifiers. A, B and SR are differential LVPECL inputs. C, the prescaler input, is a single-ended LVTTL input. The measuring logic also provides three LEDs on the front panel with control signals.

The interpolator transforms a pulse width between 20 and 33 ns to a voltage. This voltage is read by an ADC. The interpolator is calibrated by reference pulses having a width of 20 and 30 ns . The measurement pulse varies between 22 and 32 ns typically. The ADC has two reference voltages, the lower limit and the upper limit. The interpolated voltage must never fall outside these limits.

Select the default setting from the front panel. Apply a 10 MHz sinewave signal (stable low jitter signal) to input A. The signal should be found at the pins of the FPGA. Check that the measurement signal is present on pins 17 and 18 (differential input) on the FPGA U11.The trigger indicator LED A on the front panel should blink. The gate indicator on the front panel should also blink and the display should show the measurement result. In this setting the S/R flip-flop U12 is used. Check that the measurement signal is present on pins 30 and 31 (differential input) on the FPGA U11.

Move the 10 MHz sinewave signal to input B. Change the measurement function to Frequency B. Check that the measurement signal is present on pins 20 and 21 (differential input) on the FPGA U11. The trigger level LED B and the gate indicator LED should blink and the display should show the measurement result.

Move the 10 MHz sinewave signal back to input A. Change the measurement function to Period Single A. Now the S/R flip-flop should not be used, check the control signal at R623, it should be -1.6 V (on is -1.0 V). Select statistics. The std deviation should be less than 100 ps.

Change the measurement function to Time Interval A - A. Select Statistics Mode. Check that the standard deviation is less than 100 ps. Measure at pin 8 of the ADCs U23, U22, U21 and U20. Two types are current, ADC10461 and ADC1061. See Figure 6-49 for a typical timing diagram with ADC10461. Figure 6-50 shows an example with ADC1061. Check the upper (TP3) and lower (TP4) voltage limits of the ADCs. They should be approximately 3.5 - 3.6 V and 1.1 - 1.4 V. The important thing is that the lowest voltage pulse on any

pin 8 of the ADCs (U23, U22, U21, U20) should be at least 0.2 V above the lower limit and that the highest voltage pulse on any pin 8 of the ADCs should be at least 0.3 V below the upper limit. If an interpolator has a voltage pulse outside the limits the measurement result will be wrong. Figure cc shows the signals on an ADC.

The signal from the prescaler is connected to pin 22 (single-ended) of U11. It comes via a level converter. Check the input signal to the converter at R335 (PECL levels).

If the FPGA or a part in the interpolators has been changed or repaired, a calibration of internals must be performed afterwards. See Chapter 7.

Note The interpolator design has varied slightly in the course of time, but the pulses in Figures 6-49 and 6-50 are very little affected.

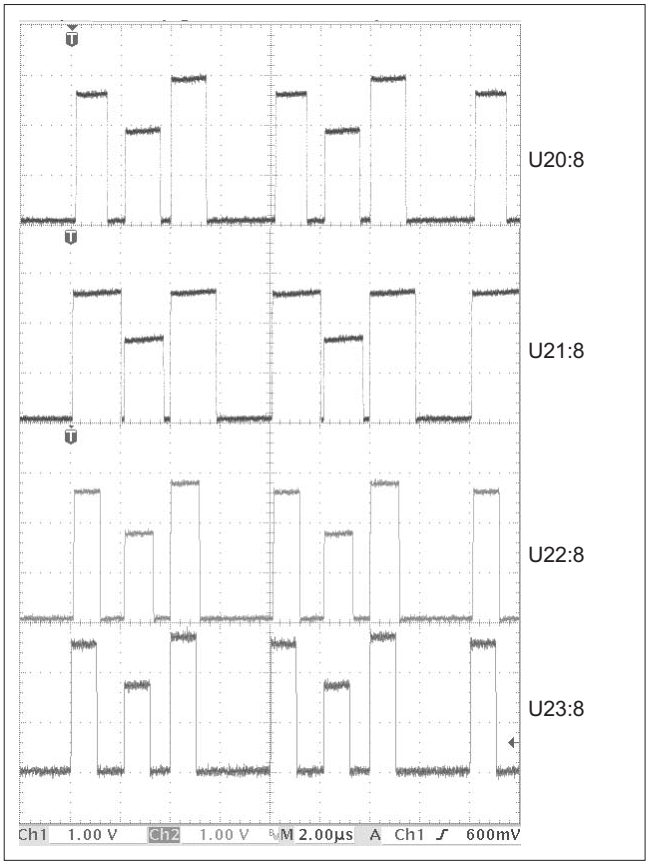

Figure 6-49 *ADC 10461 behavior. Time A-A, 10 MHz in.*

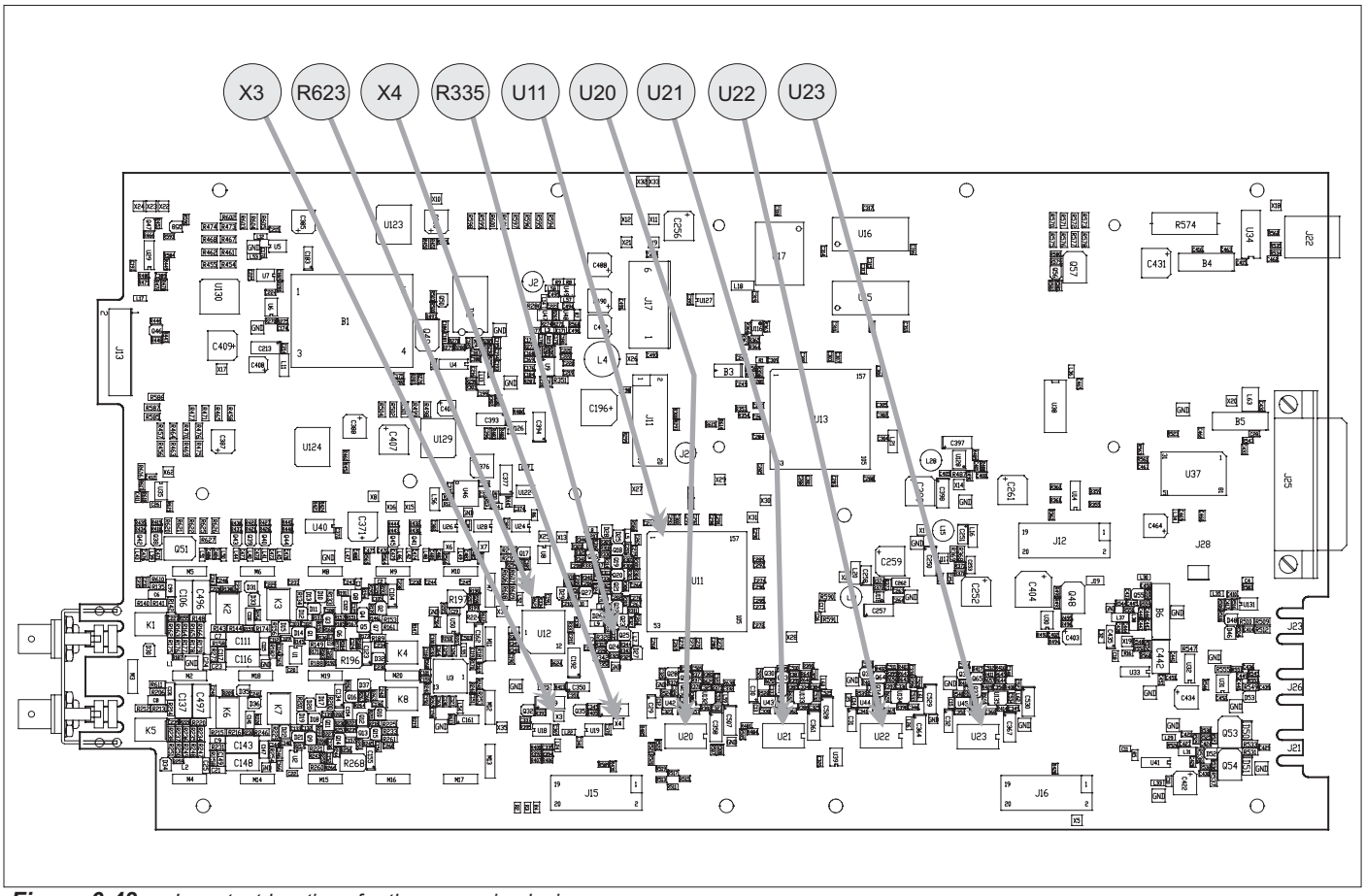

Figure 6-48 *Important locations for the measuring logic.*

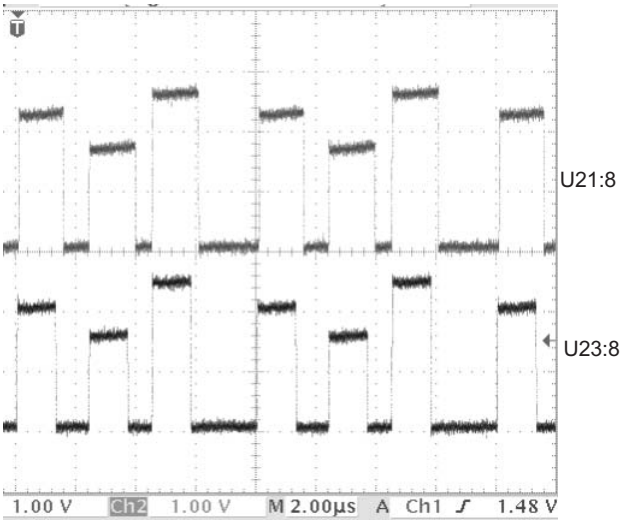

Figure 6-50 *ADC 1061 behavior. Time A-A, 10 MHz in.*

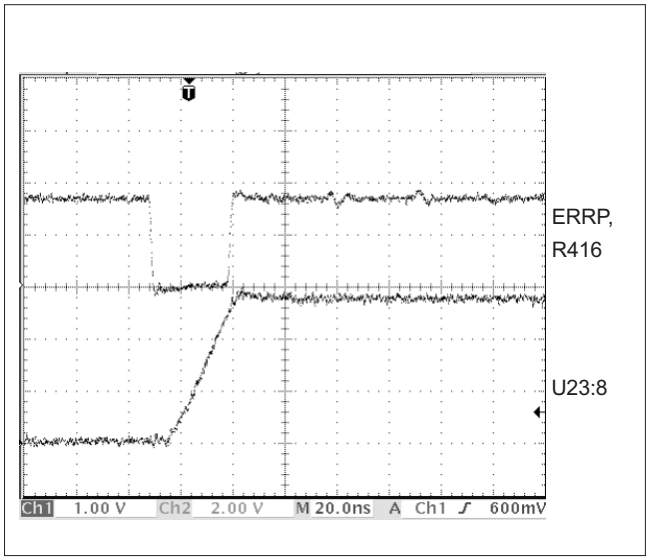

Figure 6-52 *Close-up of error pulse and S/H output.*

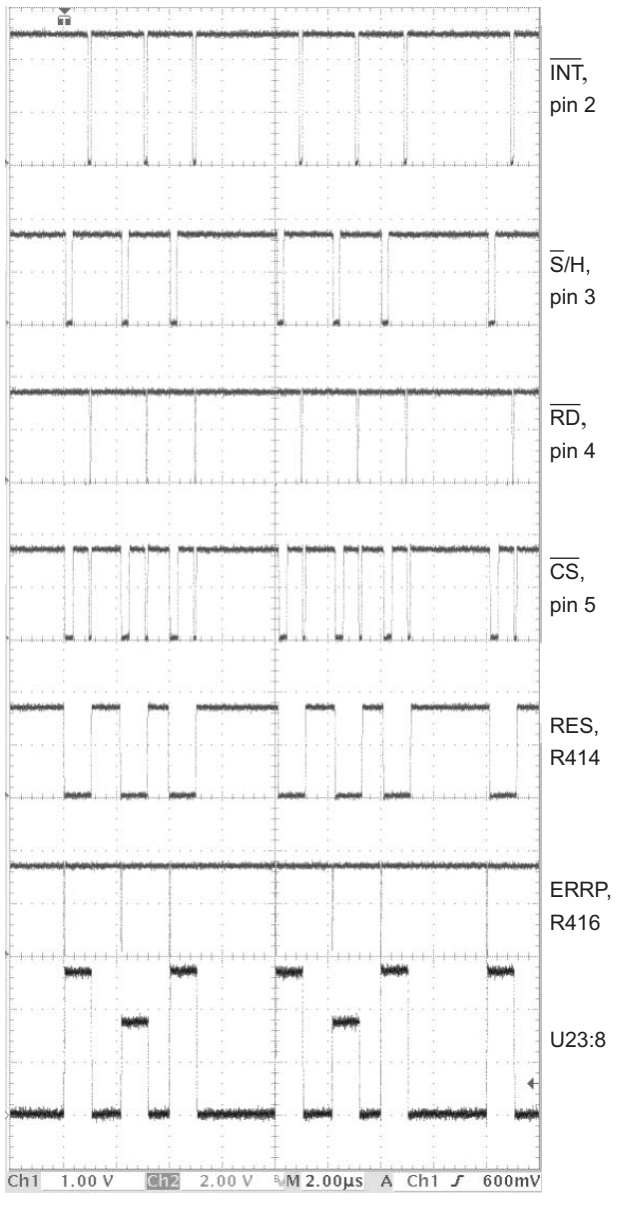

Figure 6-51 *Different signals around an ADC.*

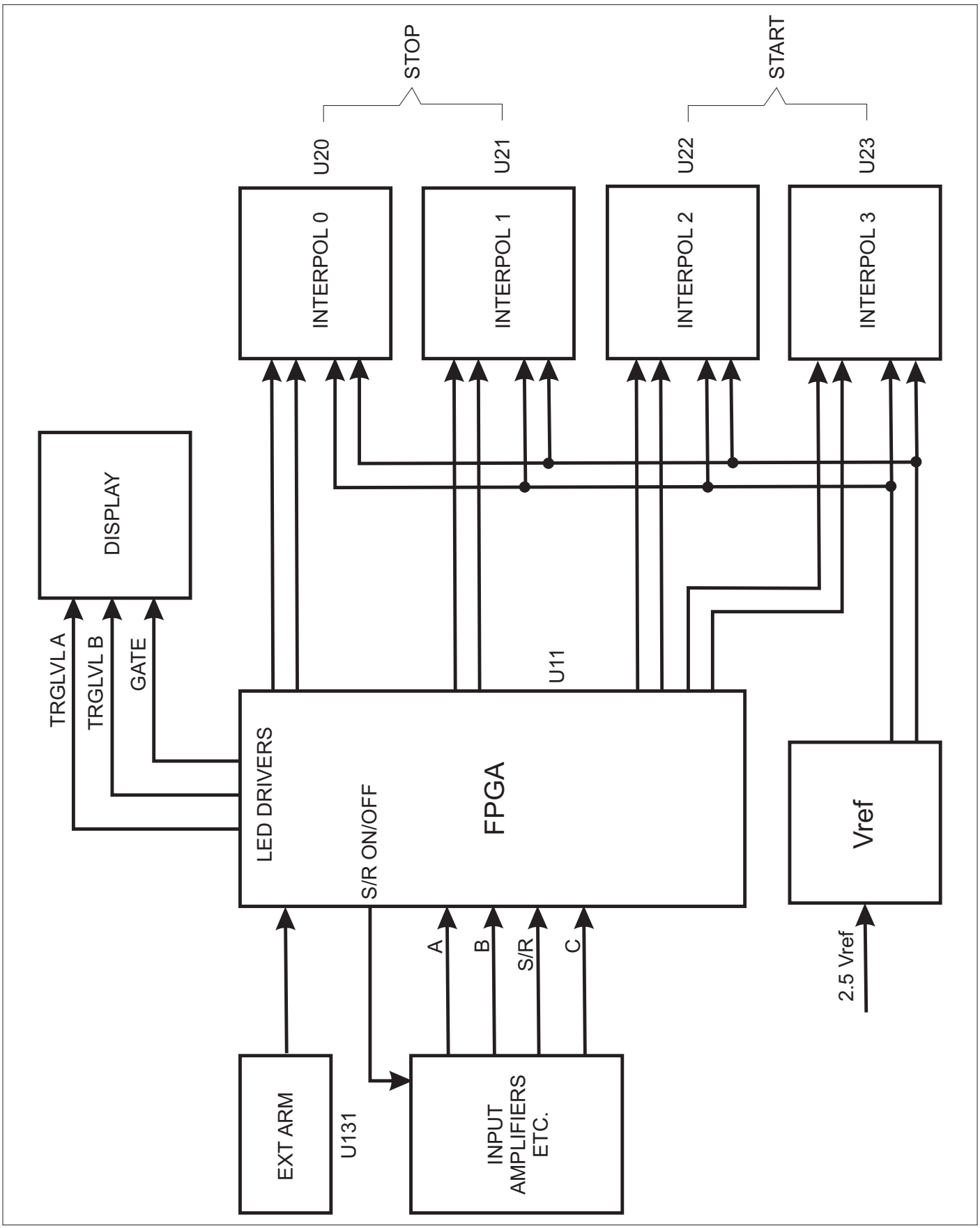

Figure 6-53 *Measuring logic, block diagram.*

Version B

The descriptions in this section apply to instruments having a Sharp microprocessor.

See General Information on page III for details on relevant serial numbers etc.

Troubleshooting

General

The '90' is a highly integrated Timer/Counter in which a dedicated FPGA counter circuit handles the signal processing, and a microcontroller does the postprocessing and supervising jobs. A number of additional functional units support these basic tasks, for instance power supply, reference oscillator, wideband input amplifiers, comparators, memory (RAM & ROM), digital/analog converters, etc.

The units are treated from a troubleshooting point of view in this chapter, which means that units described earlier should be considered faultless before troubleshooting on units described later.

WARNING: Live parts and accessible terminals which can be dangerous to life are always exposed inside the unit when it is connected to the line power. Use extreme caution when handling, testing or adjusting the counter.

Where to Start

After reading the safety instructions, continue with this chapter for troubleshooting and repair instructions. When you have fixed the instrument, always do the Safety Inspection and Test after Repair, as described later in this Chapter. Then do the checks in Chapter 2, Performance Check. Recalibrate if required by following the adjustment instructions in Chapter 7, Calibration Adjustments.

	Positive ECL	Negative ECL	CMOS	TTL
Supply voltage	+5 V	-5 V	+5 V	+5 V
Signal ground	0 V	0 V	0 V	0 V
Input voltage				
High, VIH	>+3.9 V	>-1.1 V	>+4 V	>+2 V
Low, VIL	<+3.5 V	<-1.5 V	<+1 V	<+0.8 V
Output voltage				
High, VOH	>+4 V	>-1 V	>+4.9 V	>+2.7 V
Low, VOL	<+3.3 V	<-1.7 V	<+0.05 V	<+0.4 V
Bias ref. voltage, VBB	+3.7 V	-1.3 V	-	-

Table 6-3 *Logic levels.*

Logic Levels

The '90' contains logic of different families. The levels of the standard families are listed in Table 6-3. In addition to these families there is also low-level logic requiring lower supply voltages, e.g. +3.3 V and +1.8 V.

Required Test Equipment

To be able to test the instrument properly using this manual you will need the equipment listed in Table 2-1. The list contains the critical parameter specifications.

Operating Conditions

Power voltage must be between 90 V_{AC} and 260 V_{AC}. The instrument adapts automatically to the applied voltage.

Basic Functional Units

These are the units that are described in this chapter with reference to the page where the section starts:

- Power Supply (p. 6-32)
- Input Amplifiers (p. 6-36)
- Timebase Reference Circuits (p. 6-40)
- Prescalers (p.6-43)
- Microprocessor & Memories (p. 6-43)
- Microprocessor Bus & Interfaces (p. 6-49)
- Measurement Logic (p. 6-55)

Power Supply

The DC voltages needed in the instrument are generated from the three main voltages of the AC/DC module.

The instrument has only a secondary power switch, i.e. the AC/DC module is always operating if line power is applied. The three output DC voltages (+5 V, +15 V, -15 V) from the module are present on the main circuit board. When switched off, the instrument is in the standby mode. In this mode only

the ON/OFF circuitry and the optional oven oscillator are powered.

The AC/DC module should not be repaired. Not even the built-in fuse should be replaced. Built-in circuits protect against external overloads, so a blown fuse indicates that a severe internal fault has occurred. Replace the complete module instead.

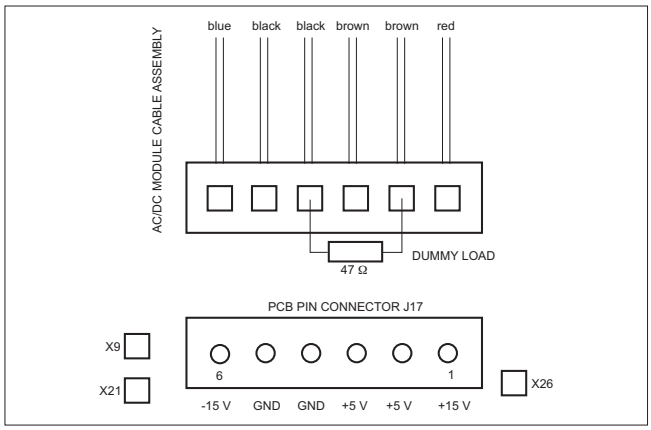

Figure 6-55 *Dummy load connection.*

Test the AC/DC module by measuring the three DC voltages in TP9 (+5.1 ± 0.05 V), TP21 (-15 ± 1 V) and TP26 (+15 ± 1 V) on the main circuit board. See Figure 6-55. Note that there is a +5 V trimmer on the module. If the +5 V is not correct, disconnect the cable to J17 on the main circuit board. Put a 47 Ω 1 W resistor on the connector according to Figure 6-55. Measure on the connector +5.1 ± 0.05 V, +15 ± 1 V and -15 ± 1 V.

It can be difficult to measure the resistance in the supply connector J17 on the main circuit board, because charges are kept by capacitors some time after line power is removed. Remove the cable from the AC/DC module. The resistance between +5 V and ground should be approximately 700 Ω. See Figure 6-55. In a timer/counter with all capacitors uncharged, +15 V and -15 V should be >1 MΩ.

Another way to test J17 is to connect 3 DC voltages from a separate bench power supply directly to J17 (suitable connector MOLEX 09-91-0600). See Figure 6-55. The currents drawn from the different supply voltages depend on options installed. Before making this measurement, you should remove any prescaler option.

A timer/counter without options gives the following typical results:

+5 V	0.7 A
+15 V	0.3 A
- 15 V	0.4 A

The oven oscillator increases the + 15 V current between 0.35 A (cold) and 0.1 A (warm).

A block diagram of the secondary power supply is shown in Figure 6-54. All secondary voltages are switched off in standby mode except +12 VU for the optional oven oscillator.

The ON/OFF circuitry controls the ON and OFF of the secondary voltages. Its own supply voltage is always ON, as long as the instrument is connected to line power. See Figure 6-59.

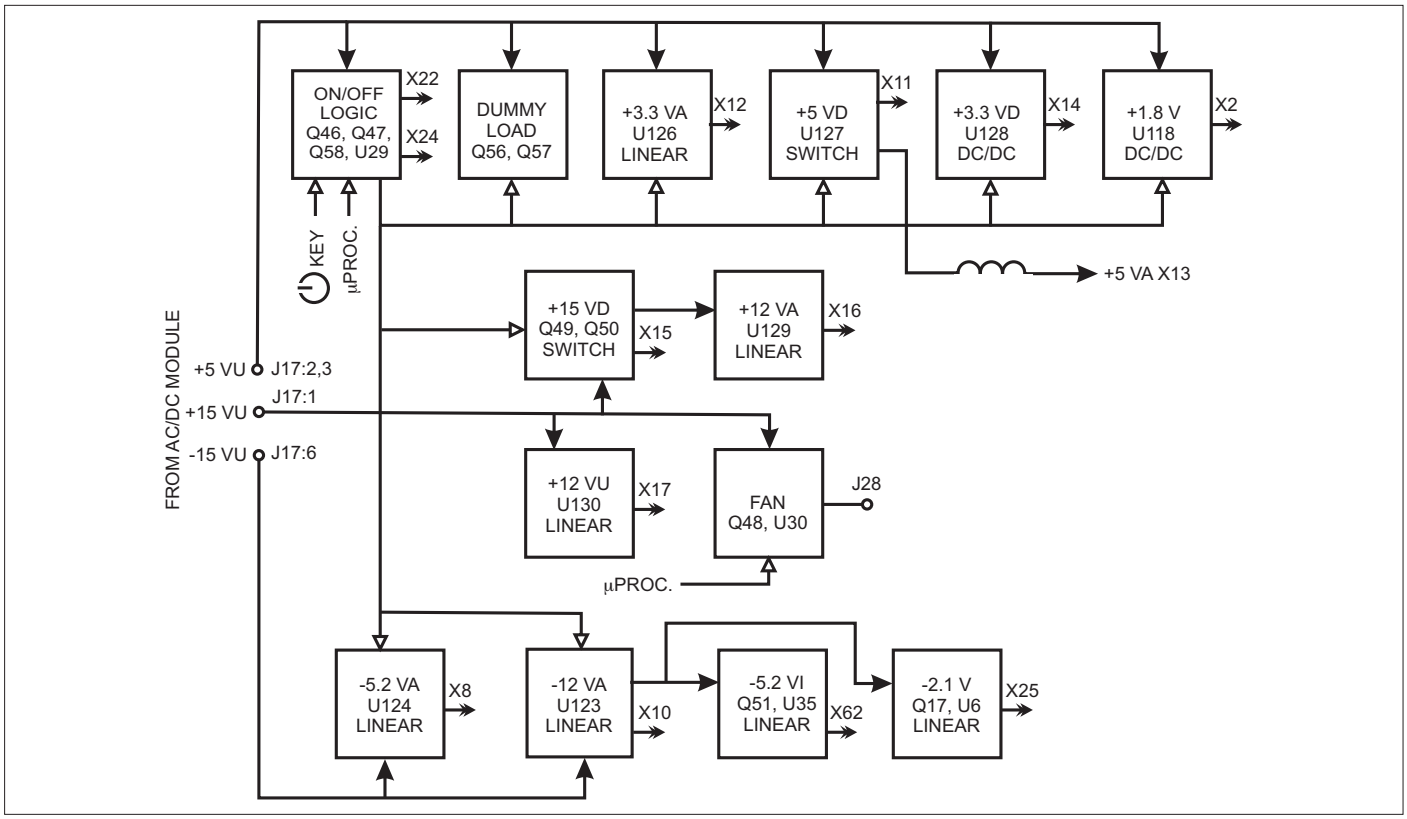

Figure 6-54 *Power distribution*

On connection of line power, R478 and C389 keep the RESETN input of the flip-flop U29 low. This sets the QN output of U29 high. Via Q47 (output signal low) and Q58 (output signal high) the secondary power supply will be set in ON mode. To switch to the standby mode, the processor sets the SETN input of U29 low. This results in the QN output being low and the secondary power supply being set to standby mode via Q47 (output signal high) and Q58 (output signal low). In standby mode a bleeder circuit on +5 VU is connected. It draws approximately 100 mA to stabilize the AC/DC module. The standby LED on the front panel is switched on. To switch to ON mode from standby mode, a negative pulse, generated by pressing the ON/OFF key on the front panel, is connected to the RESETN input of U29.

Linear regulators are used for some voltages to ensure minimum noise. Check the TPs below:

X12: +3.3 VA (from +5 VU)
X8: -5.2 VA (from -15 VU)
X10: -12 VA (from -15 VU)
X62: -5.2 VI (from -12 VA)
X25: -2.1 V (from -12 VA)
X16: +12 VA (from +15 VD)

X17: +12 VU (from +15 VU) (to oven oscillator, not switched off in standby mode)

For digital and general use some voltages are generated by DC/DC converters. Check the following TPs:

X14: +3.3 VD (from +5 VU)
X2: +1.8 V (from +5 VU)

Some voltages derived directly from the AC/DC module are used as secondary supply voltages without further regulation, and they have semiconductor switches in series to make it possible to shut them off in standby mode. Check the TPs below:

X15: +15 VD (from +15 VU)
X11: +5 VD (from +5 VU)
X13: +5 VA (from +5 VD)

These 12 secondary voltages are used all over the instrument. All secondary supply voltage lines are segmented into branches with ferrite beads. See the schematics. This makes it easier to isolate short circuits by removing ferrite beads temporarily.

The microprocessor, U13, has an internal linear regulator that generates +1.8 V from +3.3 V. This voltage is used by the processor core and can be checked at X66.

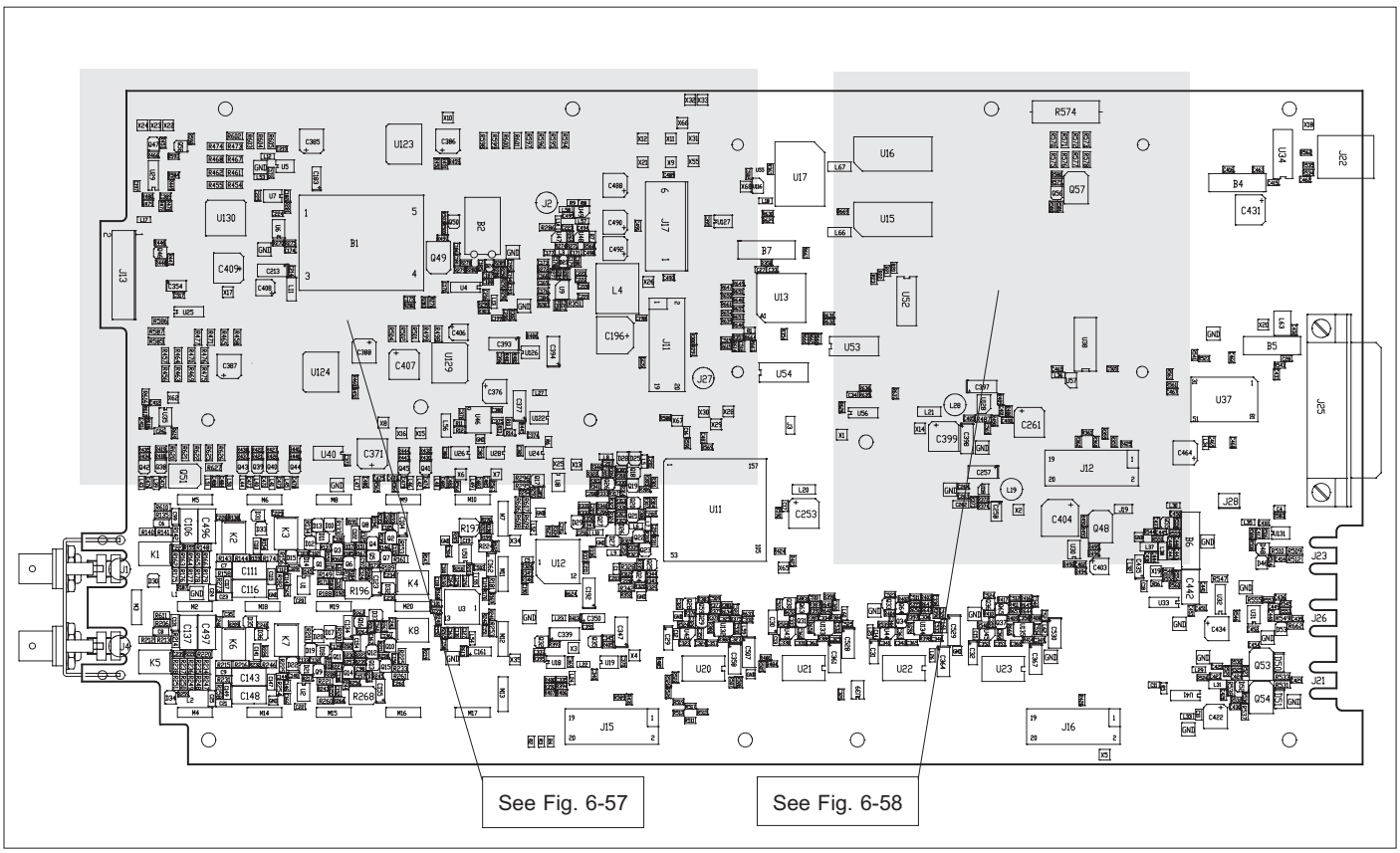

Figure 6-56 *PCB1 survey*

Fan Control

The fan is connected to +15 VU over a speed control circuit. It is only ON if a control signal from the processor is present. The first 8 minutes after power-up the fan will run at a fixed speed, fed with +8.3 V. After that the fan is temperature controlled. The processor reads the temperature from U39 via the I^2C bus. Depending on the temperature, the fan is fed with a DC voltage between 8 and 13.5 V. The processor uses a PWM signal that is filtered to control the fan.

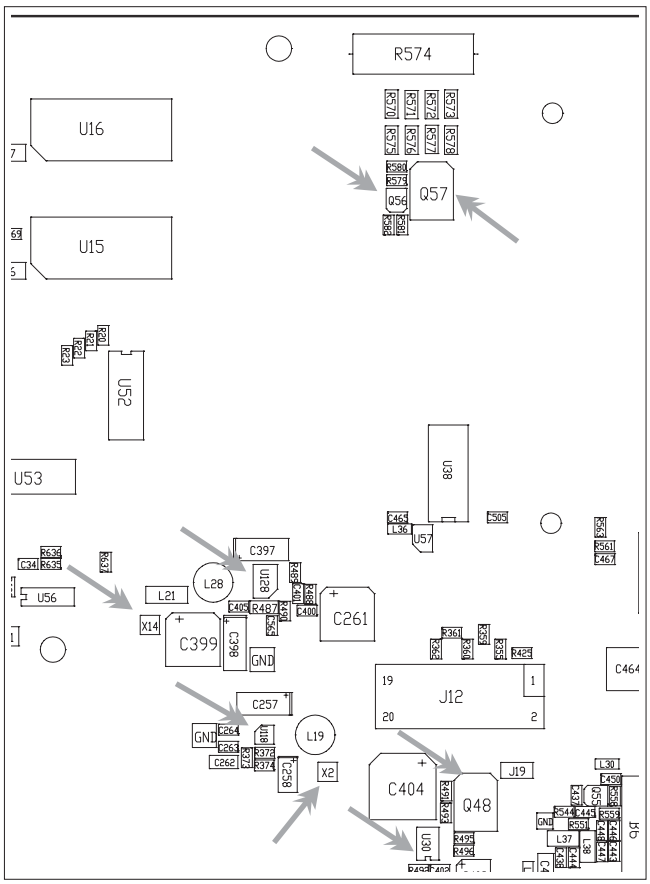

Figure 6-58 *Important power supply locations #2.*

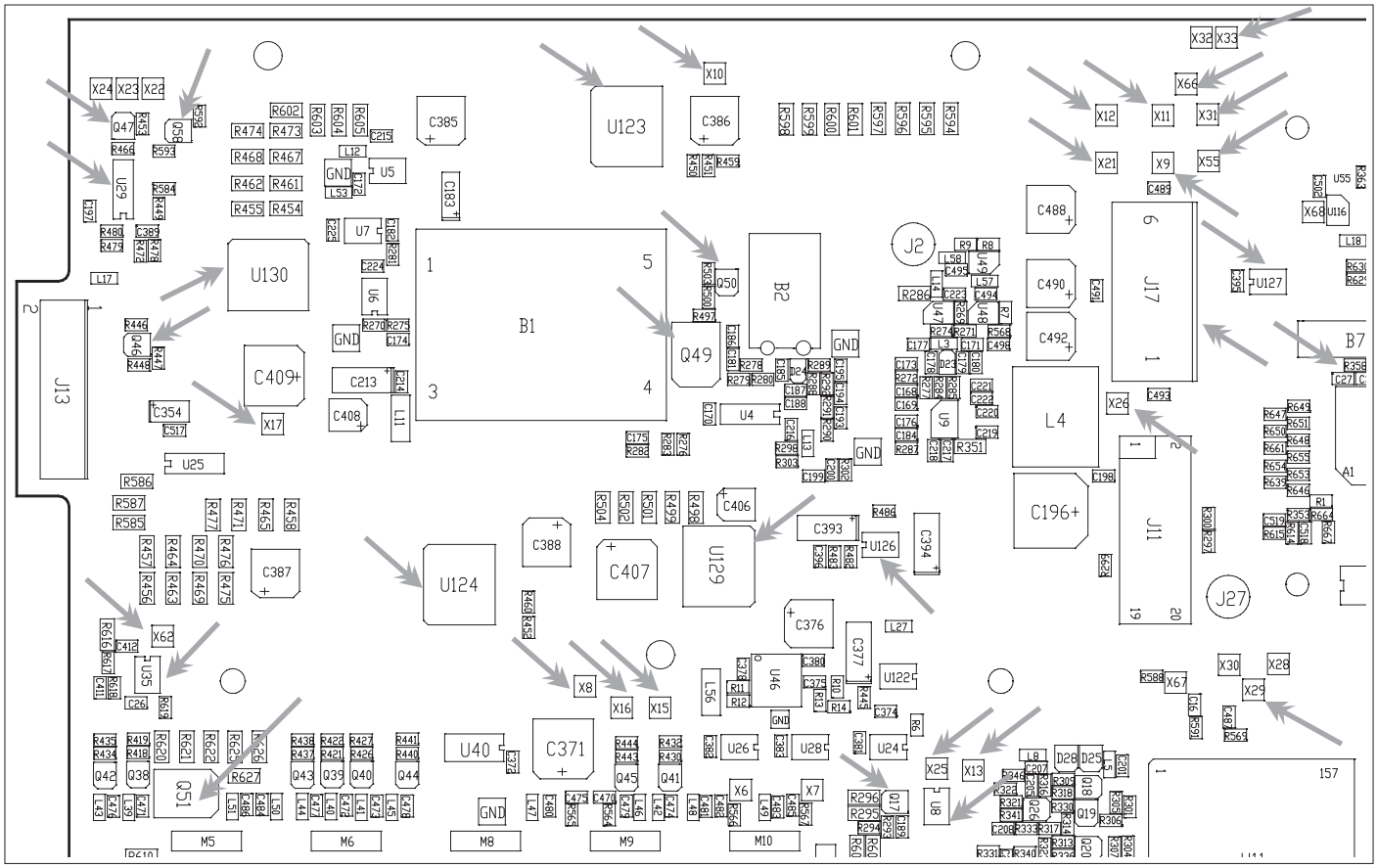

Figure 6-57 *Important power supply locations #1.*

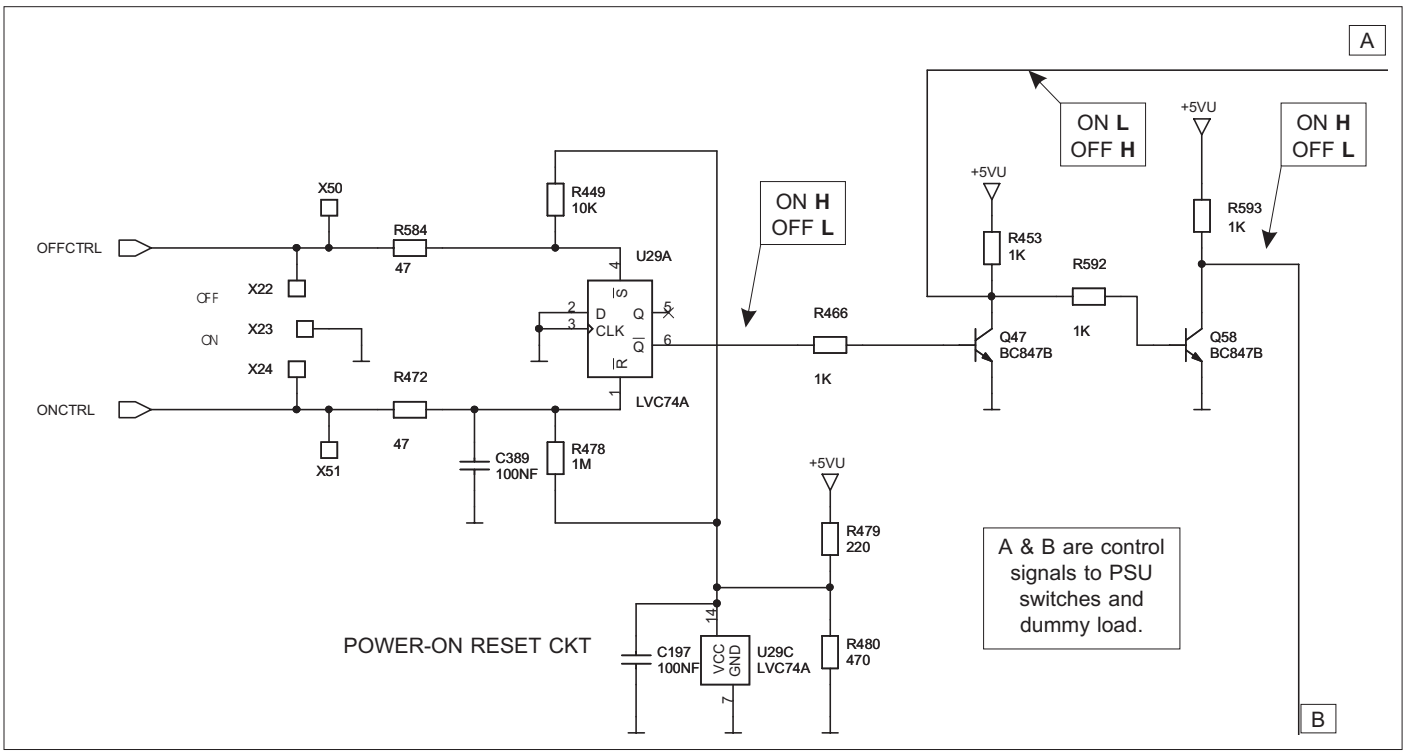

Figure 6-59 *ON/OFF logic*

Input Amplifiers

The input amplifiers for Channel A and Channel B are identical. A trigger level circuit belongs to each amplifier. The trigger level is adjusted to match the hardware during the voltage calibration procedure, see Chapter 7. Note that the input amplifiers must be adjusted according to Chapter 7 (step response, sensitivity etc). The description refers to both channels (Channel B information within parentheses).

Recall the timer/counter default setting. Select the measurement function *Time A-B*. Set both input channels to DC, Man Trig = 0.000 V. No signals connected.

The RF shield must be removed before measuring on the input amplifiers. It is soldered to two of the shield clips. Don't forget to put the shield back afterwards and secure it by resoldering.

First measure some DC values. U3 pin 9 (pin 13) should be near 0.000 V. The same applies to the trigger level, U3 pin 10 (pin 12). The voltage to ground at the point where R171 (R243) and R172 (R244) are connected should be approximately -0.8 V.

Connect a 1 kHz square wave with amplitude 1 V_{pp} in 1 MΩ to Input A (Input B). Measure at the following points (see also Figure 6-60) and use the ground pads that are distributed over the PC board:

Test Points	Approximate Voltage
R140 to R141 (R212 to R213)	1.00 V_{pp}
R156 to C109 (R229 to C140)	0.40 V_{pp}
U1 pin 2 (U2 pin 2)	0.20 V_{pp}
U1 pin 3 (U2 pin 3)	0.20 V_{pp}
U1 pin 6 (U2 pin 6)	-1.00 V_{dc}
R151 to R157 (R223 to R230)	0.40 V_{pp}
U3 pin 9 (U3 pin 13)	0.40 V_{pp}
R309 and R314 (R313 and R315)	ECL levels -1.0 V and -1.7 V
R301 both sides (R304 both sides)	LVPECL levels 1.6 V and 2.6 V

Test the trigger level by manually setting the following trigger levels. Check the voltage at X6 (X7) and U3 pin 10 (pin 12).

Set Level	Approximate Voltage
+1 V	+0.41 V
+4 V	+1.65 V
-4 V	-1.65 V
-1 V	-0.41 V

Set the timer/counter to default. Select the measuring function Single Period. Connect the 1 kHz square wave to channel A (B). Measure with oscilloscope at X6 (X7). See Figure 6-65 (Figure 6-66) for a typical signal.

If any repair work has been done on the input amplifiers, both adjustment and voltage calibration must be performed afterwards. If any repair work has been done on the trigger level circuits, at least voltage calibration must be performed afterwards. See Chapter 7.

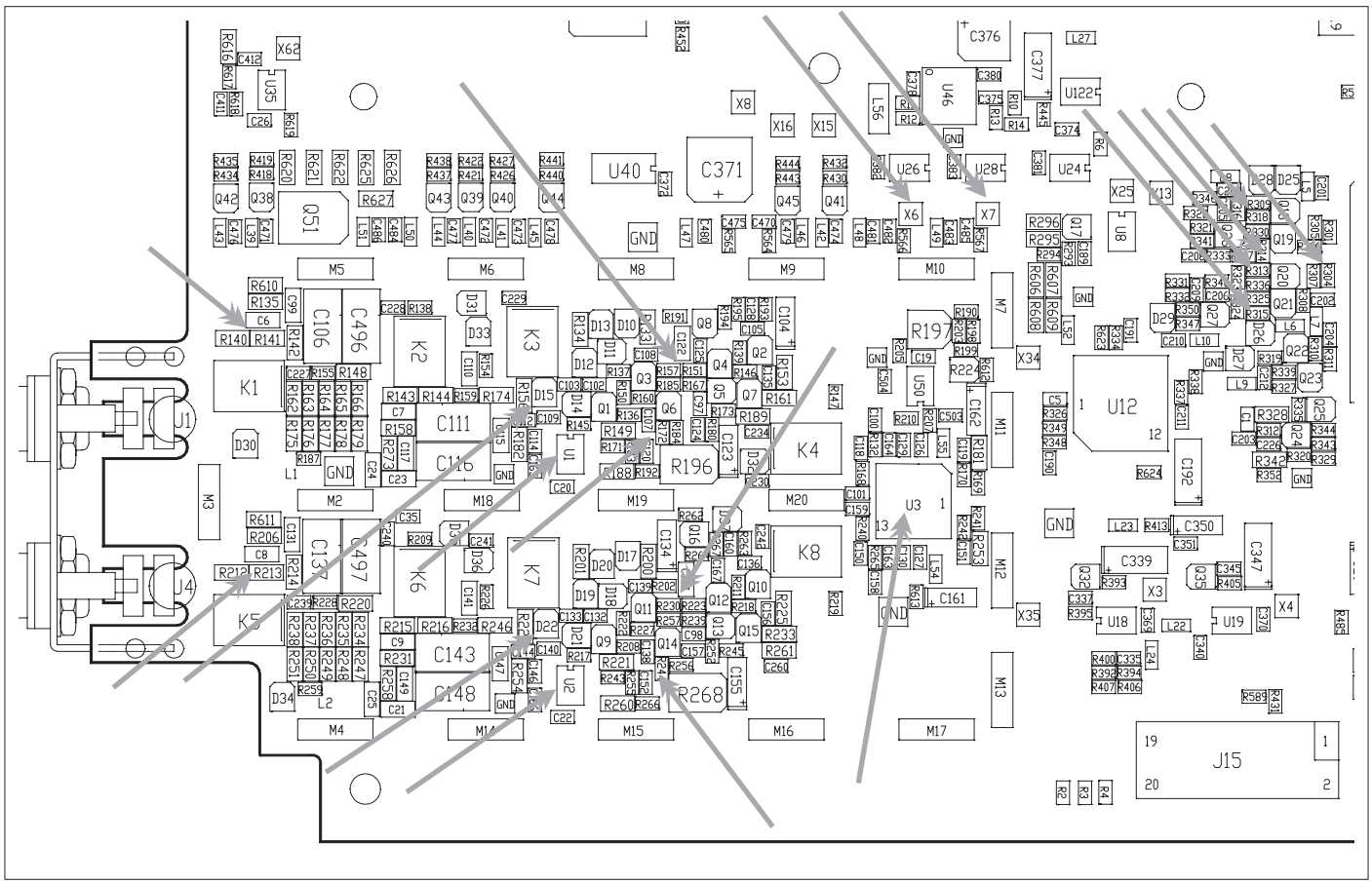

Figure 6-60 *Test points for troubleshooting the input amplifiers.*

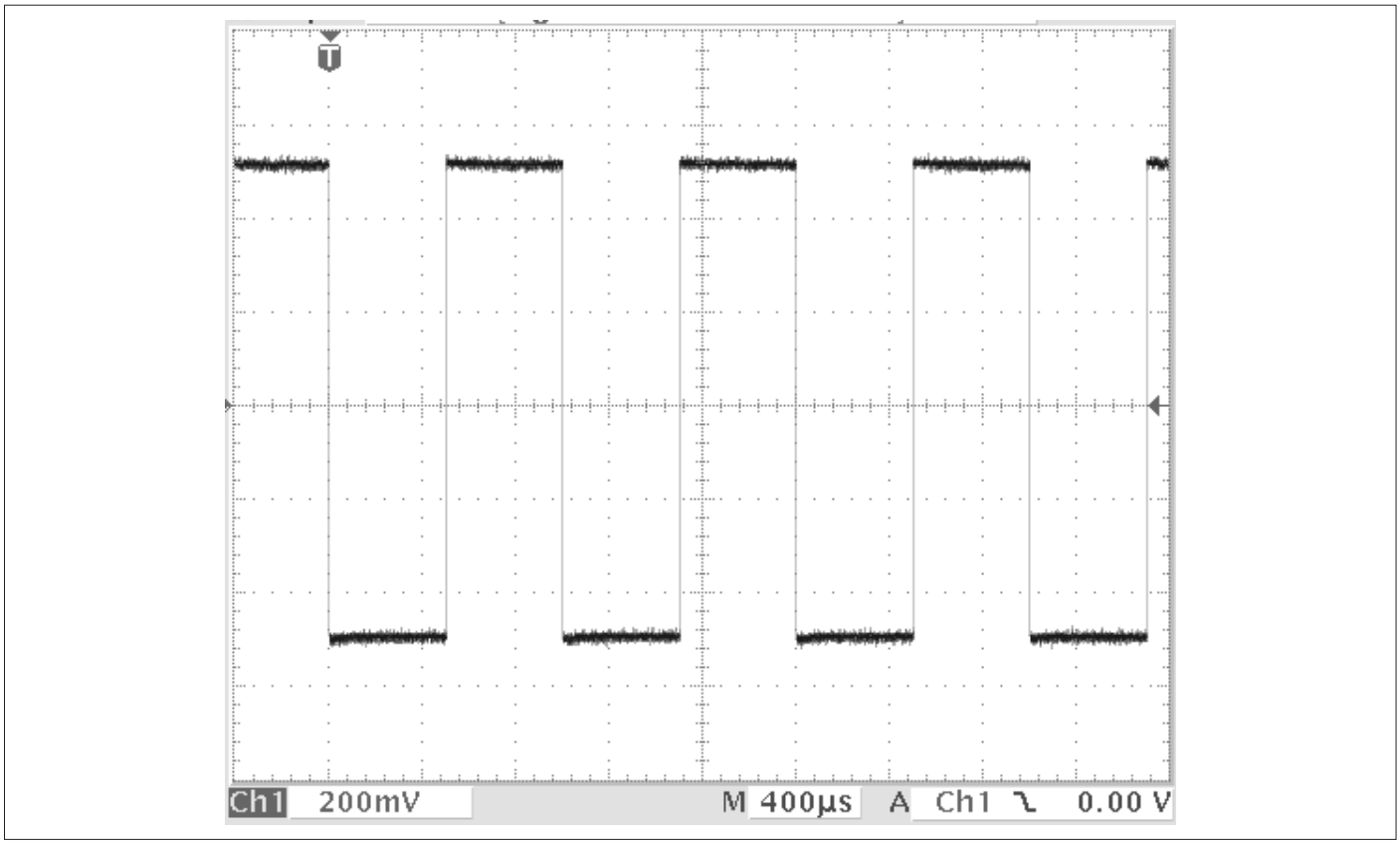

Figure 6-61 *Oscillogram showing the signal at the interconnection of R140 (R212) and R141 (R213).*

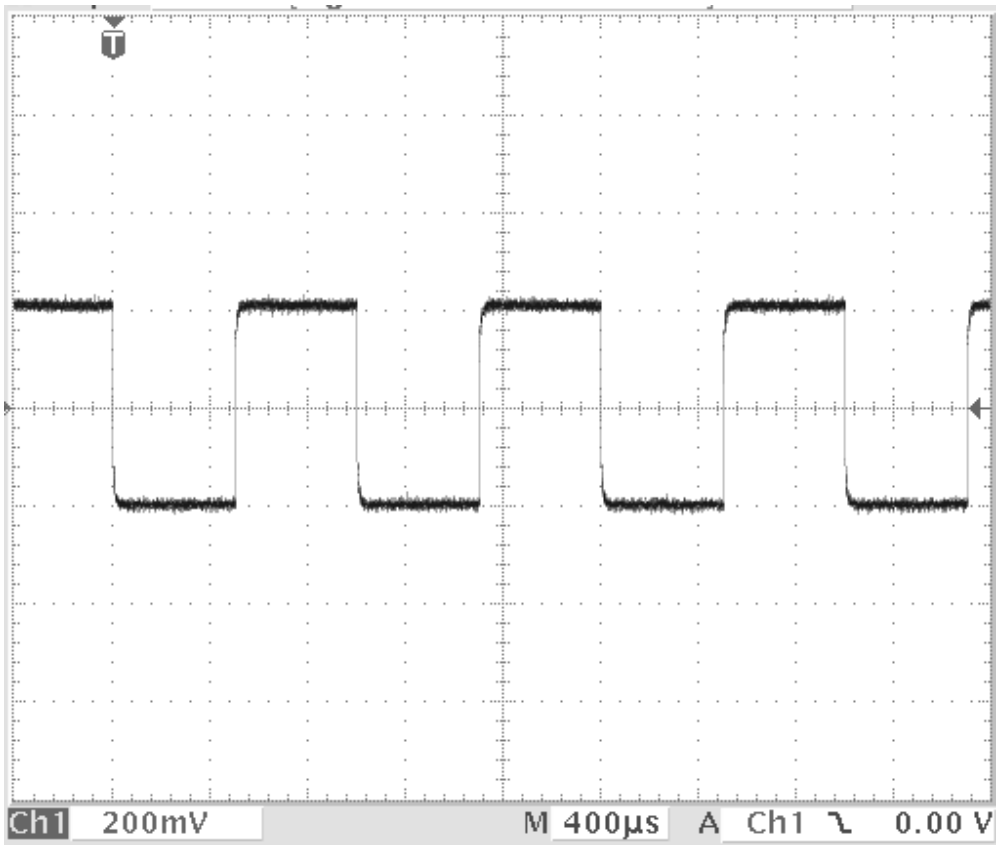

Figure 6-62 *Oscillogram showing the signal at the interconnection of R156 (R229) and C109 (C140).*

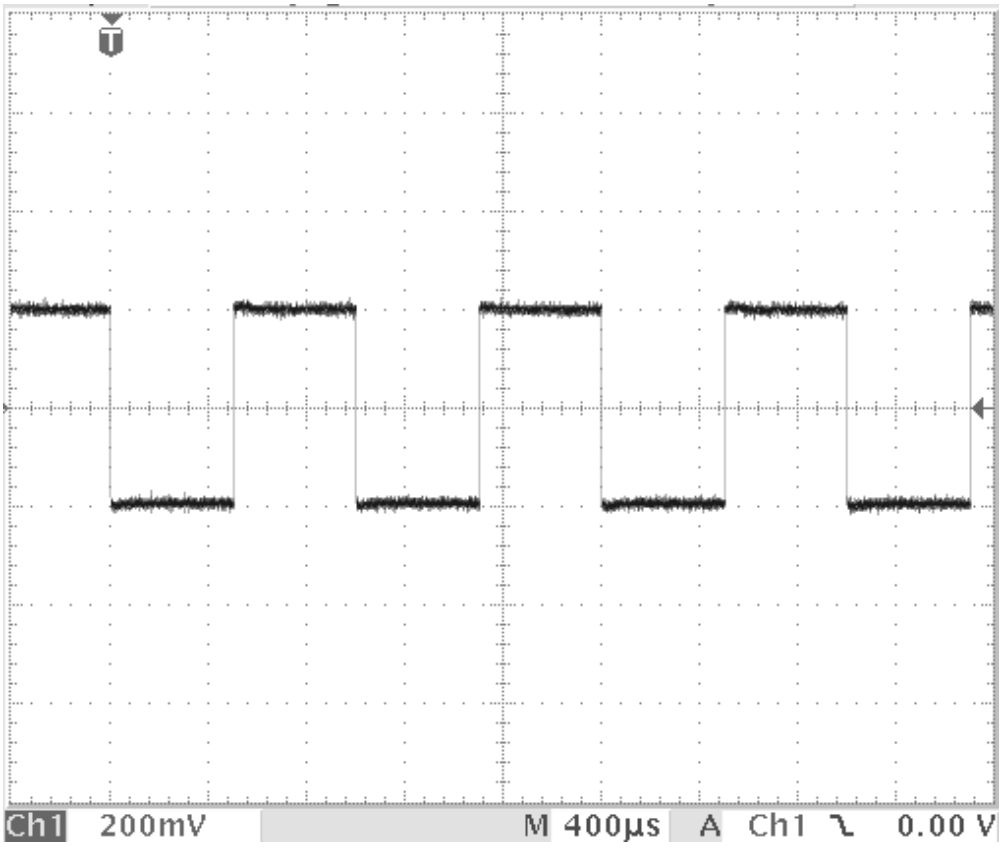

Figure 6-63 *Oscillogram showing the signal at U3:9 (U3:13).*

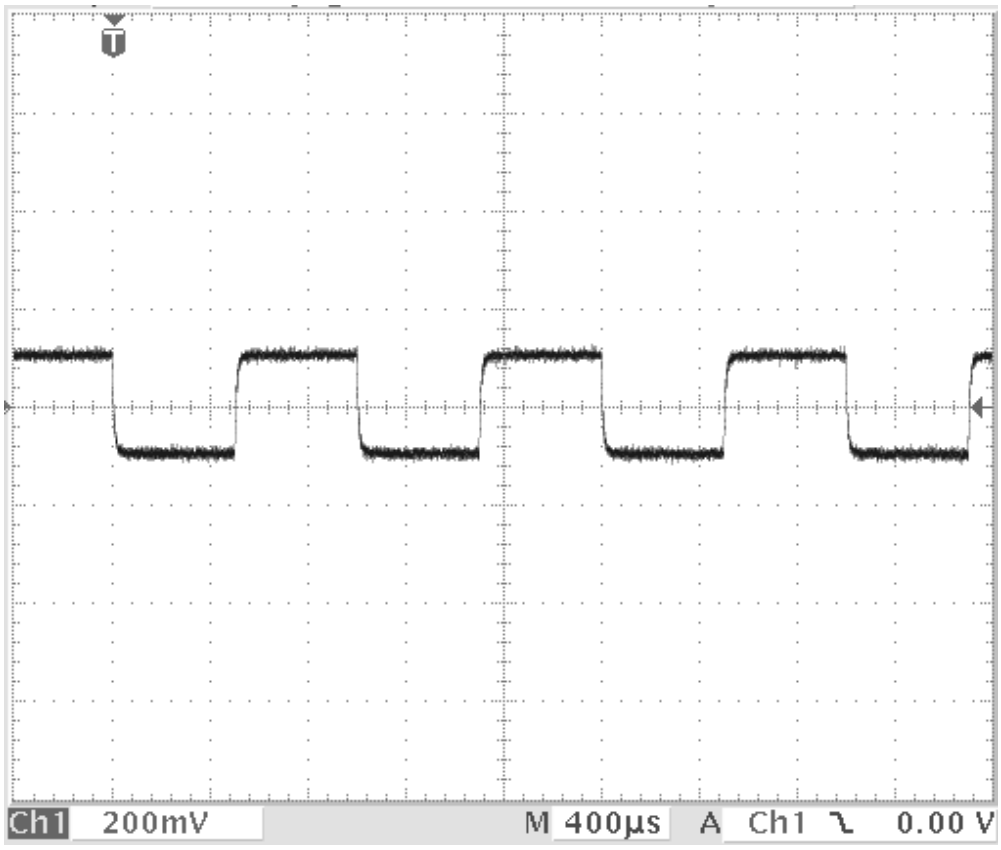

Figure 6-64 *Oscillogram showing the signal at U1:2 (U2:2).*

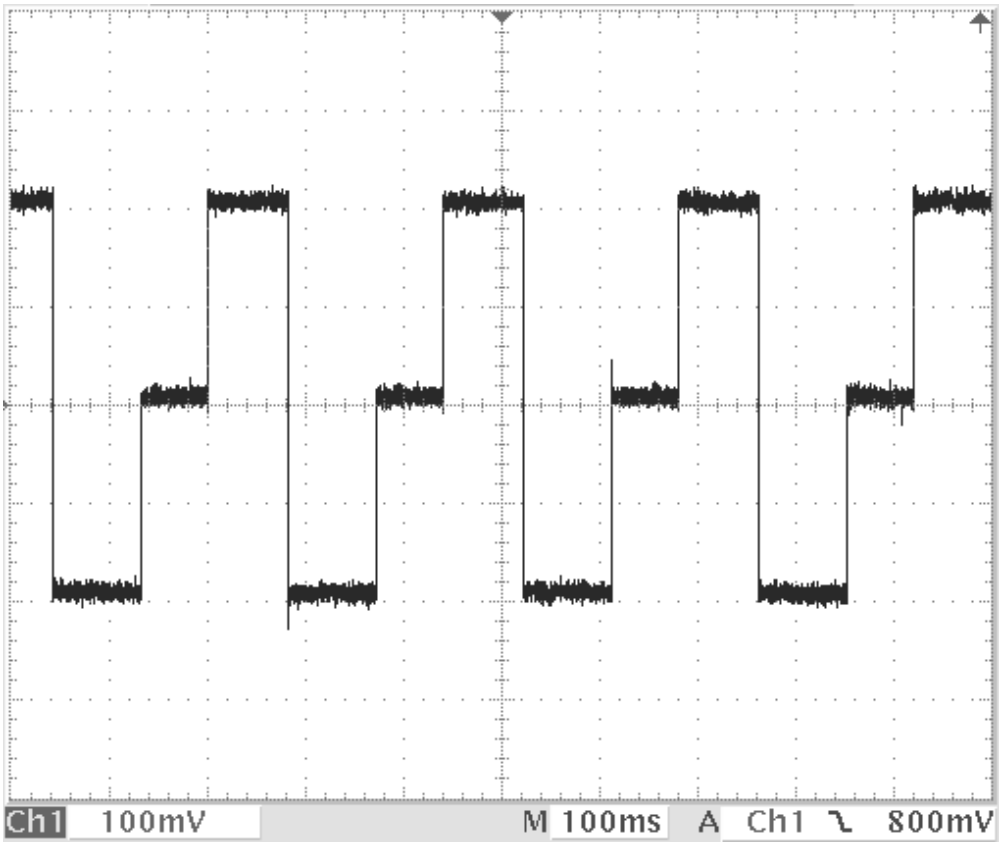

Figure 6-65 *Oscillogram showing the signal at X6, Period Single A.*

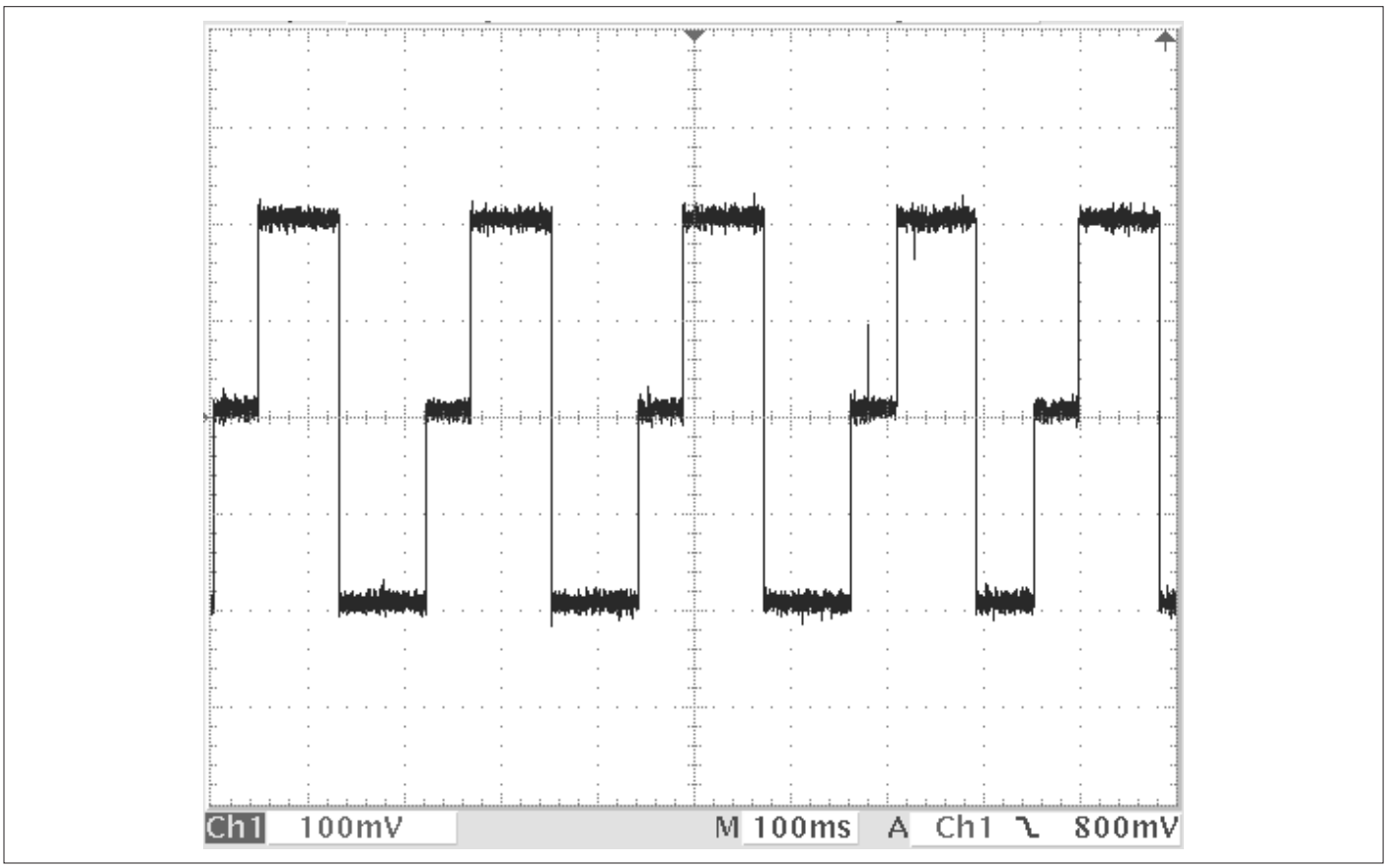

Figure 6-66 *Oscillogram showing the signal at X7, Period Single B.*

Timebase Reference Circuits

The measurement reference is either a 10 MHz signal from an internal oven-controlled crystal oscillator on the main circuit board or a signal from the external reference input that accepts the following frequencies: 1, 5 and 10 MHz. A frequency multiplier transforms the external signal to 10 MHz. The selected 10 MHz reference is always available at the internal reference output. See Figure 6-67.

The main PCB is prepared for both types of internal timebase, but only one of them is mounted. The selection is made at the factory. You have to run the utility program if the oscillator is to be changed. *Closed Case Calibration* is used to adjust the oscillator. On power-up the processor outputs the setting that is stored as the correct one for 10.000000 MHz. It will take some time for the oven oscillator to reach the correct frequency. A calibration must be performed if the adjusting voltage should move during operation, not only on power-up.

The selection between the on board oscillator and the external reference is made in the FPGA. The 10 MHz signal from the other source is switched off.

Connect a 10 MHz signal to the external reference input. Use the **SETTINGS** menu to alternate between internal and external oscillator. Check for correct signals at U4:6 for the standard oscillator, at U4:8 for the oven oscillator and at U33:3 for the external reference. Check also that the selected timebase reference is present at the internal reference output BNC connector on the rear panel.

Oven Oscillator

See Figure 6-68 and Figure 6-69.

The oven oscillator is a self-contained unit, enclosed in a metal box and soldered to the main circuit board. It cannot be repaired and must be replaced with a new oscillator if it is faulty.

Let the oven oscillator warm up 10 minutes before starting measurements. The 12 V supply voltage can be checked at X17. The oven oscillator should be powered also in standby mode.

The oven oscillator outputs a 10 MHz signal if powered. It should be 1.3 V_{pp} measured at R282. If not selected, a gate (U4) stops the signal, the control signal (U4:9) is then low. The frequency is controlled by a DAC (U5). Its reference voltage is derived from the oscillator, approximately +5 V (C174). The polarity of the reference voltage is reversed in an op amp (U6), and the voltage at U5:1 should be -5 V. The output voltage from the DAC should be between 0 and V_{ref}, measured at R281. The DAC is controlled by the processor via the SPI bus.

The frequency adjustment range should be wide enough to allow for more than 10 years of oscillator aging. The oscillator

must be replaced if the normal control voltage range cannot make the oscillator output 10.000000 MHz.

As a last resort to exclude external causes of malfunction, desolder the oven oscillator from the main circuit board. Place it upside down and connect +12 V and ground according to Figure 6-68. A cold oven oscillator draws approximately 0.30 - 0.35 A. During heating the current consumption varies. After 10 minutes it should stabilize on less than 0.1 A. The output V_{ref} should be approximately +5 V and the 10 MHz sinewave output signal should have an amplitude of more than 2.5 V_{pp} measured with a 1 MΩ, 10x probe. The control input has an internal bias to keep the output frequency in the middle of the range. Adjust the control voltage between 0 V and +5 V and check the output frequency range with a frequency counter. The minimum trimming range should be ±5 Hz. 10.000000 MHz must be reached somewhere between 0 V and +5 V.

If the oven oscillator circuitry is repaired, a new calibration must be performed. See Chapter 7. A new factory calibration by means of the utility program should also be performed.

External Reference Input

See Figure 6-67 and Figure 6-70.

The input signal is amplified in U31. The output signal from the amplifier should be a square wave with logic levels, reproducing the timing characteristics of the input signal. Check the signal at U32:11. U32 generates a short pulse (approximately 40 ns) for each input cycle, check at U32:9. These pulses generate a broad spectrum of harmonics, and the following high-Q 10 MHz crystal filter allows only a 10 MHz sinewave to pass. Measure at X19. Note that the trimmer C442 is used for maximizing the amplitude at X19. Check that the amplitude is not less than 1 V_{pp}. If external reference is not selected, the gate U33 stops the 10 MHz signal. The control signal on U33:1 is then low.

100 MHz Multiplier

See Figure 6-67 and Figure 6-69.

100 MHz is used in the measuring logic, mainly as a reference clock, but also for other purposes. A PLL is used for multiplying the 10 MHz reference to 100 MHz. On power-up the processor sets up the PLL IC (U9) via the SPI bus. An output signal, PLL LOCK, tells the processor if the loop is locked (high level). A VCO, consisting of an inverter (U47) and an LC circuit in the feedback loop, is controlled by the PLL IC. The DC voltage from U9:2 is filtered and controls a capacitance diode. The VCO frequency changes with the capacitance. The loop can handle the switching of 10 MHz reference, from internal to external and vice versa. There is no need for a new setup. If external reference is selected and no such signal is connected to the instrument, the PLL will be un-

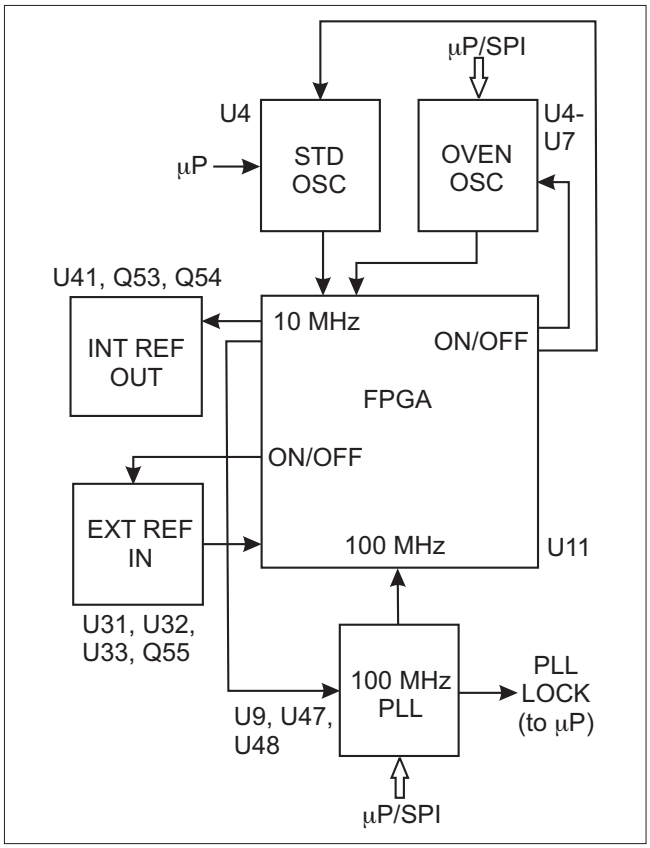

Figure 6-67 *Timebase reference system.*

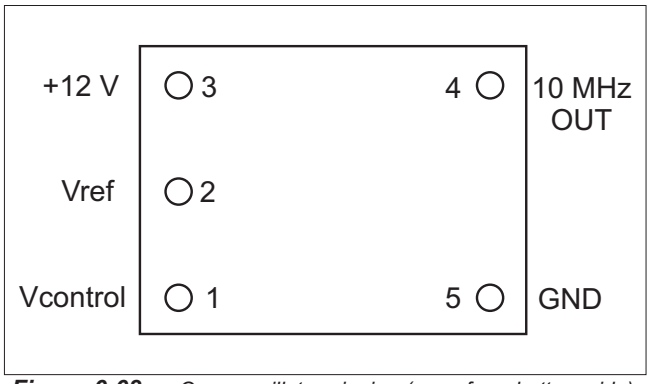

Figure 6-68 *Oven oscillator pinning (seen from bottom side).*

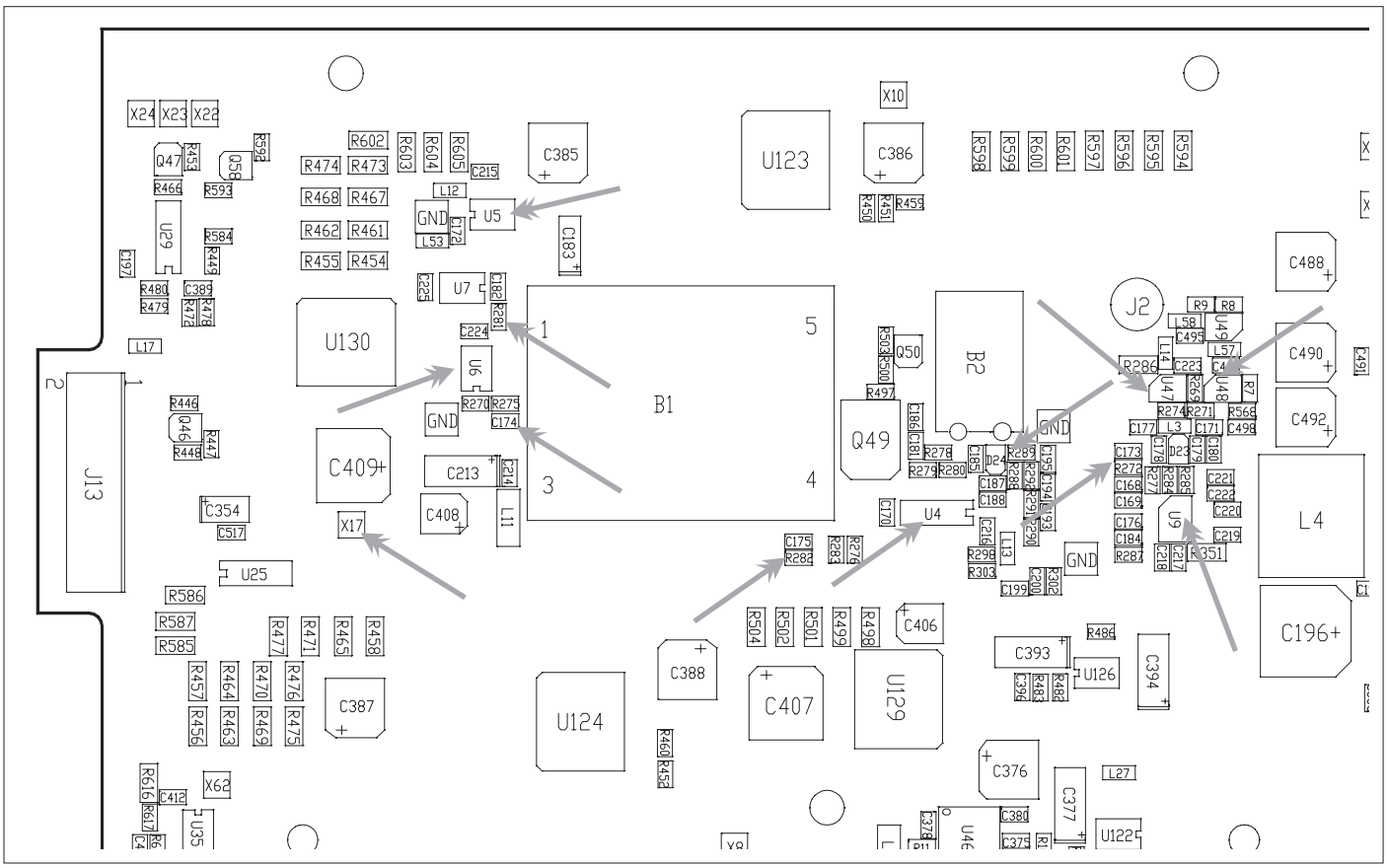

Figure 6-69 *Important locations in the internal timebase reference circuits.*

Figure 6-70 *Important locations in the external timebase reference circuits.*

locked, and the VCO will go to one of the extremes. The typical range of the VCO is 95 to 105 MHz, thus giving an error of typically 5 % in the measuring results.

Check the loop voltage (DC) at R272. It should be 1.6 - 2.2 V. Check the 100 MHz signal at U48:4. It should be locked to the incoming 10 MHz at U9:8. Check the lock condition with a 2-channel oscilloscope. Trigger on the 10 MHz channel. Then the signal on the other channel shall be fixed, i.e. not moving along the time axis. Check the PLL LOCK signal at U9:14 (lock is high).

Prescaler

The optional prescalers are not to be repaired. The faulty unit should be sent to the factory, and an exchange unit will be returned.

The best way to isolate the fault is to use another, functioning, timer/counter with the same prescaler. Interchange the prescalers and see if the problem follows the prescaler or the timer/counter.

First measure with Channels A and B and check that the result is OK. Select the function *Frequency C*. Connect a signal according to Table 6-2 to Input C. Check the following pins on the prescaler connector J15 on the main circuit board.

Pin 1 +5 V supply
Pin 5 +12 V supply
Pin 7 ON/OFF, ON is 0 V
Pin 11 test signal, should be 0 V
Pin 12 code 0, see Table 6-2
Pin 14 code 1, see Table 6-2
Pin 16 code 2, see Table 6-2
Pin 4 prescaler output signal, PECL levels (+4.1 V and +3.4 V)

	PRESCALER 2.7 GHz
Frequency (GHz)	1
Level (dBm)	0
Division Factor	16
Code 0	0
Code 1	1
Code 2	0

Table 6-4 *Prescaler characteristics.*

Measure with oscilloscope and probe at pin 4. The output frequency should be the input frequency divided by the factor in the table. Check with a frequency counter.

Note: The 2.7 GHz option has a sensitivity trimmer. See page 7-14 for information on how to adjust it.

Microprocessor & Memories

Startup Process

The processor in this instrument is a Sharp LH79524 with a 32-bit ARM720T core. It is housed in an IC (U13) together with peripheral units like SRAM, timers, I^2C bus interface, SPI bus interface and LCD controller.

The 32-bit microprocessor bus is connected to one 16-bit Flash PROM (U17) and two 16-bit SDRAMs (U15 & U16). The two SDRAMs are organized as one 32-bit wide memory. The microprocessor bus is also, via bidirectional buffers, connected to an FPGA, a USB IC and a GPIB IC.

A reset IC (U116) monitors +3.3 VD and +1.8 V. The reset signal is active low and is kept low for approximately 160 to 180 ms after the voltages have settled and been approved. Measure at X33. The ramp-up time for +3.3 VD is approximately 3 ms.

The processor has an internal linear regulator that generates the core voltage (+1.8 V) from the +3.3 VD I/O voltage. Check +1.8 V at X66.

The rising edge of the reset signal marks the start of the boot sequence. All I/Os on the processor are set to inputs. The 11.2896 MHz oscillator will start running (check at R358). An internal PLL generates 1.88 MHz (reset value) as microprocessor clock (check at X29). The processor will start reading in the Flash PROM. The initializing of the processor and the peripherals will start.

The I/Os will be set up, the processor clock will be set to 50.8 MHz (check at X29). The SDRAMs will start, and the code is copied from the Flash PROM to the SDRAMs. From now on the code is executed from the SDRAMs. Then all the other subsystems are initialized: I^2C bus, LCD controller, SPI bus, fan etc. The FPGA is also programmed by the processor.

The progress of the initialization can be followed at two test points, X55 and X31.

Test Point	Reset	I/O Setup	SDRAM Execute	I^2C Init	Init Ready
X55	float. inp.	1	0	1	0
X31	float. inp.	1	1	0	0

See Figures 6-74 to 6-76 for a survey of a typical instrument startup.

The LCD is switched on. The LCD controller in the processor generates the control signals for the LCD. See Figures 6-77 to 6-81and 6-83. Note the different timing for the signals. The I^2C bus is used for switching the LCD on. The ON signal can be checked at R34 on the display board. It should be high. The LCD voltages must also be switched on. It is done by a control signal from the processor. Check the signal at R33 on the display board. It should be high. Negative pulses on this signal are used for adjusting the contrast of the LCD, i.e. the LCD

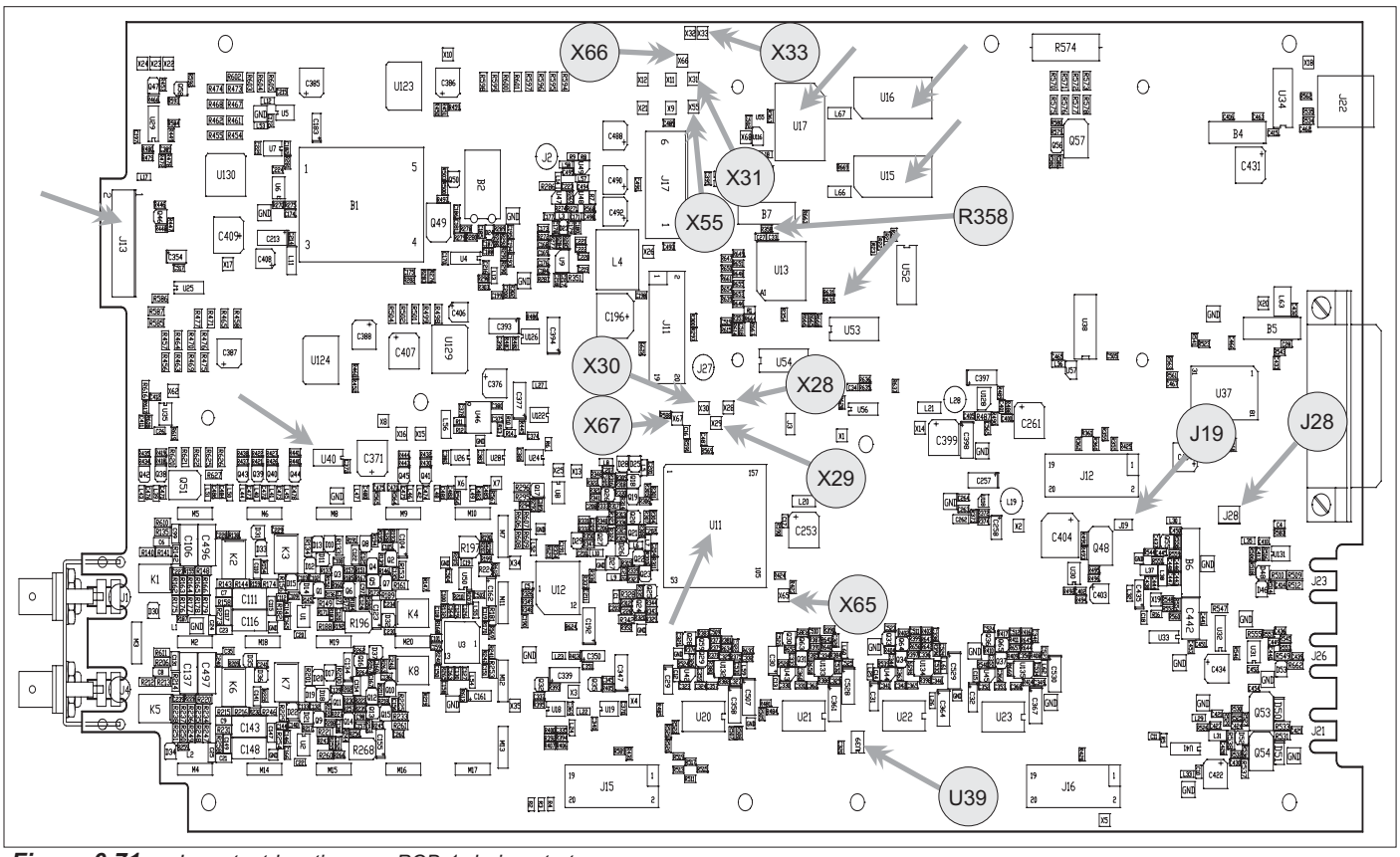

Figure 6-71 *Important locations on PCB 1 during startup.*

voltages. The range is 14.9 V to 17.5 V measured at X1 on the display board. Set the contrast so X1 is 16.2 V. Check the LCD voltages at X2 (14.7 V), X3 (13.3 V), X4 (2.9 V) and X5 (1.5 V). See Figure 6-72.

The FPGA (U11) is programmed by the processor. The used pins are PROGN, INITN, DONE (X65), Clock and Data. See Figure 6-75. The loading starts when PROGN is set low. Then the processor checks that INITN is low and sets PROGN high again. The FPGA responds by setting DONE low. After loading, which takes approximately 1.4 s, the FPGA sets DONE high (check X65), if the loading was successful. If an error is detected, INITN is set low. One clock pulse after DONE is set high, all I/Os on the FPGA are defined. If the loading of the FPGA is not successful, the program just goes on with the rest of the startup procedure. At test point X67 the FPGA will output approximately 14 Hz. This signal shows that the FPGA is working and will be switched off about 8 minutes after power-up.

The fan is set to 8.4 V. Measure on J19 or J28. The input amplifiers are initialized and a "click" from the relays is heard. The I^2C bus is used for controlling the relays.

Note: The I^2C bus is of the utmost importance for the start of the instrument. The keys, the LCD and the relays in the input amplifiers all need a faultless I^2C bus to work properly.

Note: If the Flash PROM is exchanged, it must be replaced by a preprogrammed Flash PROM. Voltage and timebase calibration must be performed anew. The utility program must be used for transferring the calibration results to new factory calibrations. The serial number and the oscillator option must also be programmed by the utility program.

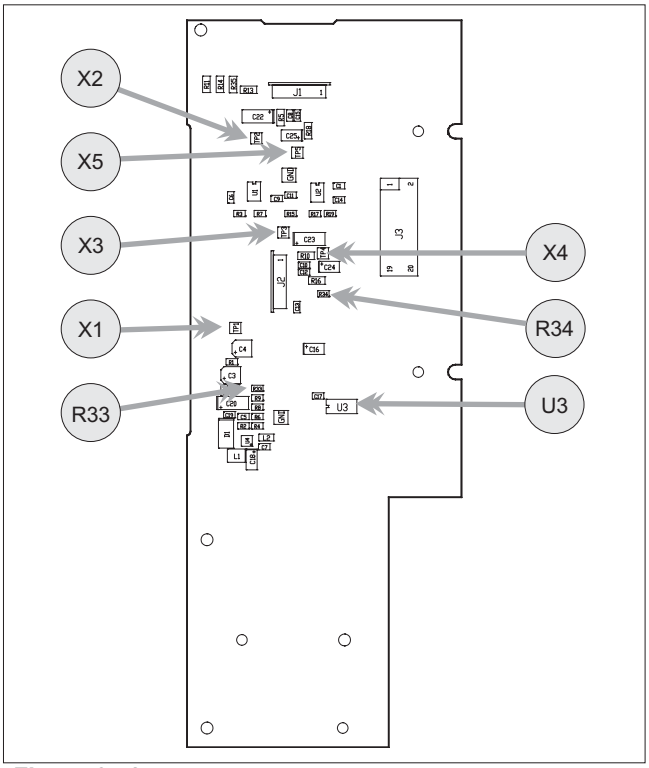

Figure 6-72 *Important locations on PCB 2 during startup.*

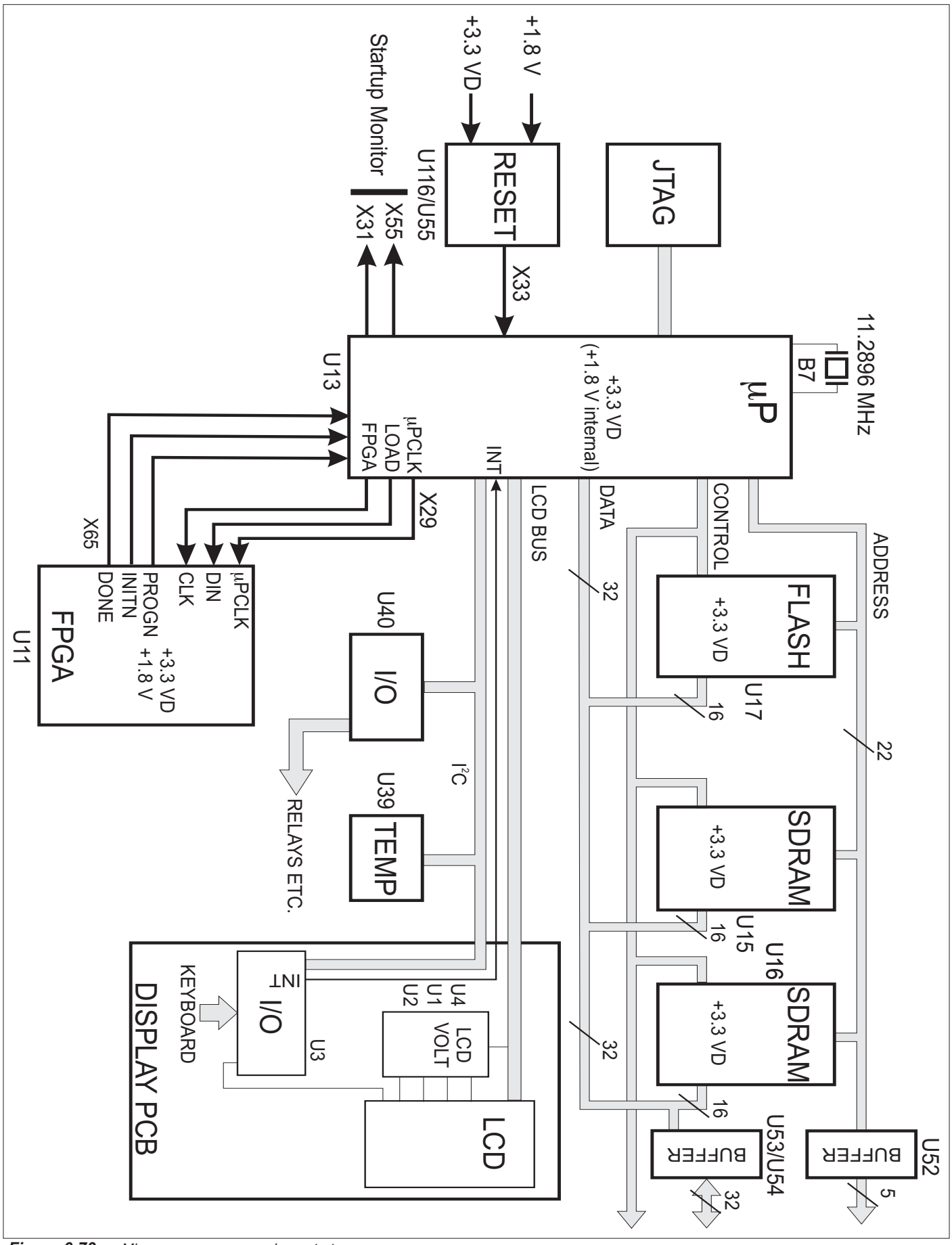

Figure 6-73 *Microprocessor, memories - startup.*

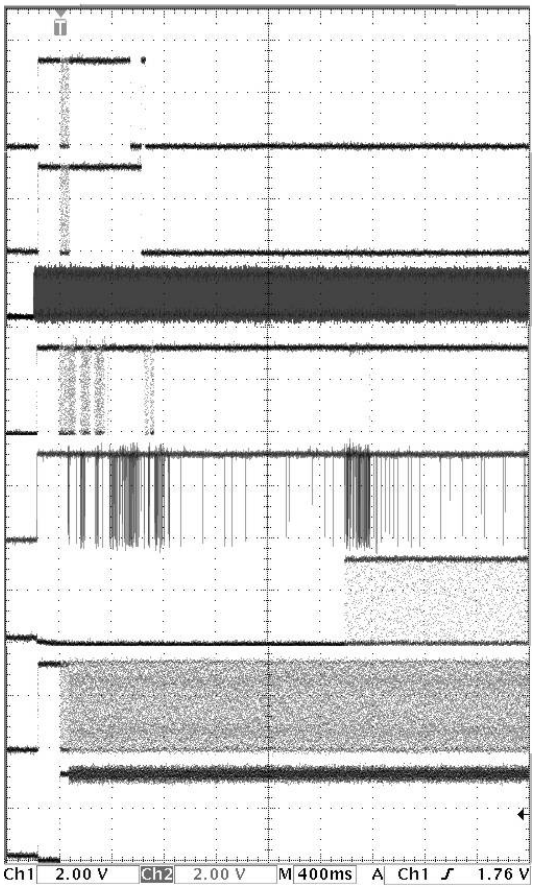

Figure 6-74 *Startup timing - processor, memories, fan.*

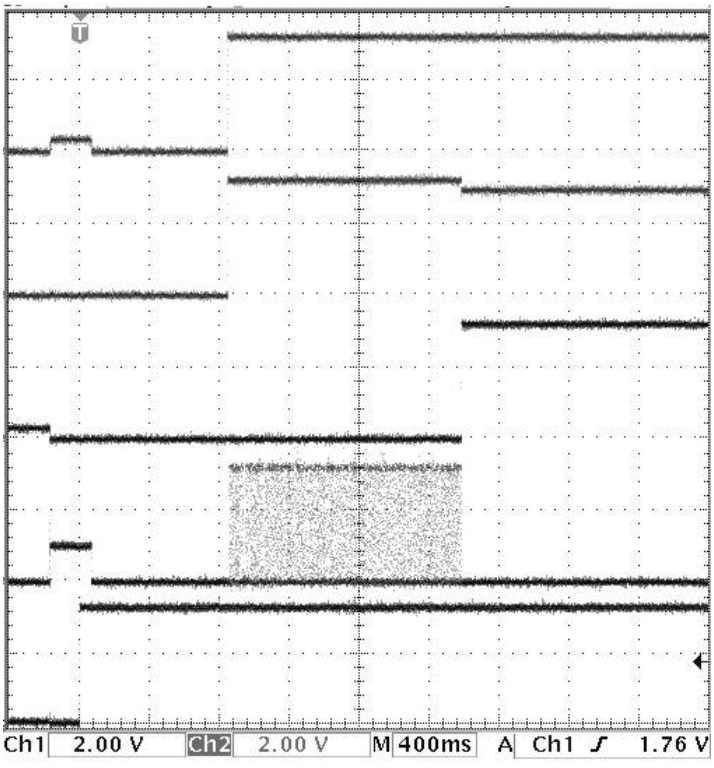

Figure 6-75 *FPGA loading.*

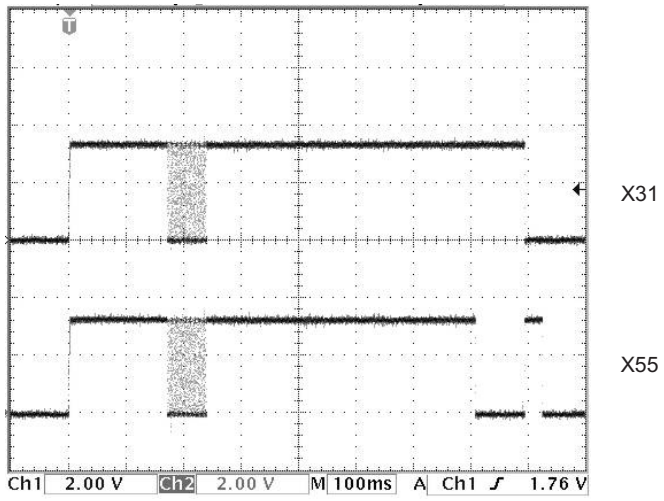

Figure 6-76 *Startup indicator test points.*

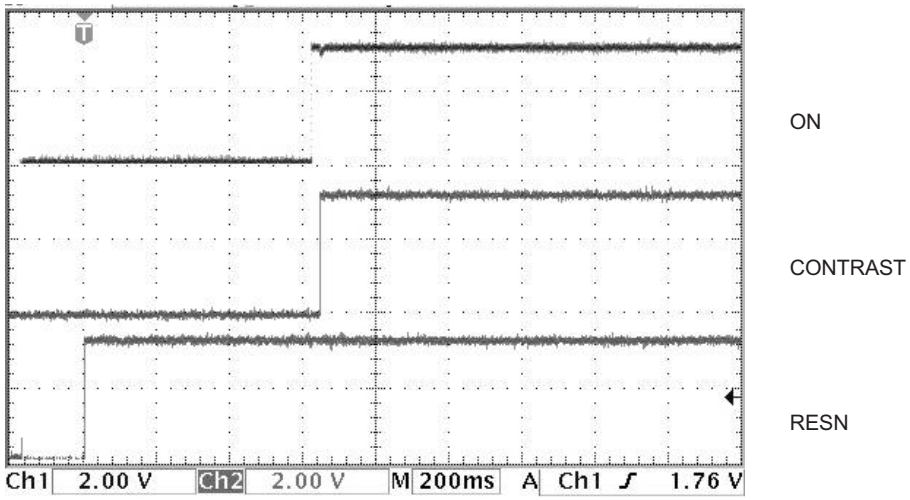

Figure 6-77 *LCD control signals, ocillogram #1.*

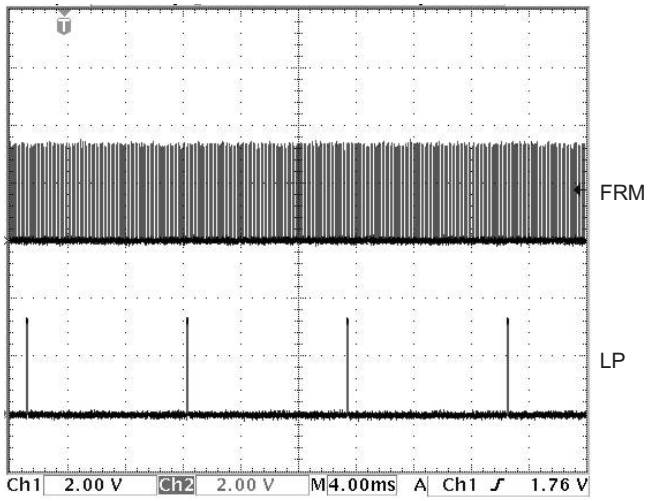

Figure 6-78 *LCD control signals, oscillogram #2.*

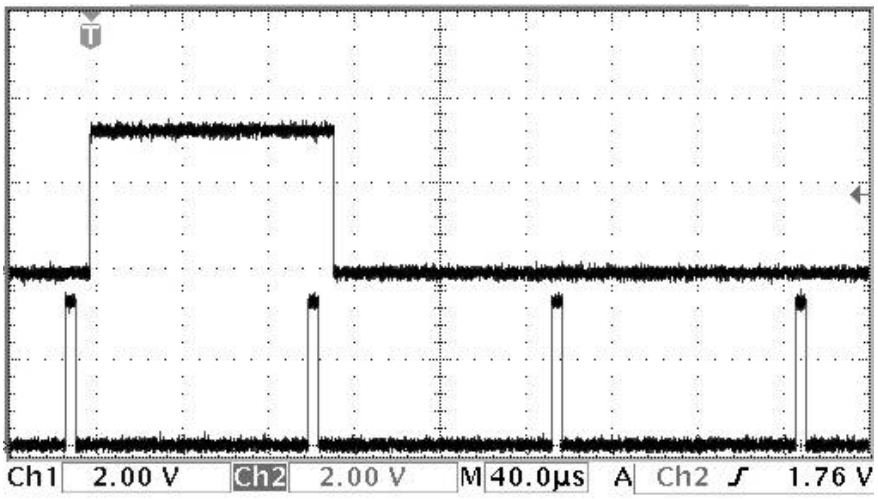

Figure 6-79 *LCD control signals, oscillogram #3.*

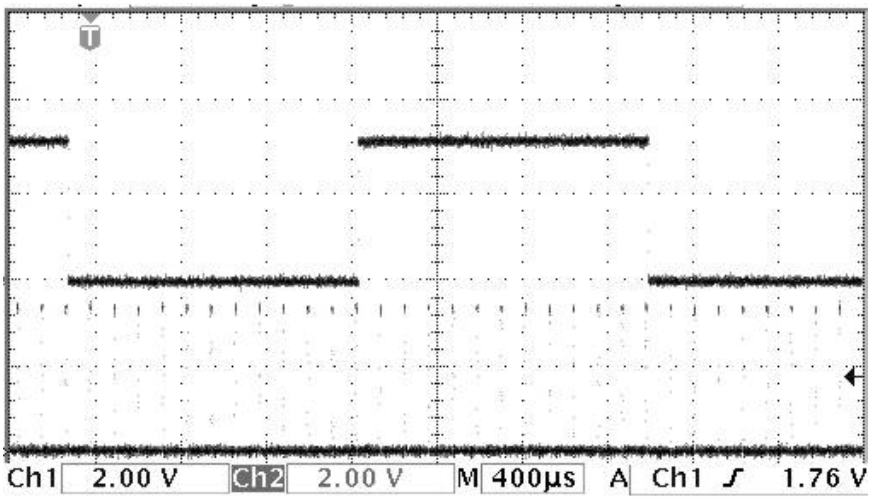

Figure 6-80 *LCD control signals, oscillogram #4.*

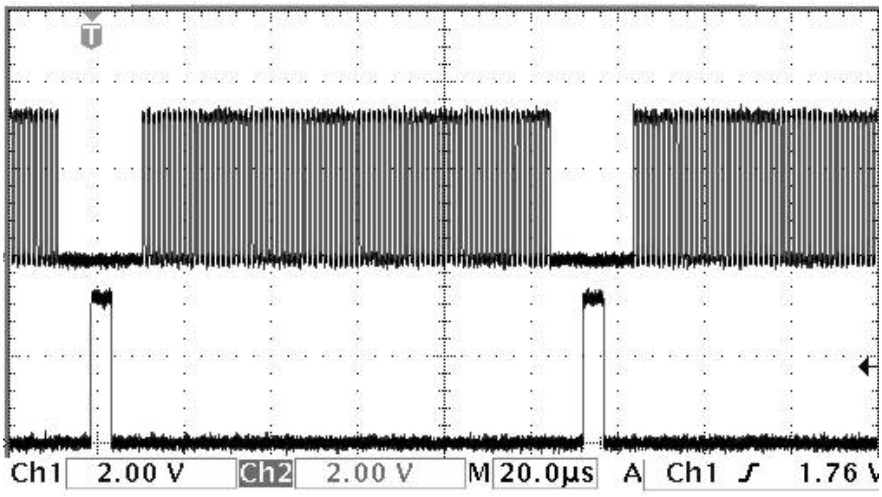

Figure 6-81 *LCD control signals, oscillogram #5.*

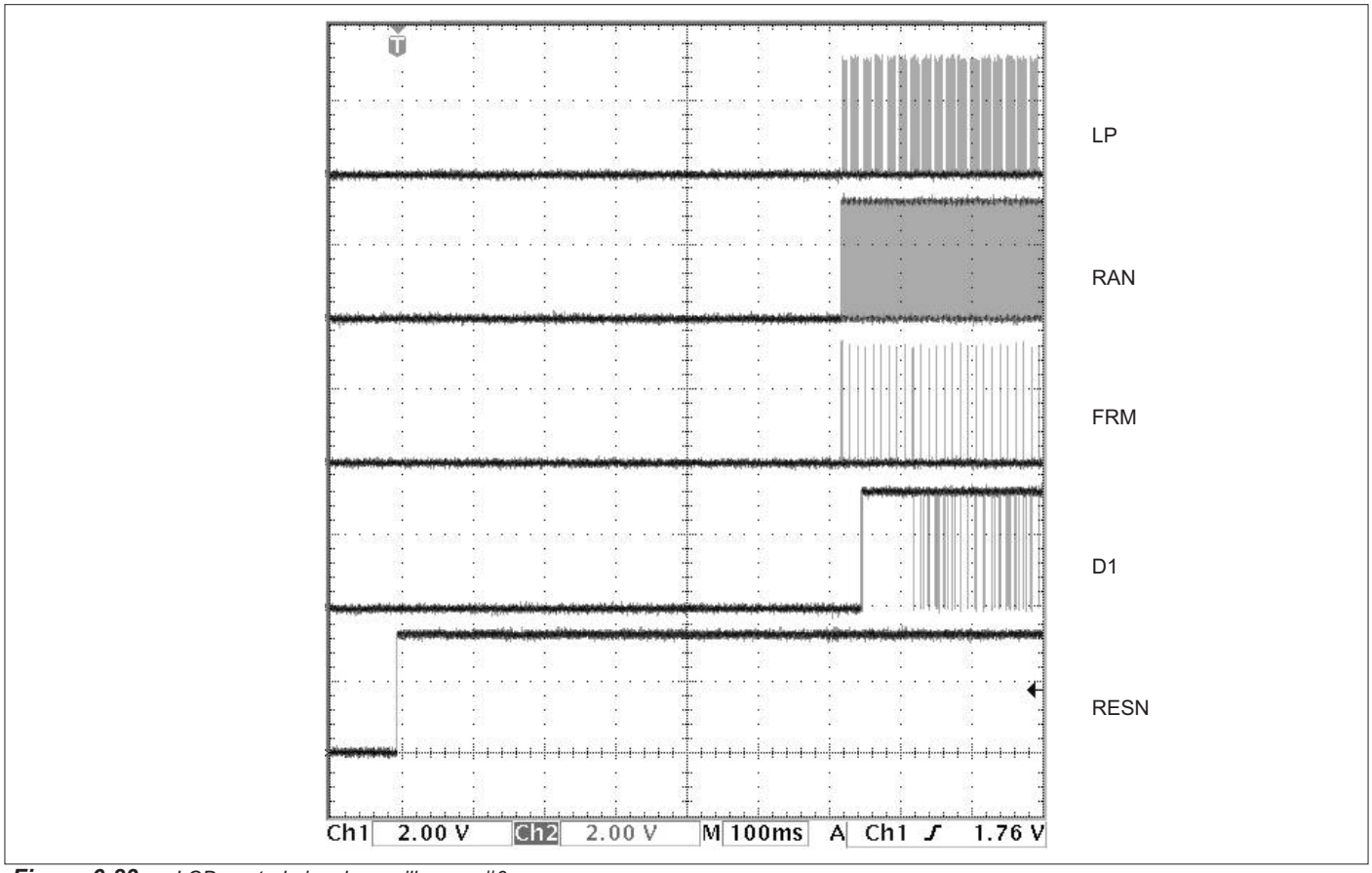

Figure 6-83 *LCD control signals, oscillogram #6.*

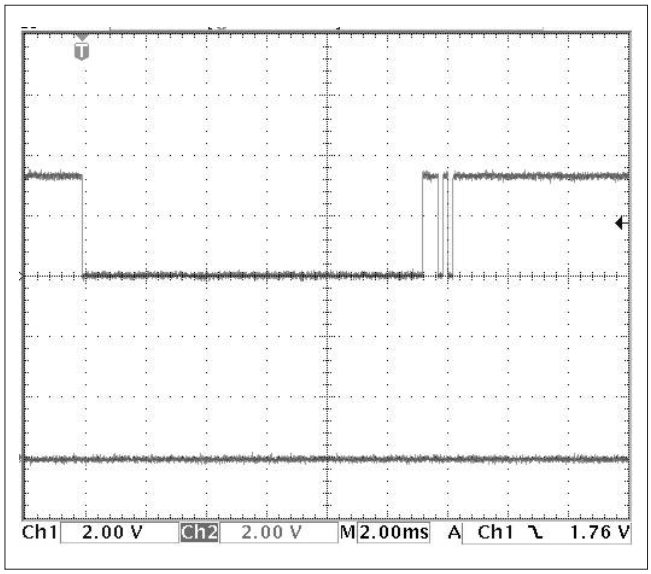

Figure 6-82 *Keyboard interrupt .*

The fan is kept at +8.4 V for the first 8.3 minutes. After that the fan is temperature controlled. The processor reads the temperature via the I^2C bus every 10th second. IC U39 measures the temperature.

The keys on the display board are read over the I^2C bus. If a key is pressed, the I^2C bus circuit U3 notices that and sends an interrupt to the processor. Check at J13:9; low is interrupt. The processor then scans the keys via the I^2C bus to find the depressed key. See Figure 6-82. During the scanning there may appear some extra interrupts. This is not an error condition.

Microprocessor Bus & Interfaces

The microprocessor bus is divided into two parts with buffers. The inner part consists of the Flash PROM and the SDRAMs. Buffers isolate the inner part from long lines in order to make the SDRAM work safely. The buffers of the 32-bit data bus are bidirectional and a control signal opens the buffers only during reads and writes (U56:8, low to open buffers). The direction of the buffers is controlled by the *rdn* from the processor.

The outer part consists of the 32-bit data bus and the 5-bit address bus. It connects the processor (U13) to the FPGA (U11), the GPIB and the USB. See Figure 6-87.

The FPGA connection has 32 data bits, 5 address bits, chip select, *wrn* and *rdn*. The FPGA is controlled by the processor via the bus; measurement functions are selected, for instance. The FPGA is controlled between each measurement or block of measurements. An interrupt signal from the FPGA is connected to the processor. See Figure 6-89 for a typical timing diagram.

The connection to the USB has 16 data bits, 1 address bit, chip select, wrn and rdn. An interrupt signal from the USB IC is connected to the processor. See Figure 6-90 for a typical timing diagram. The USB IC is a complete USB unit. It is not powered from the USB bus. The USB IC (U34) has a 6 MHz oscillator. Check at C416.

The connection to the GPIB has 8 data bits, 5 address bits, chip select, wrn, rdn and a special control signal for the level shifting IC (U38). U38 is a buffer between the logic level of +3.3 V for the processor and the logic level of +5 V for the GPIB IC (U37). An interrupt signal from the GPIB IC is connected to the processor. See Figure 6-91 for a typical timing diagram. The GPIB IC is a complete GPIB unit. The GPIB IC (U37) has a 40 MHz oscillator. Check at TP20.

Only the selected interface is involved in communication on the microprocessor bus.

Since both interfaces consist of only one IC each, troubleshooting is fairly simple. Check that the oscillator (40 MHz or 6 MHz) is running. Check that the processor communicates with the selected IC. Make sure the external controller (GPIB or USB) and the interconnection cable used are OK.

The transfer of measurement results from the FPGA to the microprocessor goes via the 32-bit microprocessor bus and normal *reads*. There are some extra handshake pins to facilitate the transfer. An interrupt signal is sent to the microprocessor if results are to be read, ALERT, X30. X28 (EMPTY) indicates that it is allowed to read results, and the microprocessor sets a signal high to indicate that it is reading results, UPRD, U11:203. Results are always read in packets of 8 words. See Figure 6-92 for a typical timing diagram.

Another bus from the microprocessor is the SPI bus. It is a serial bus with one data signal and one clock signal that are common to all ICs connected to the bus. A separate load signal for each IC controls the loading of the data. Connected to the SPI bus are (See Figure 6-93 to Figure 6-96):

- The 100 MHz PLL IC (U9). The SPI bus is used only for initialization after power on.
- The optional oven oscillator IC (U5). The SPI bus is used for initialization after power on and during a timebase calibration.
- The trigger levels IC (U46).

The last bus is the I^2C bus. It is also a serial bus with two signals, SDA and SCL. Each connected IC has a unique address. The message sent includes the address, and only the addressed IC will listen to the message and respond by sending an acknowledge to the master. Then it will react accordingly.

Introduction to the I^2C Bus

The I^2C bus is a 2-line serial bus for the communication between the ICs. The microprocessor controls the communication by means of the clock line SCL. One or more slaves can read or write on the data line SDA.

The SDA and SCL are high at standby. All ICs connected to the bus can sink SDA to low as they are interconnected via open collector outputs. The microprocessor starts and stops the communication by sending terms of start and stop:

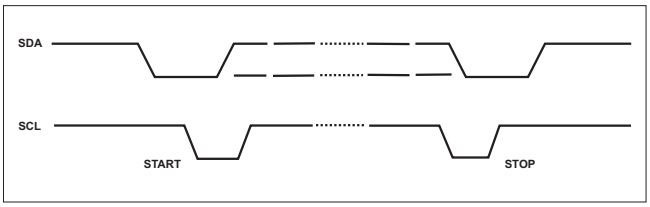

Figure 6-84 *Terms of start and stop.*

During transmission the SDA can be changed only when the SCL is low.

The microprocessor always begins to send the address information. The format of this address information is seven address bits, one read/write bit, and one acknowledge bit.

The addressed slave accepts by keeping the SDA line low while the acknowledge bit (ACKN in) is sent by the microprocessor.

Example of addressing (address 30H):

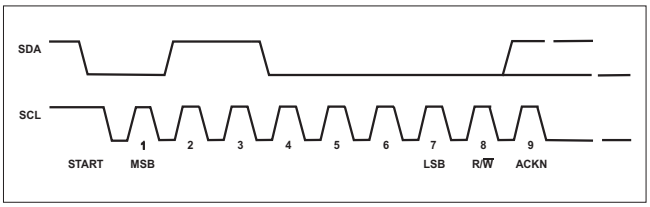

Figure 6-85 *Addressing.*

The read/write bit R/$\overline{W}$ has the following meaning:

R/$\overline{W}$ = 1 means information from the slave to the µprocessor
R/$\overline{W}$ = 0 means information from the µprocessor to the slave.

The data information is sent after the address information. The format of the data information is eight data bits followed by one acknowledge bit. The reciever accepts by keeping the SDA line low while the acknowledge bit (ACKN in) is sent.

Example of data transmission (data 9BH):

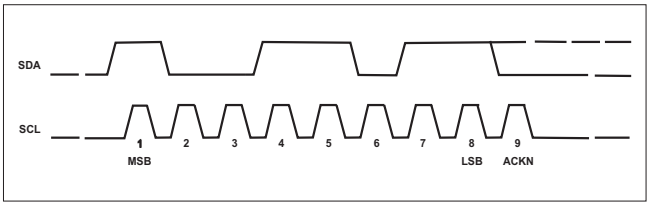

Figure 6-86 *Data transmission.*

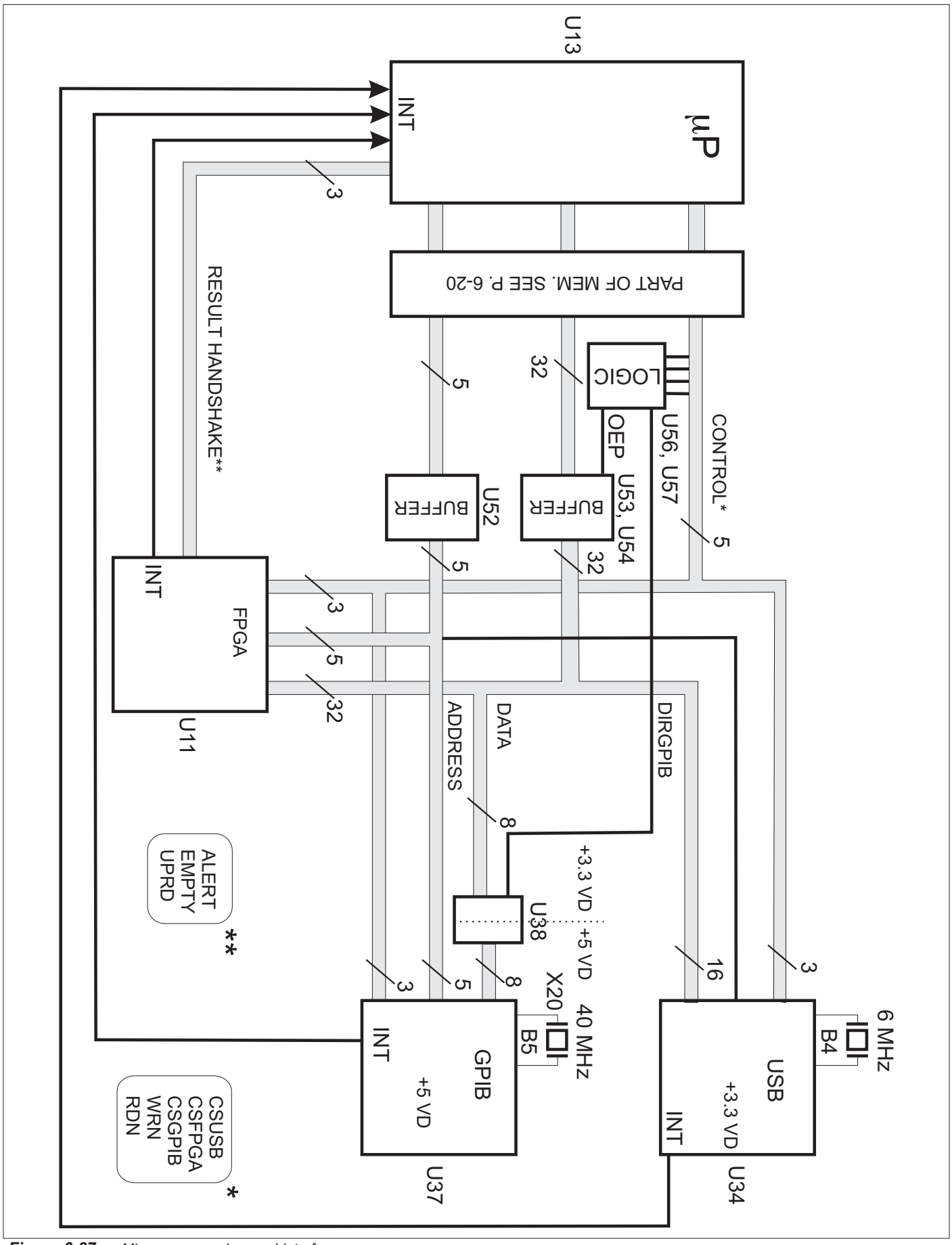

Figure 6-87 *Microprocessor bus and interfaces.*

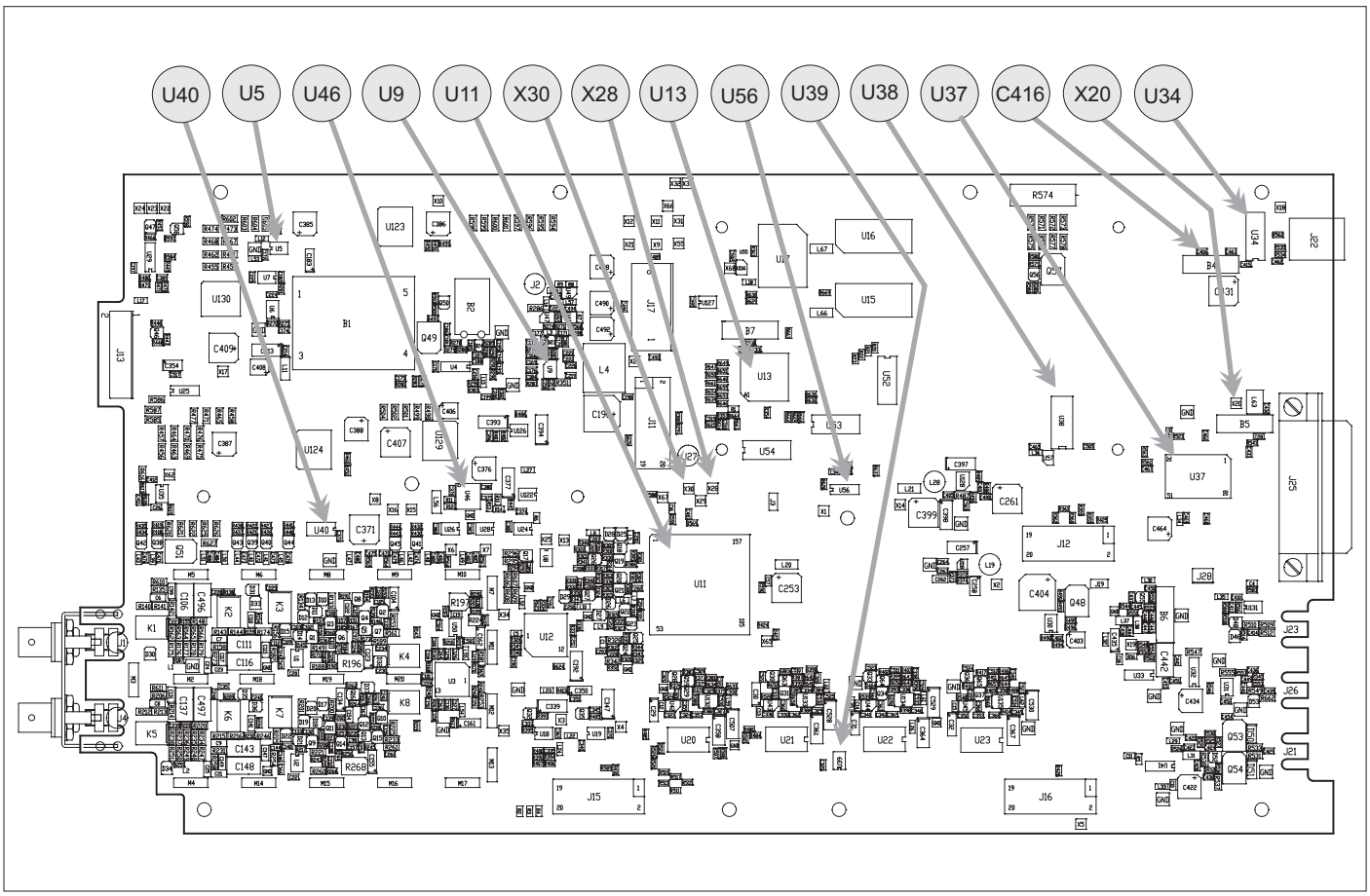

Figure 6-88 *Important locations for the microprocessor and its buses and interfaces.*

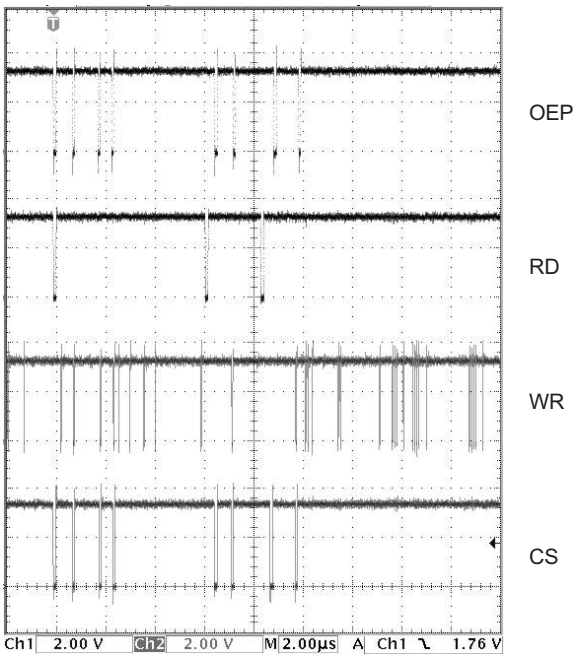

Figure 6-89 *Microprocessor bus - FPGA timing - Single Period - Hold, after Restart.*

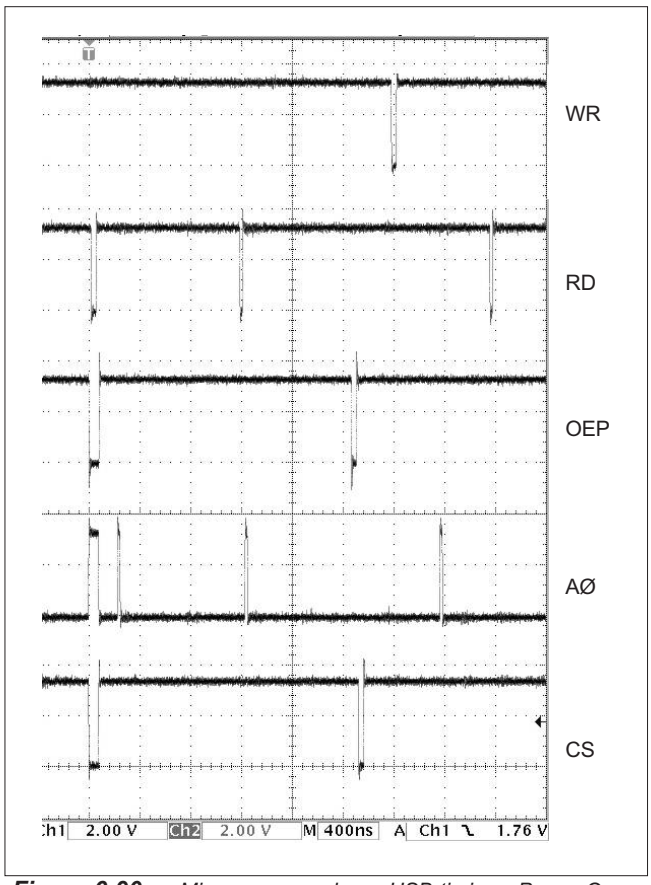

Figure 6-90 *Microprocessor bus - USB timing - Power On.*

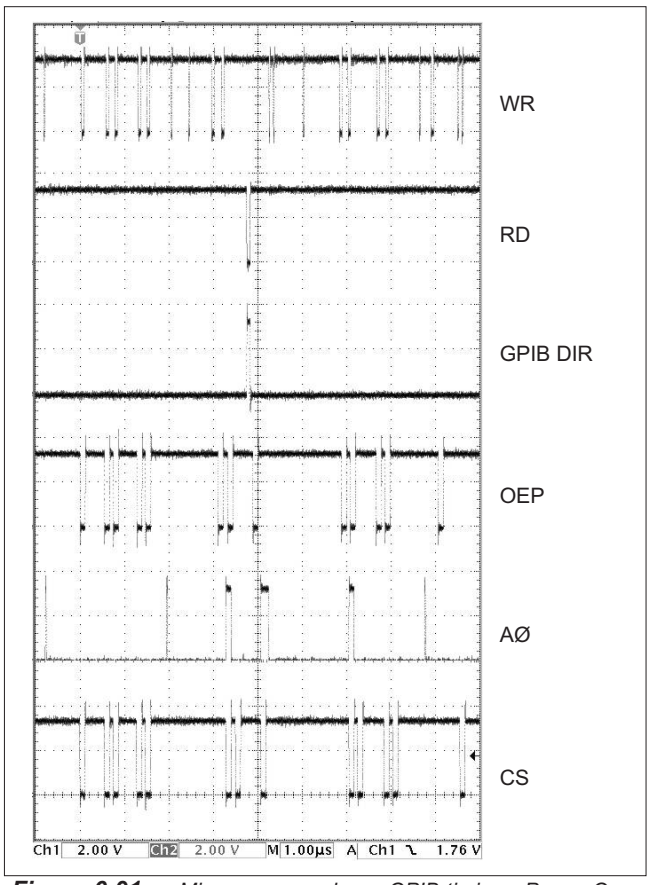

Figure 6-91 *Microprocessor bus - GPIB timing - Power On.*

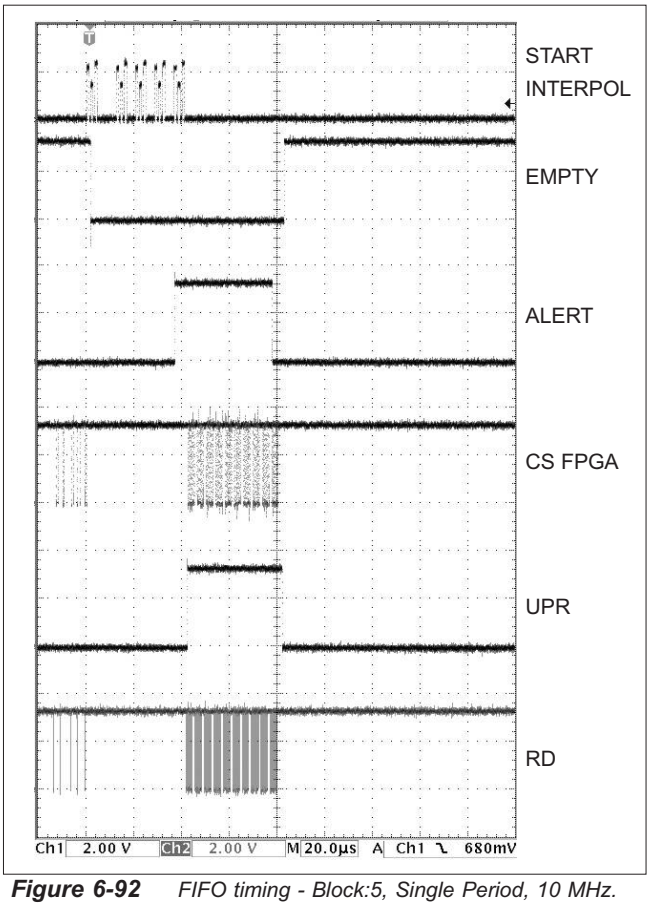

Figure 6-92 *FIFO timing - Block:5, Single Period, 10 MHz.*

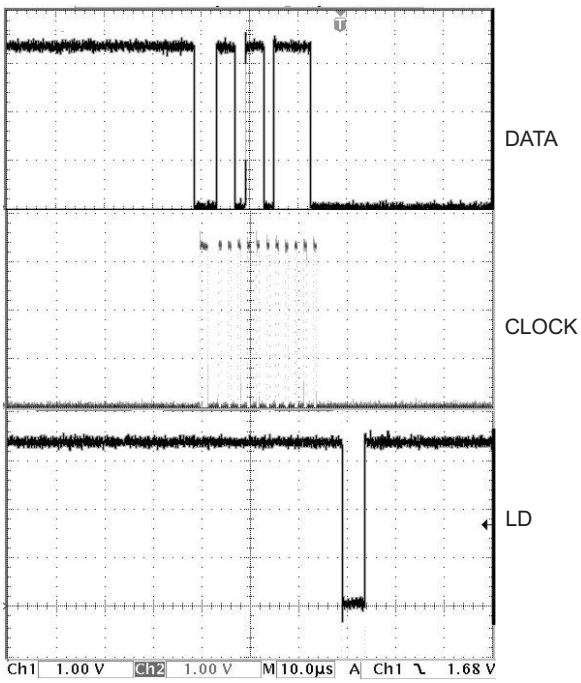

Figure 6-93 *SPI bus activity - oven - directly after power-up.*

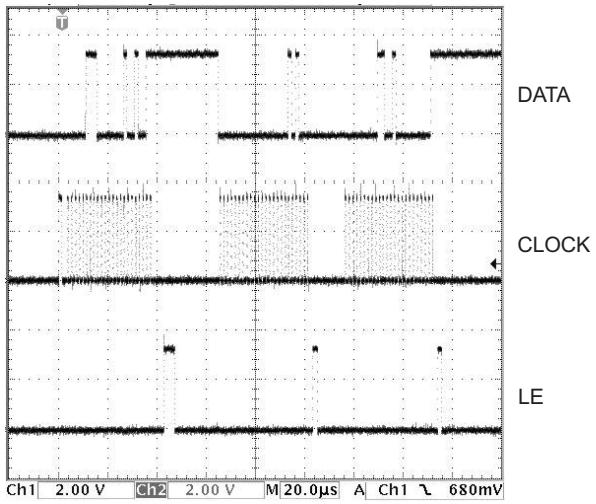

Figure 6-94 *SPI bus activity - PLL - directly after power-up.*

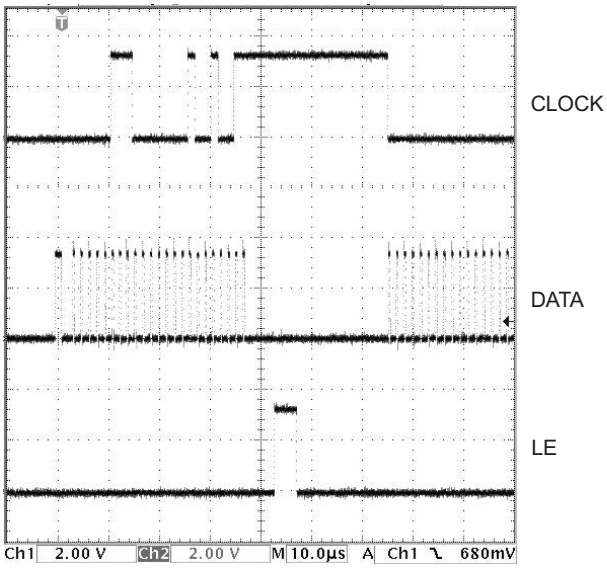

Figure 6-95 *SPI bus activity - PLL - first transfer close-up.*

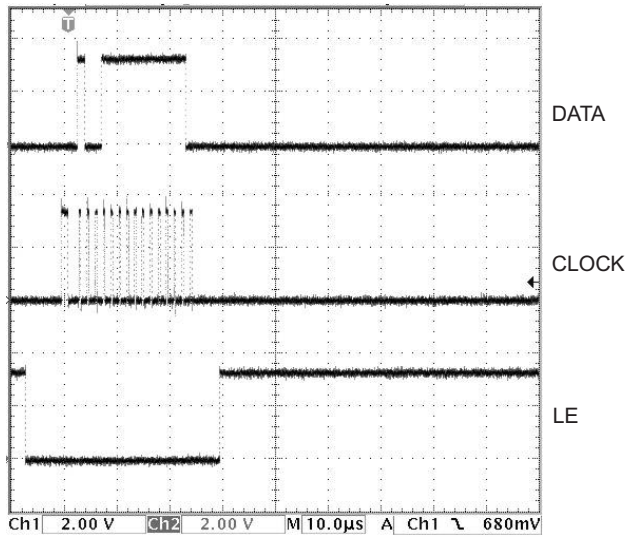

Figure 6-96 *SPI bus activity - trglvl.*

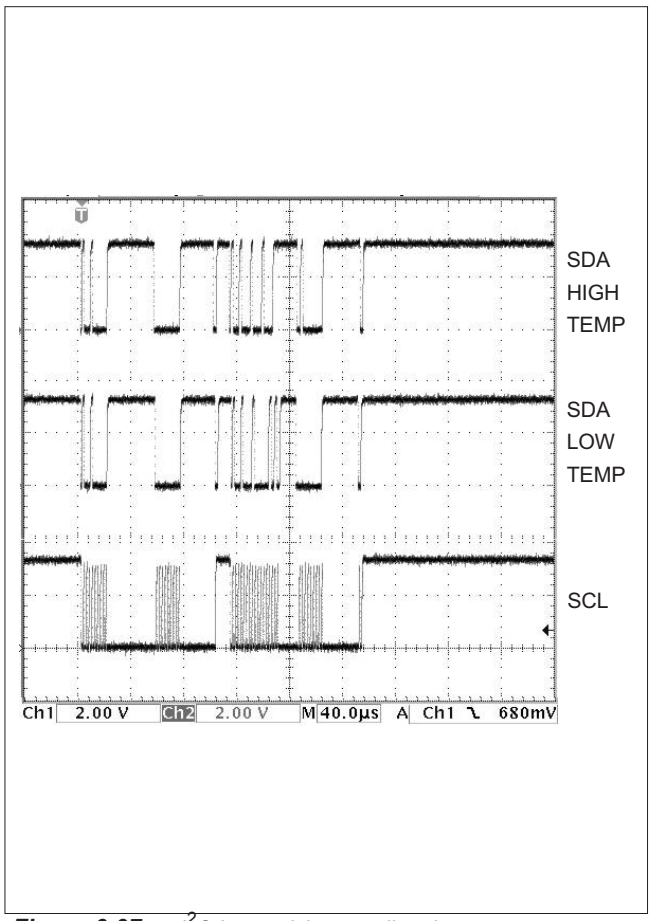

Figure 6-97 *I^2C bus activity - reading the temperature.*

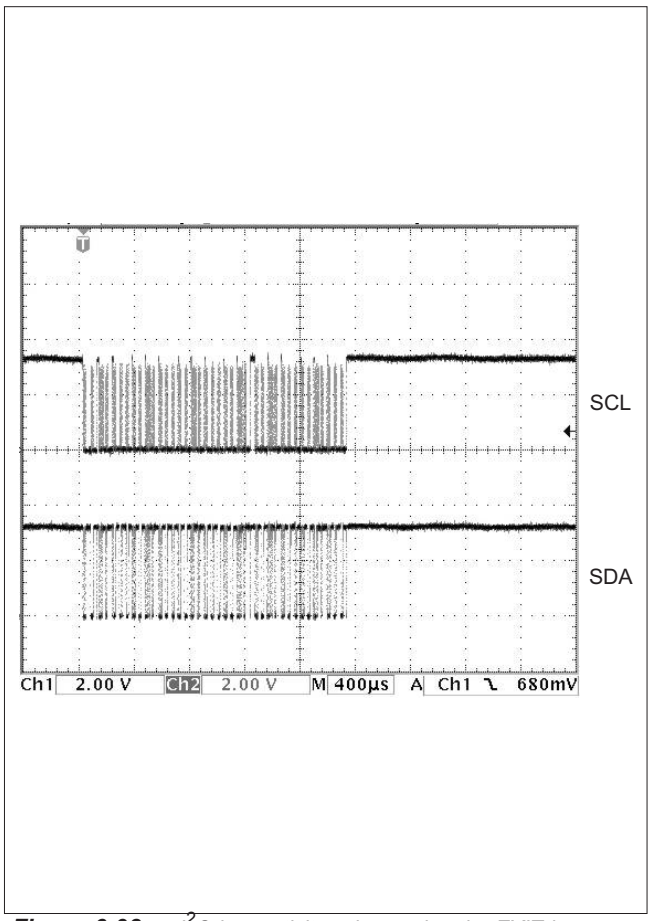

Figure 6-98 *I^2C bus activity - depressing the EXIT key.*

■ The I^2C Bus in the '90'

The processor is the Master on the I^2C bus. Slaves on the bus are:

- The digital I/O IC U40 with address 20hex. It controls the relays and filters in the input amplifiers.
- The temperature measuring IC U39 with address 48hex.
- The digital I/O IC U3 with address 21hex. It switches the LCD display on after power-on initialization, it scans the keyboard on the display circuit board.

The bus is connected to the prescaler connector J15 for future use.

See Figure 6-97 and Figure 6-98.

Measuring Logic

The measurements are made in the FPGA. Only four interpolators are external to the FPGA. They increase the basic measurement resolution from 10 ns (100 MHz measurement clock) to less than 100 ps. Different combinations of interpolators are used for different measurement functions; two, three or four in conjunction. The input signals come from the input amplifiers. A, B and SR are differential LVPECL inputs. C, the prescaler input, is a single-ended LVTTL input. The measuring logic also provides three LEDs on the front panel with control signals.

The interpolator transforms a pulse width between 20 and 33 ns to a voltage. This voltage is read by an ADC. The interpolator is calibrated by reference pulses having a width of 20 and 30 ns . The measurement pulse varies between 22 and 32 ns typically. The ADC has two reference voltages, the lower limit and the upper limit. The interpolated voltage must never fall outside these limits.

Select the default setting from the front panel. Apply a 10 MHz sinewave signal (stable low jitter signal) to input A. The signal should be found at the pins of the FPGA. Check that the measurement signal is present on pins 10 and 11 (differential input) on the FPGA U11.The trigger indicator LED A on the front panel should blink. The gate indicator on the front panel should also blink and the display should show the measurement result. In this setting the S/R flip-flop U12 is used. Check that the measurement signal is present on pins 45 and 46 (differential input) on the FPGA U11.

Move the 10 MHz sinewave signal to input B. Change the measurement function to Frequency B. Check that the measurement signal is present on pins 20 and 21 (differential input) on the FPGA U11. The trigger level LED B and the gate indicator LED should blink and the display should show the measurement result.

Move the 10 MHz sinewave signal back to input A. Change the measurement function to Period Single A. Now the S/R flip-flop should not be used, check the control signal at R623, it should be -1.6 V (on is -1.0 V). Select statistics. The std deviation should be less than 100 ps.

Change the measurement function to Time Interval A - A. Select Statistics Mode. Check that the standard deviation is less than 100 ps. Measure at pin 8 of the ADCs U23, U22, U21 and U20. See Figure 6-100 for a typical timing diagram. Check the upper (TP3) and lower (TP4) voltage limits of the ADCs. They should be approximately 3.5 - 3.6 V and 1.0 - 1.4 V. The important thing is that the lowest voltage pulse on any pin 8 of the ADCs (U23, U22, U21, U20) should be at least 0.2 V above the lower limit and that the highest voltage pulse on any pin 8 of the ADCs should be at least 0.3 V below the upper limit. If an interpolator has a voltage pulse outside the limits the measurement result will be wrong. Figure 6-101 shows the signals on an ADC.

The signal from the prescaler is connected to pin 22 (single-ended) of U11. It comes via a level converter. Check the input signal to the converter at R335 (PECL levels).

If the FPGA or a part in the interpolators has been changed or repaired, a calibration of internals must be performed afterwards. See Chapter 7.

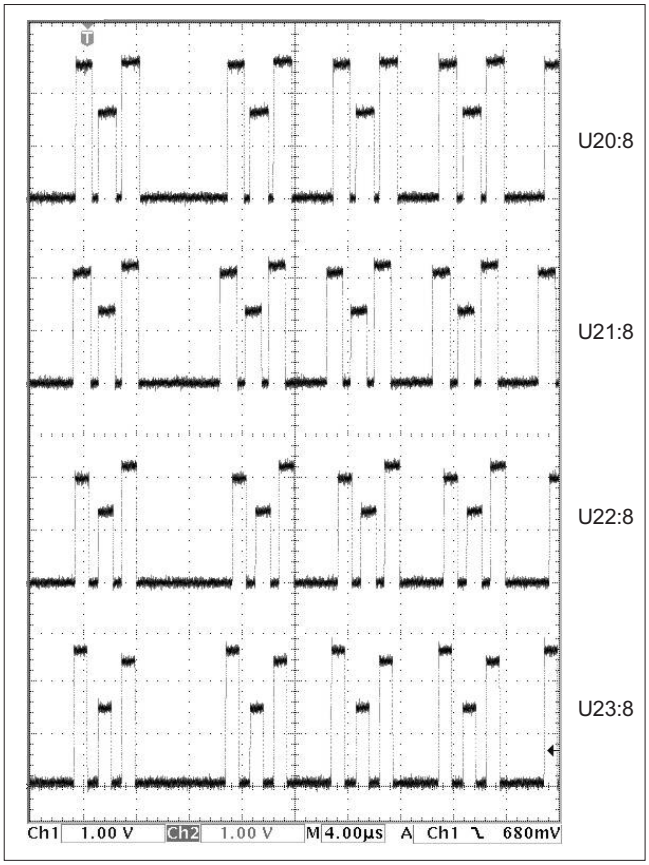

Figure 6-100 *ADC 10461 behavior. Time A-A Smart, 10 MHz in, block measurement.*

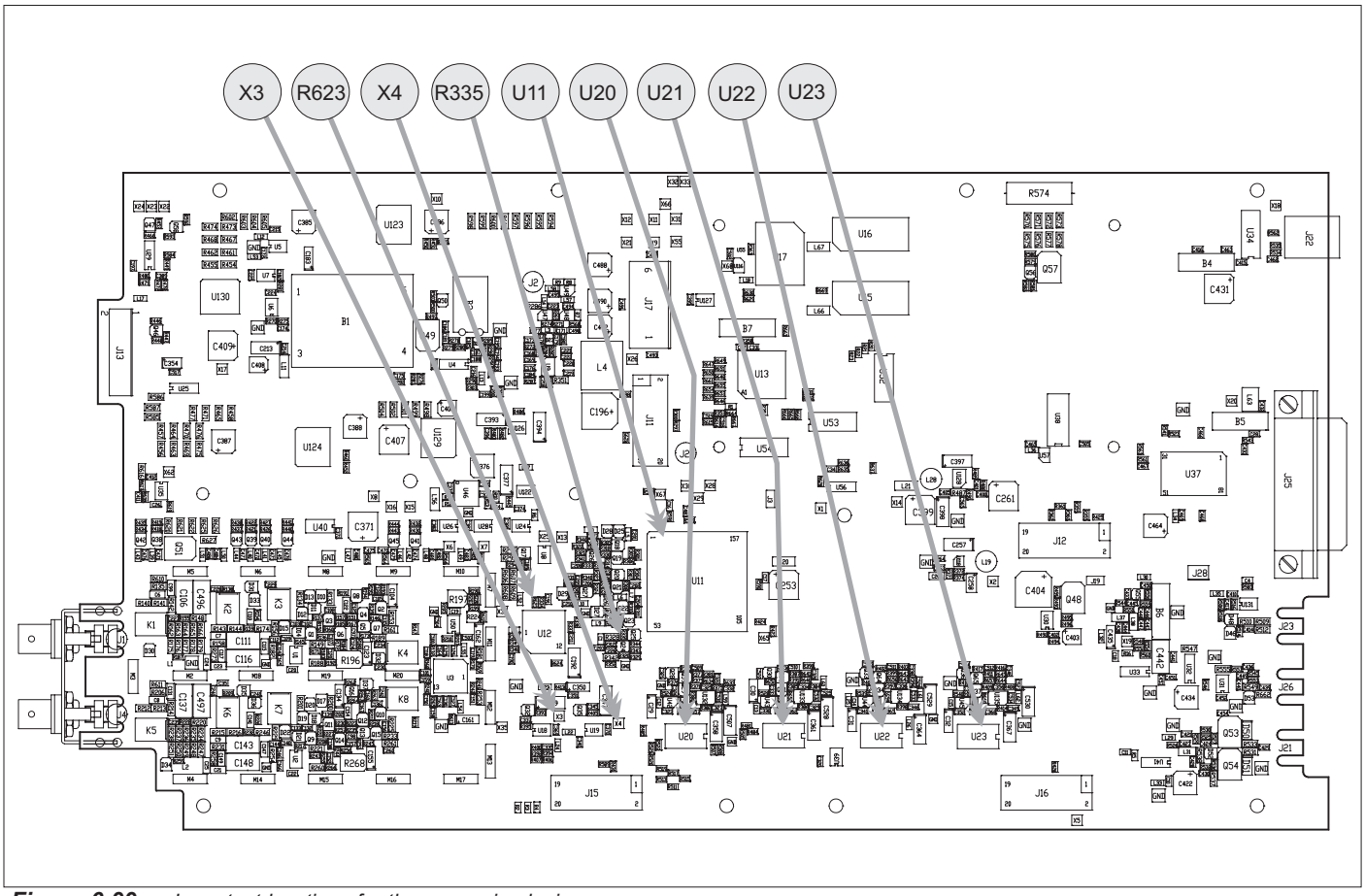

Figure 6-99 *Important locations for the measuring logic.*