WHAT IS UNIQUE ABOUT THE 8060A A/D CONVERTER

I. 10 uV resolution and 20,000 counts in monolithic CMOS, achieved by solutions to noise and linearity.

II. Method of gain changing resulting in greatly improved stability and low noise.

III. Microcomputer control of A/D and acquisition of data.

I. 10 uV resolution has not been achieved in monolithic CMOS because of: 1. Noise problems, both 1/f and thermal noise in the CMOS switches. 2. Linearity problems.

Noise problems were addresssed in two areas: The input noise of the buffer, integrator, and comparator, and the thermal noise of the CMOS switches. The use of large input transistors was very important in reducing the noise of the buffer and integrator op amps. Low resistance CMOS switches were used at critical nodes to reduce their contribution to noise.

In order to reduce noise to a level allowing a "dead quiet" display (no flicker), a digital filter was implemented. This is a software filter in the program ROM of the SM-4 Microcomputer. As implemented, it is a recursive filter which averages four succesive readings. But, unlike analog filters, it responds to step changes instantaneously. Any input change greater than four counts is displayed immediately, and the averaging then starts from the new value.

To improve linearity, the A/D converter actually resolves 80,000 counts at full scale, which gives 1/4 count resolution and reduces digitizing error by a factor of four. The microcomputer divides the total count by four before routing it to the display.

II. Integrator gain change is key

Both a 200mV and 2 Volt range of A/D conversion are necessary for modern full range multimeters. To accomplish a dual range converter a method of changing the A/D scaling had to be developed. Conventionally, a times 10 amplifier would be employed for the 200 mV range. This was not an acceptable solution because offsets would also be multiplied by 10 and therefore an additional autozero loop would be required. By employing a precision resistor R-10R network, the gain of the integrator can be changed depending on which range is desired. For the 200 mV range, the integrator gain is 20, and for the 2 V range, the integrator gain is 2. This made the full scale integrator output swing plus or minus 4 volts rather than the 2 volts typical of most converters. By making the resolution 200 uV per count at the output of the integrator, noise performance required of the comparator is halved. Also, since the slope of the integrator output is doubled, the speed and delay performance required of the comparator is halved.

Even with these improvements the design of the comparator was a formidable challenge. The speed and gain required of the comparator exacted an unacceptable stability penalty. This was solved by splitting the comparator into two devices. The first comparator has the low noise and speed requirement, but not quite enough gain. The second comparator makes up for the gain deficiency. Also, since the second comparator does not need to be in the autozero loop, overall gain in the loop is reduced, thus making the loop more stable.

III. The Microcomputer

The A/D converter is controlled through a four bit bidirectional bus which connects to the sytem microcomputer. The count that is proportional to the A/D input signal is read back through the same 4 bit buss. The major advantage of this approach is that the digital circuitry required in the MAC is greatly reduced. The MAC has only a 12 bit counter in place of the usual 16 bit counter (15 bits plus sign) required in 4 1/2 digit A/D converters. The uC picks up overflow carries from the 12 bit counter to complete the count. A further reduction in MAC digital circuitry results from its register structure. The uC eliminates the need for an A/D state machine and the complex timing circuitry usually found in a single chip A/D converter.

By having full control of all the MAC's functions, the uC can manipulate the A/D in unconventional ways. By modifying the conversion sequence, an A/D self check can be performed. This check, called the ratio test, uses the reference voltage for both phases, Integrate and Read. Since the reference is used to reference itself, the resulting count should be 10,000, a perfect 1 to 1 ratio. This user selectable test is useful to verify MAC functionality independent of the front end components. Also by changing the Read period integrator gain from the usual times 2 to times 20, a range equivalent to 20 millivolts full scale can be obtained. This is taken advantage of in the 8060A's 300 megohm range, where the voltage across the reference resistor can be as low as 6 millivolts. The uC can lock the A/D into the AZ phase if it needs more time to manipulate the data. This takes place when a dB conversion is being calculated. At certain cardinal points, the dB conversion can take as long as 400 milliseconds. This slows the total conversion rate to 1.4 readings per second, worst case.

By wedding an A/D converter to a Microcomputer, the performance of a practical instrument can be optimized, combining the analog processing power of the A/D converter, and the digital processing power of the uC. Ease of data manipulation and an enhanced feature set are the obvious benefits.