MS-9642 v2.0

CPU:

Intel Yonah Processor

System Chipset:

Intel 945GM - GMCH (North Bridge)

Intel ICH7M (South Bridge)

On Board Chipset:

Clock Generator - ICS954310

LAN -- INTEL 82573L * 3
LPC Super I/O -- W83627EHG
Azalia ALC888
BIOS -- FWH EEPROM

Main Memory:

DDR 2 * 1 (Max 2GB)

Expansion Slots:

PCI EXPRESS X16 SLOT
PCI EXPRESS X1 SLOT
PCI2.3 SLOT * 1

V-core PWM:

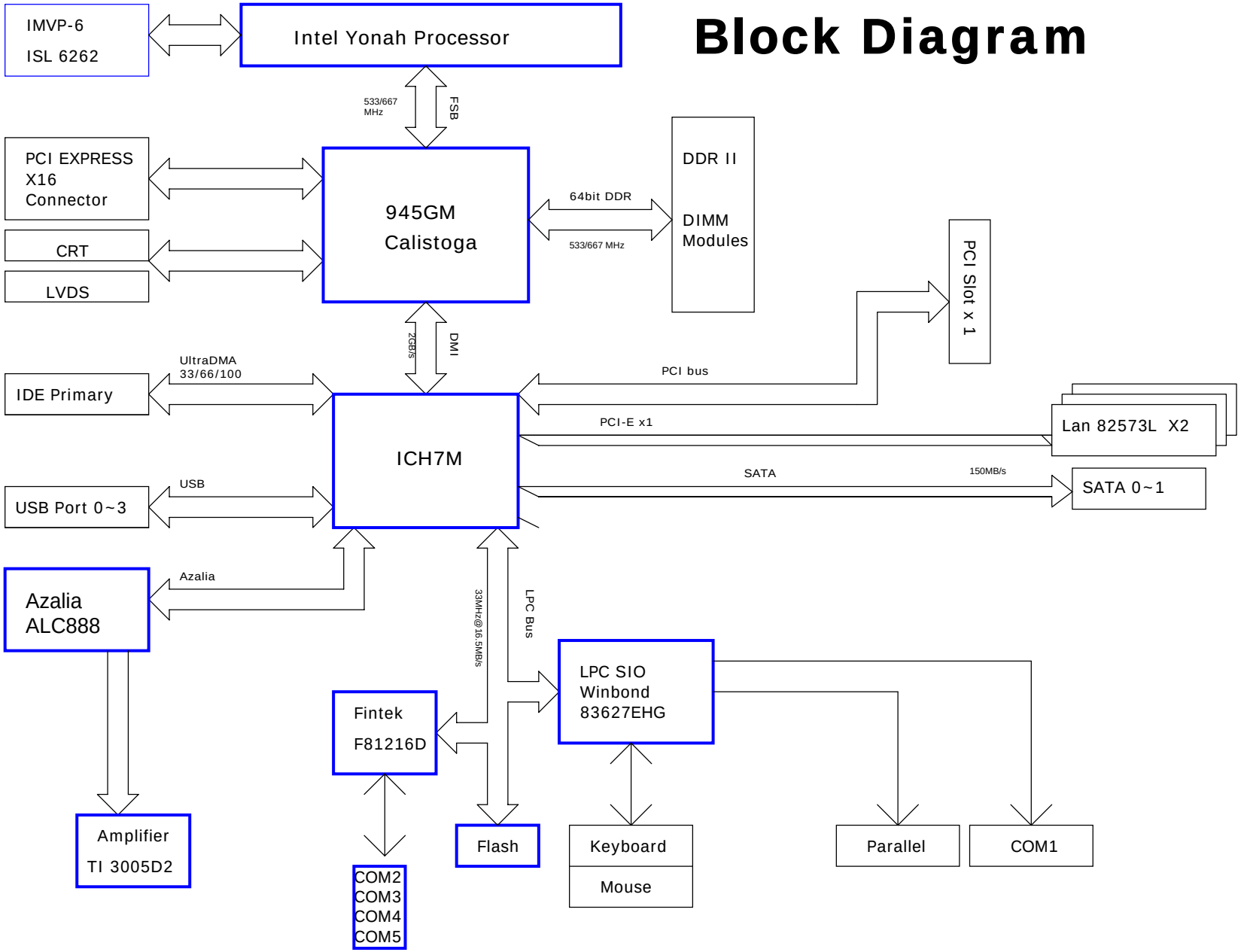
IMVP-6 Controller: ISL6262

System power PWM:

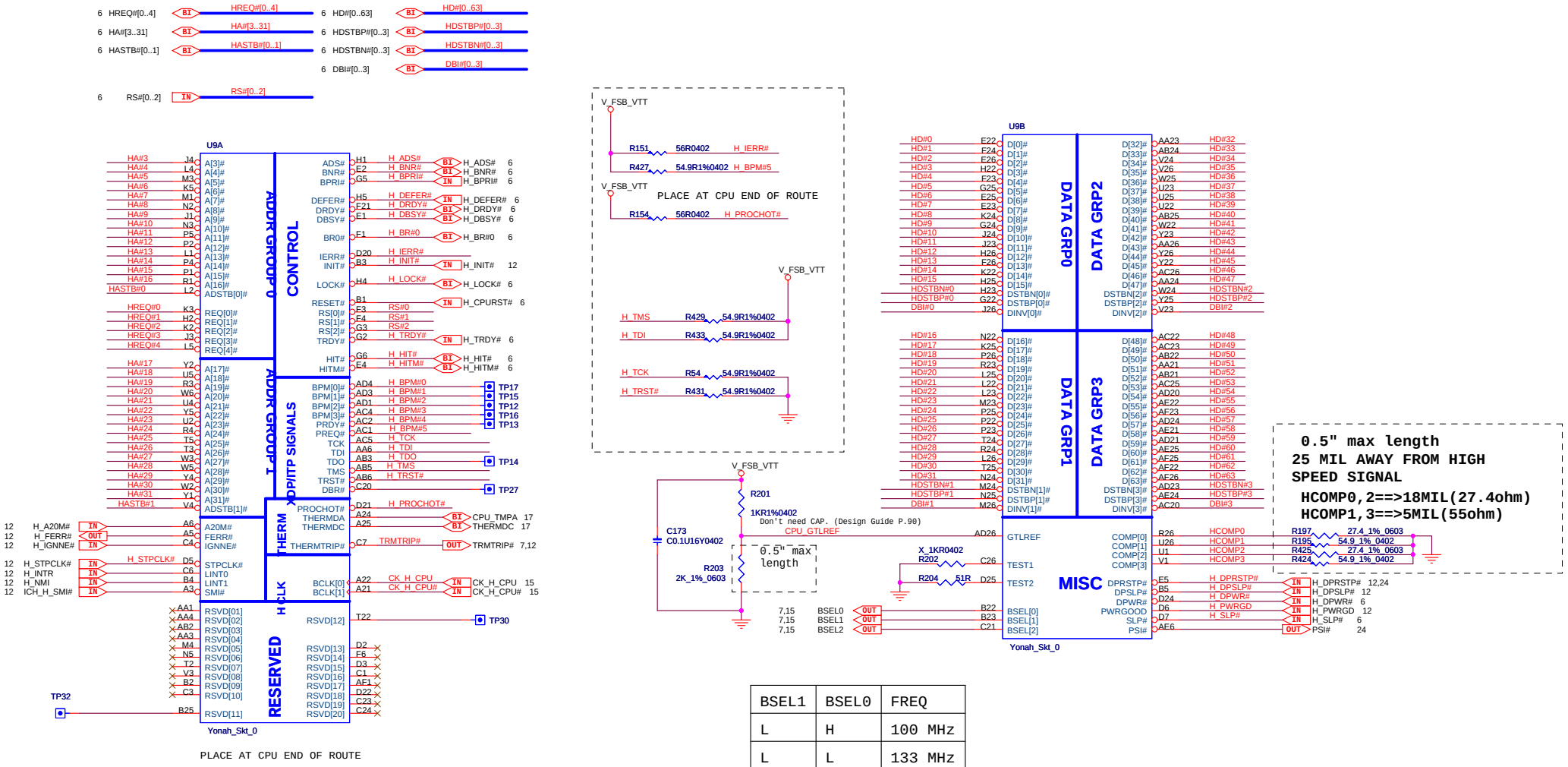
MS-7 & MS-11

MICRO-STAR INt'L CO. , LTD.		
Title: Cover Sheet		
Size: Custom	Document Number: MS-9642 v2.0	Rev
Date: Tuesday, May 08, 2007	Sheet 1 of 38	

Block Diagram

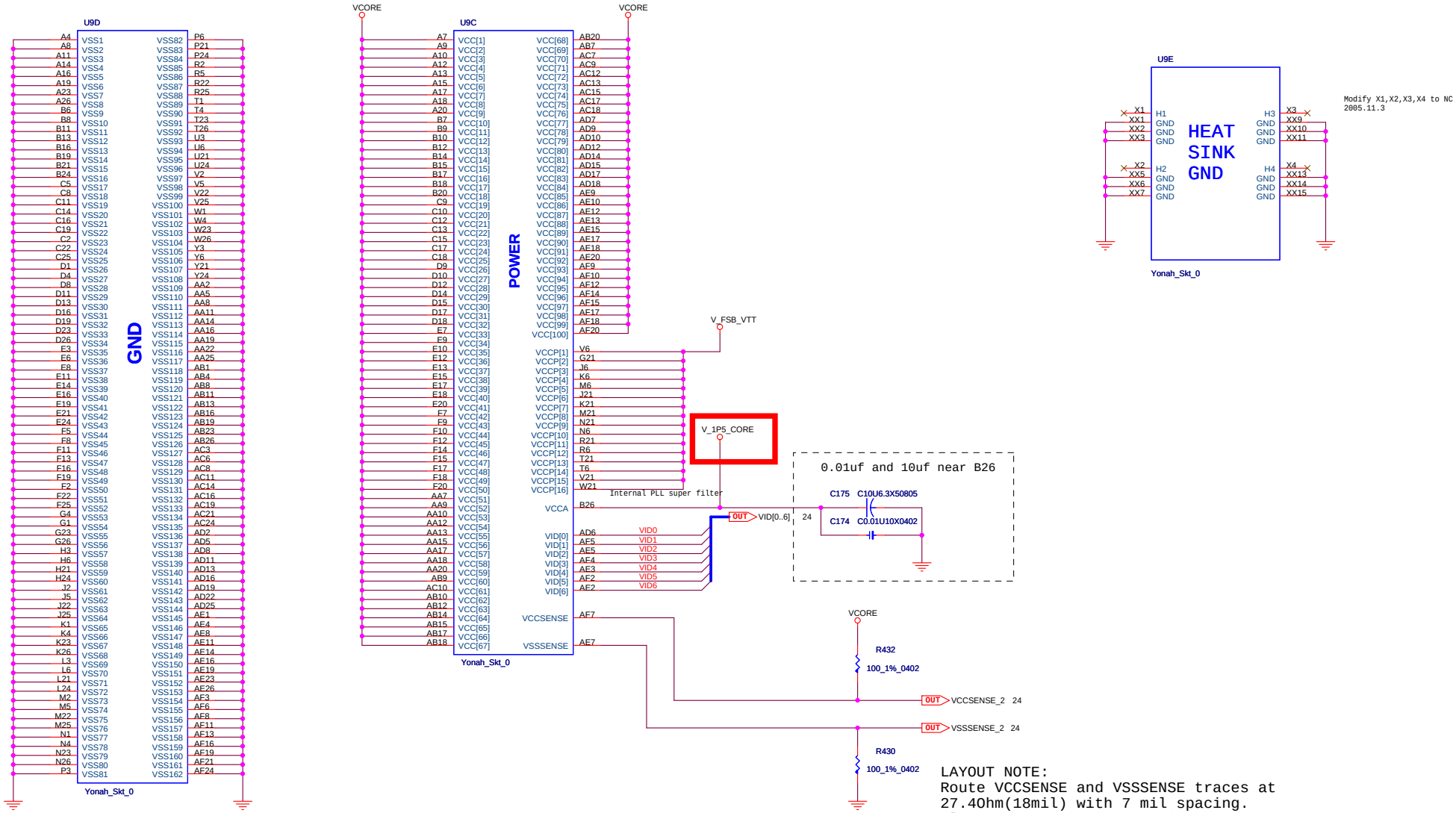


MICRO-STAR INt'L CO. , LTD.			
Title: Block Diagram			
Size: Custom	Document Number: MS-9642 v2.0		Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 2 of 38		



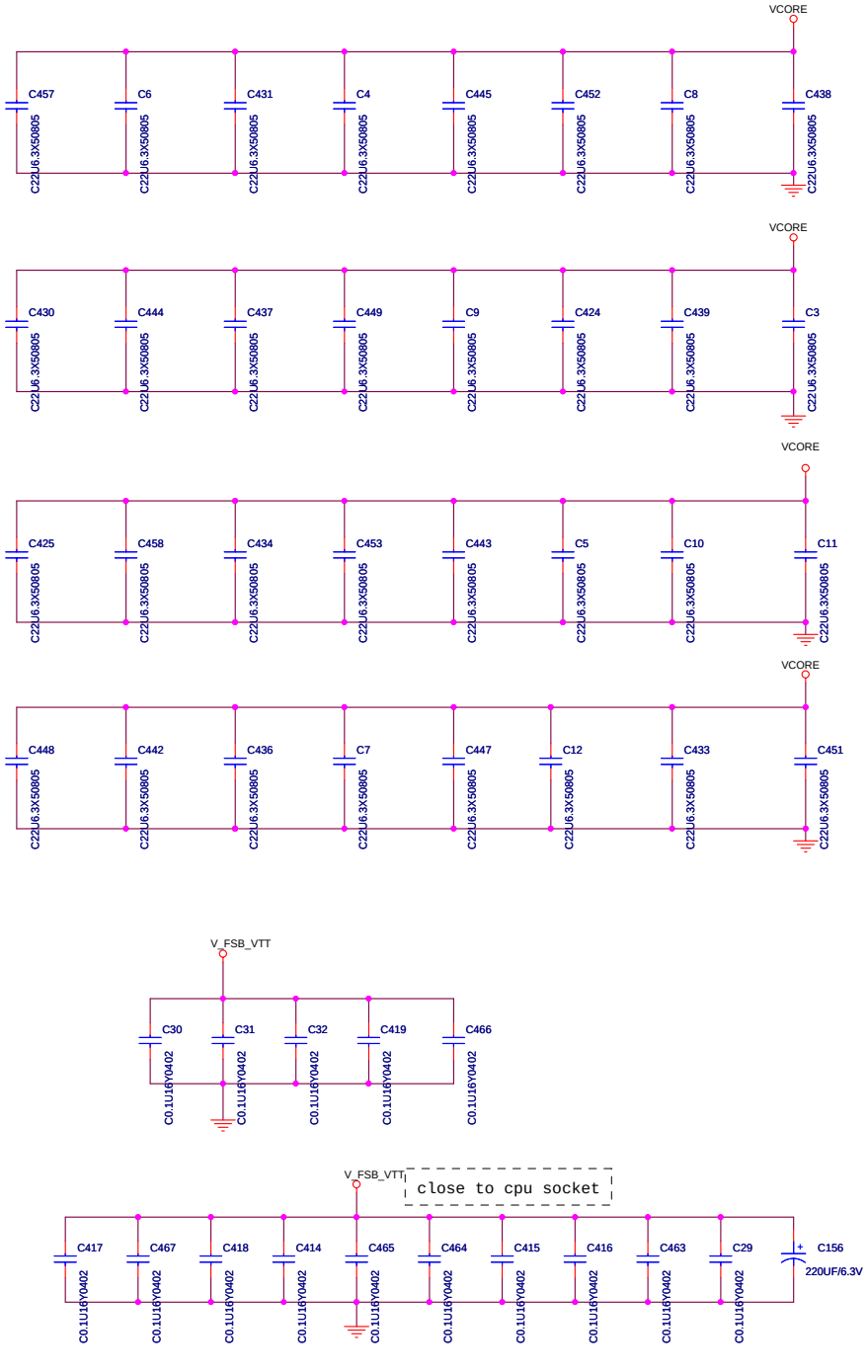
BSEL1	BSEL0	FREQ
L	H	100 MHz
L	L	133 MHz
H	L	REV
H	H	REV

MICRO-STAR INt'L CO. , LTD.	
Title	CPU - Host bus
Size: Custom	Document Number: MS-9642 v2.0
Rev	1.0
Date: Tuesday, May 08, 2007	Sheet 3 of 38

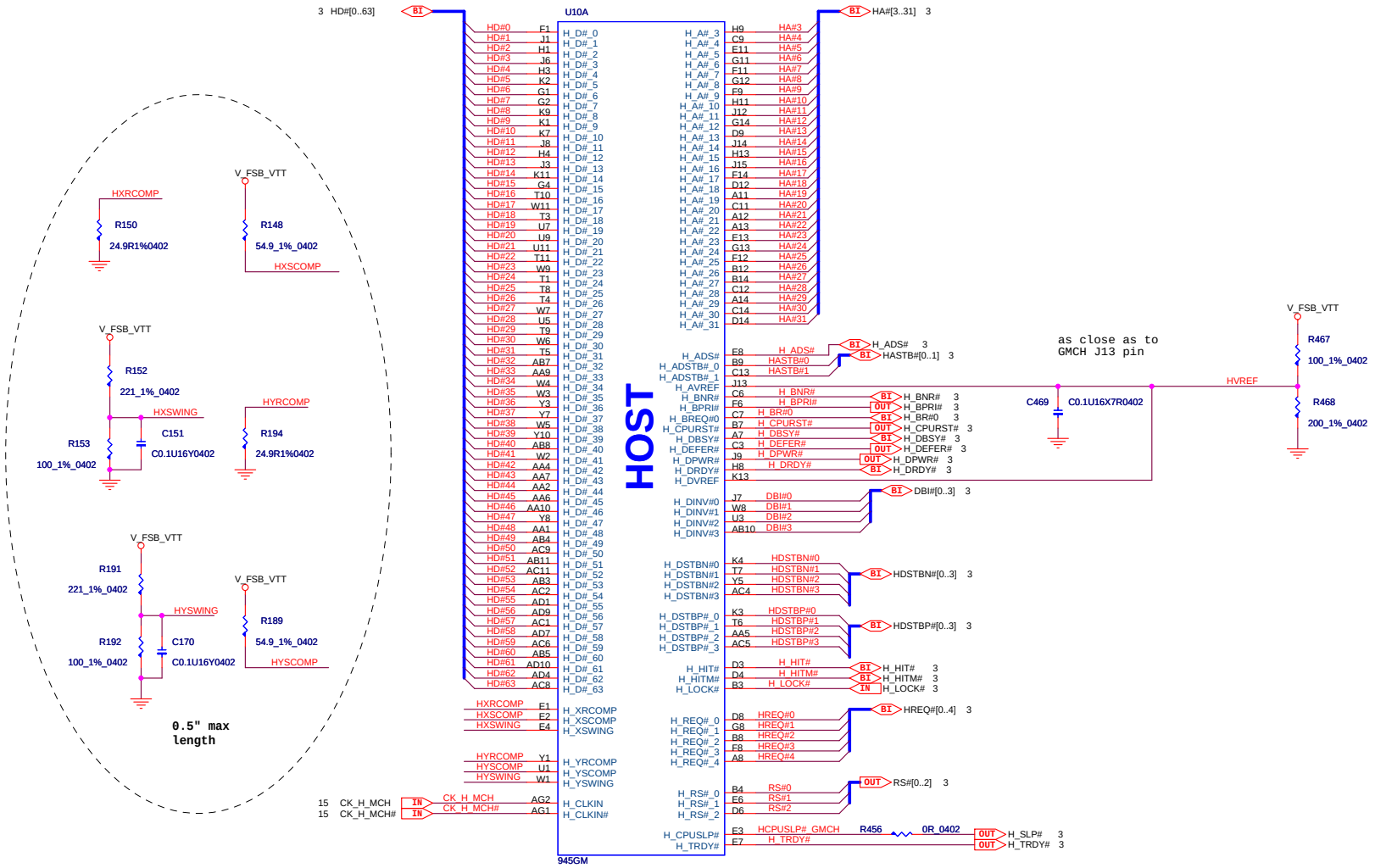


LAYOUT NOTE:
Route VCCSENSE and VSSSENSE traces at 27.4Ohm(18mil) with 7 mil spacing.
Place PU and PD within 1 inch of CPU.

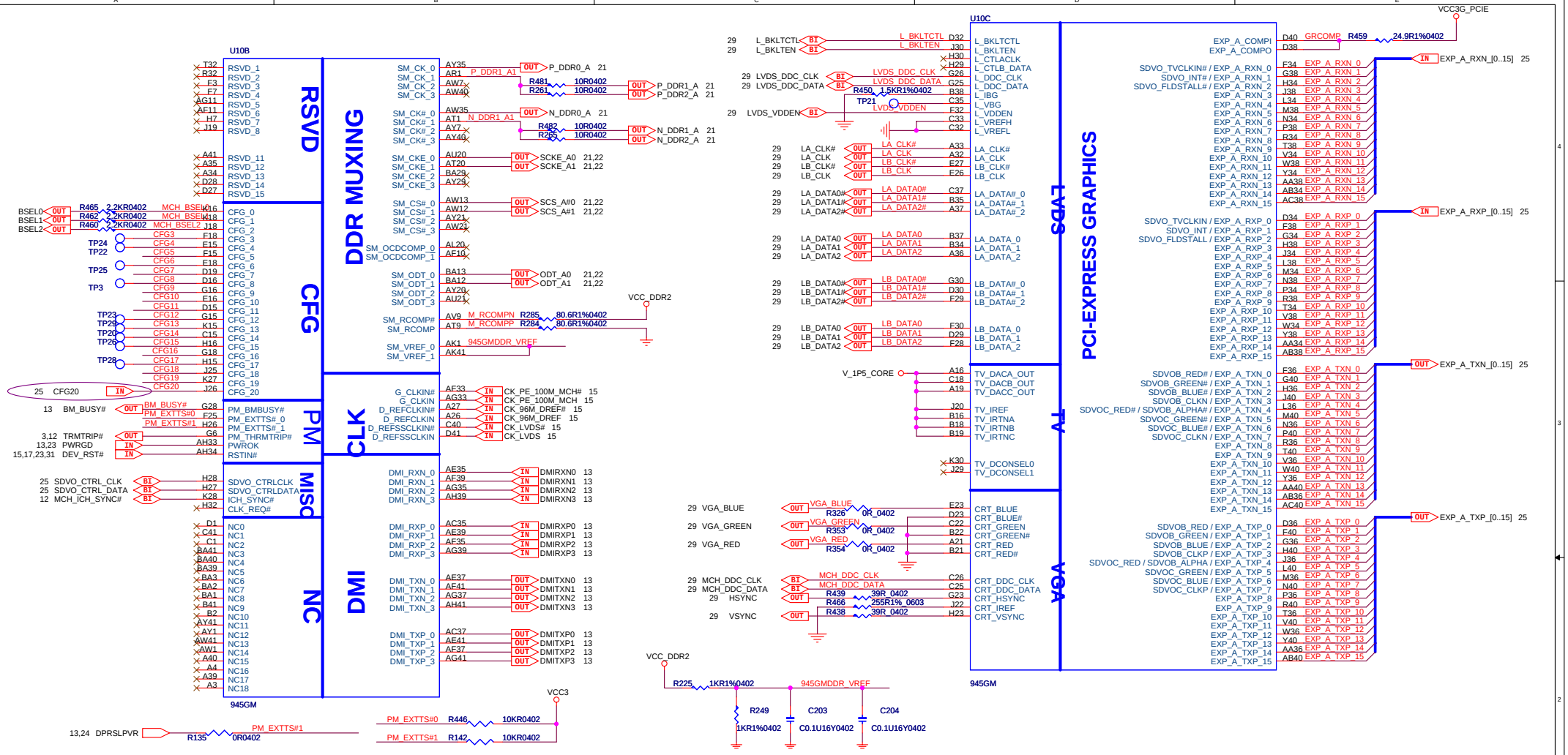
MICRO-STAR INt'L CO. , LTD.		
Title: Dothan - Power / Gnd		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 4 of 38	



MICRO-STAR INt'L CO. , LTD.		
Title: Dothan- Decoupling		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 5 of 38	

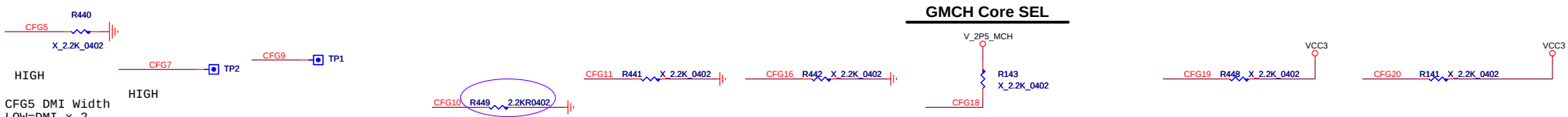


MICRO-STAR INt'L CO. , LTD.		
Title: GMCH1- Host		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 6 of 38	



NB strapping

CFG[3:17] Internal Pull up **CFG[18:20] Internal Pull down**



HIGH

CFG5 DMI Width
LOW=DMI x 2
HIGH=DMI x 4

HIGH

CFG7 CPU STRAP
LOW=REVERSED
HIGH=MOBILE CPU

CFG9 PCIE Graphics
LOW=REVERSE LAN
HIGH=NORMAL

LOW

CFG10 HOST PLL VCO SELECT
LOW=REVERSED
HIGH=MOBILITY

HIGH

CFG11 PSB 4X CLK ENABLE
LOW=4X ENABLE
HIGH=8X

HIGH

CFG16 FSB Dynamic ODT LOW=Dynamic ODT Disabled
HIGH=Dynamic ODT Enabled

HIGH

CFG18 VCC Select
LOW=1.05V
HIGH=1.5V

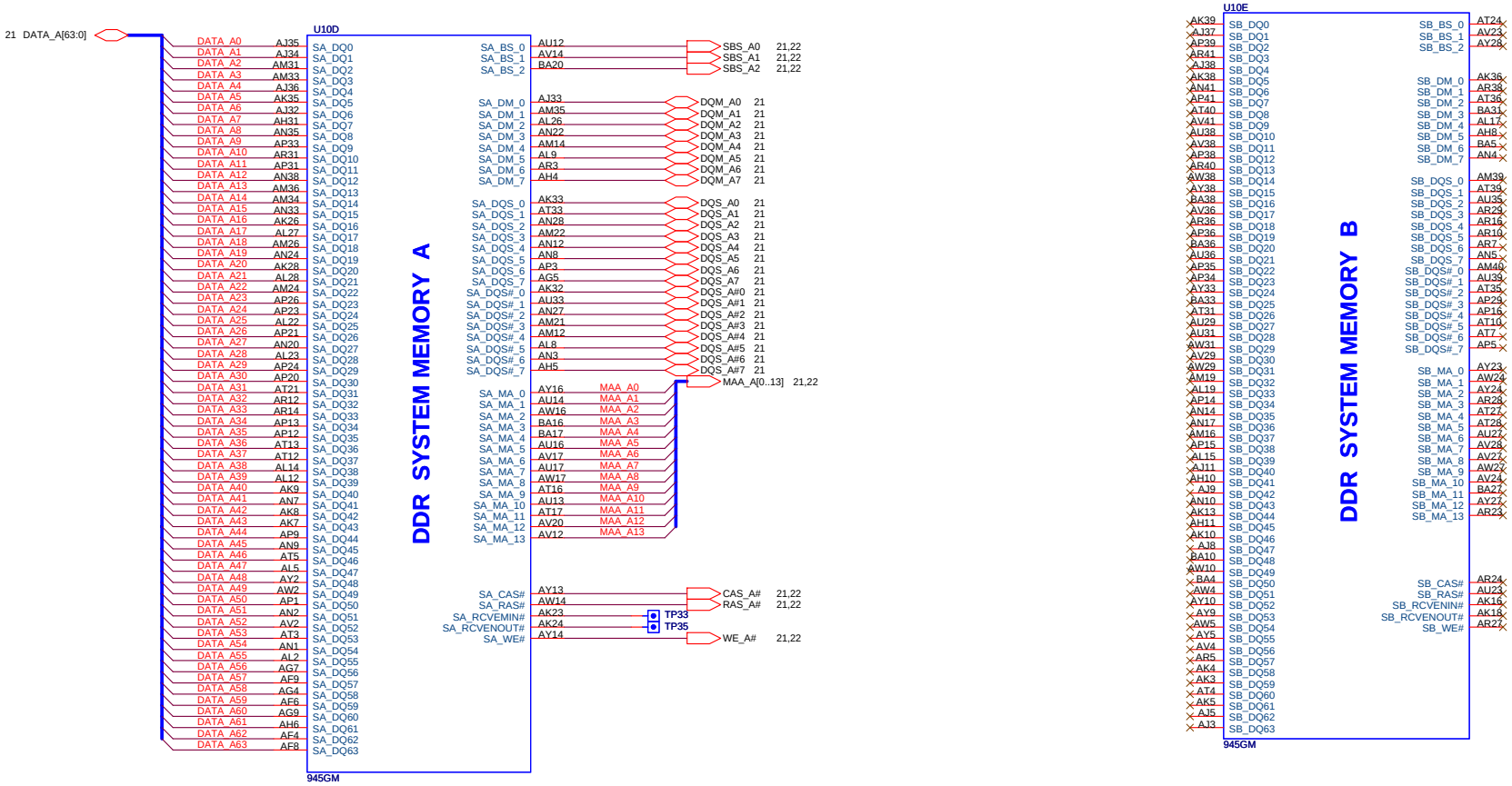
LOW

CFG19 DMI LANE REVERSAL LOW=Normal
HIGH=LANES REVRSED

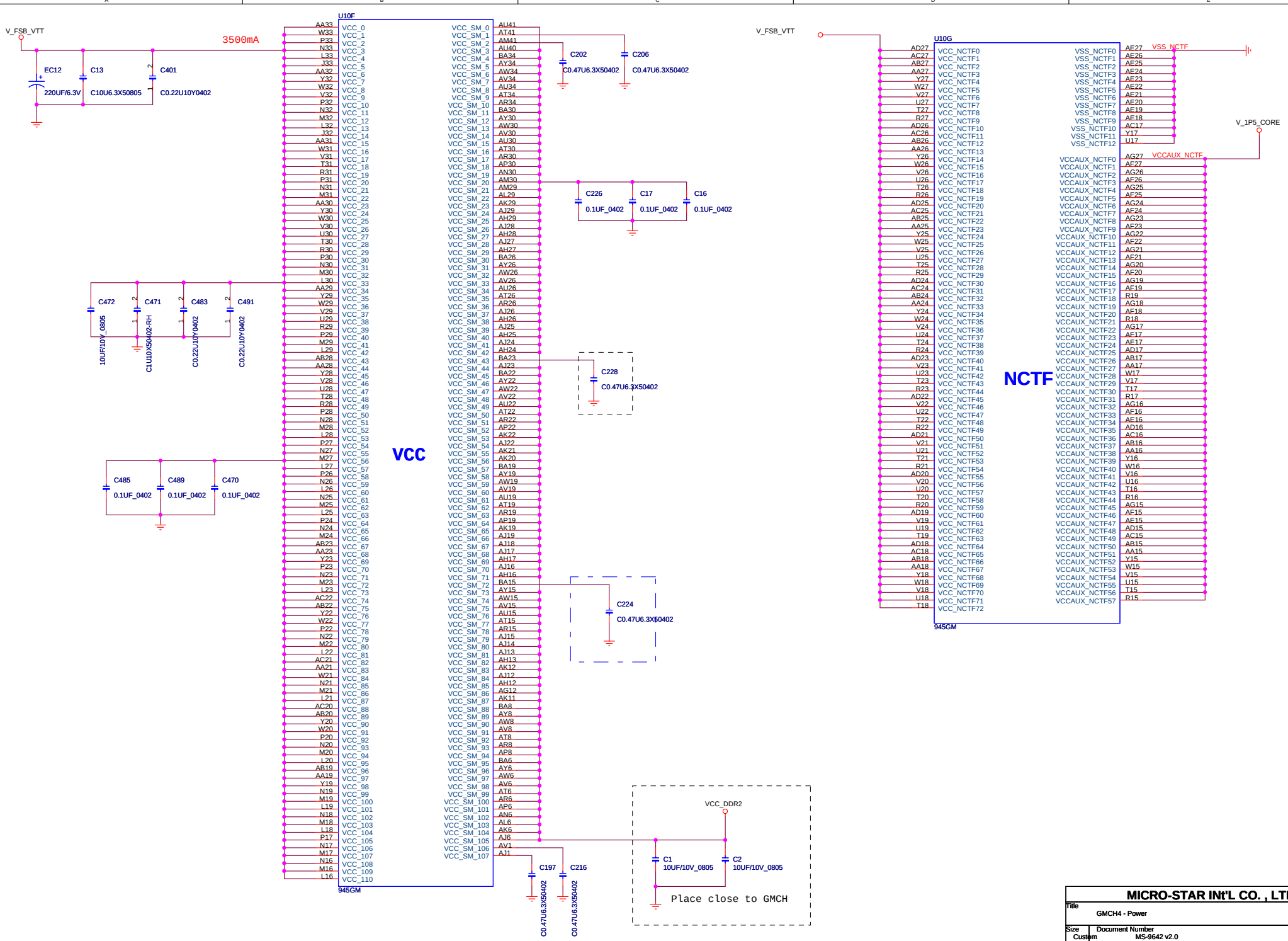
LOW

CFG20 SDVO/PCIe concurrent
LOW=Only SDVO or PCIE x 1 is operational
HIGH=SDVO and PCIE x 1 are operating simultaneously via the PEG port

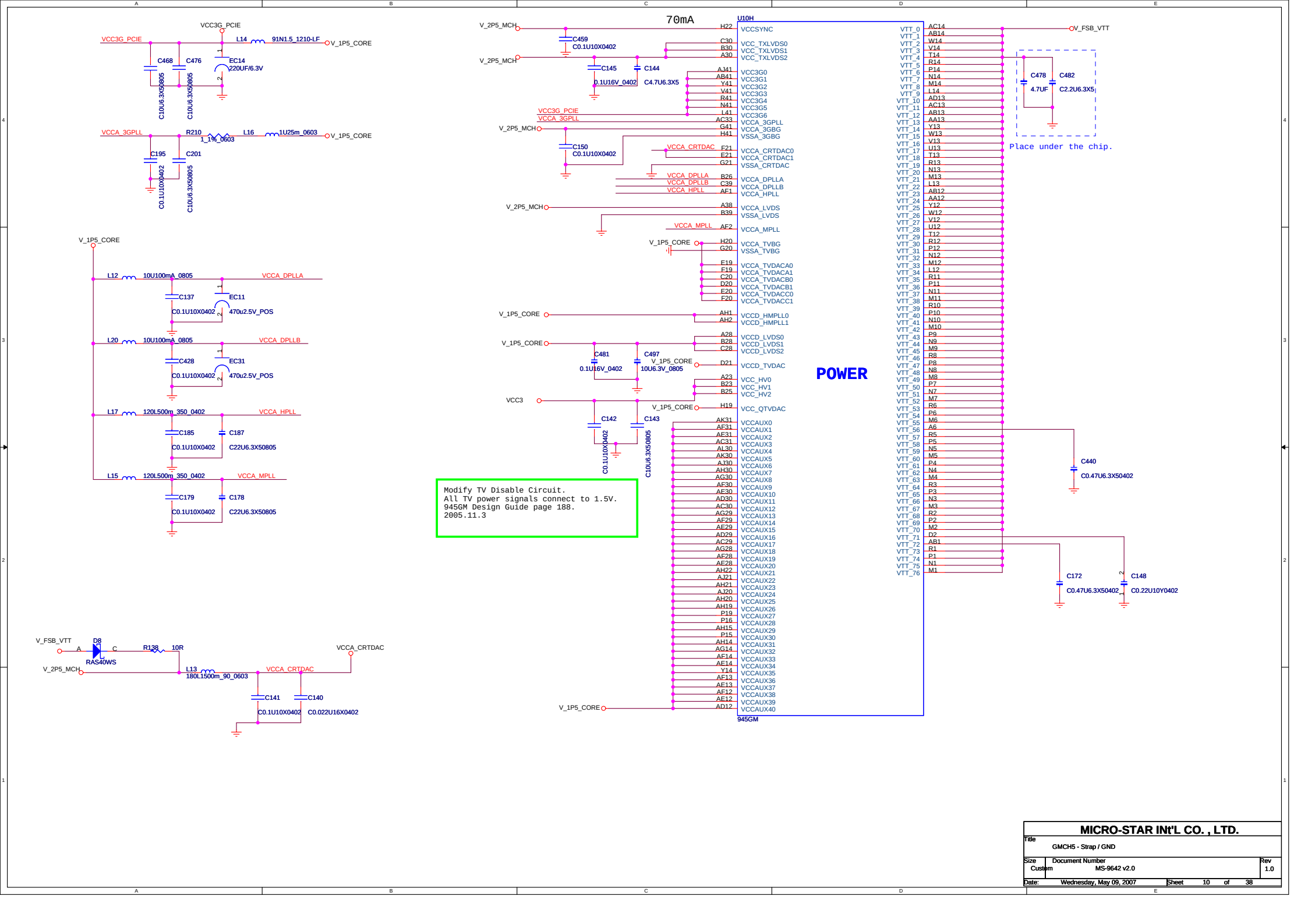
MICRO-STAR INt'L CO. , LTD.			
Title: GMCH2-PCIE/DMI/CRT			
Size: Custom	Document Number: MS-9642 v2.0		Rev: 1.0
Date: Tuesday, May 08, 2007		Sheet 7 of 38	

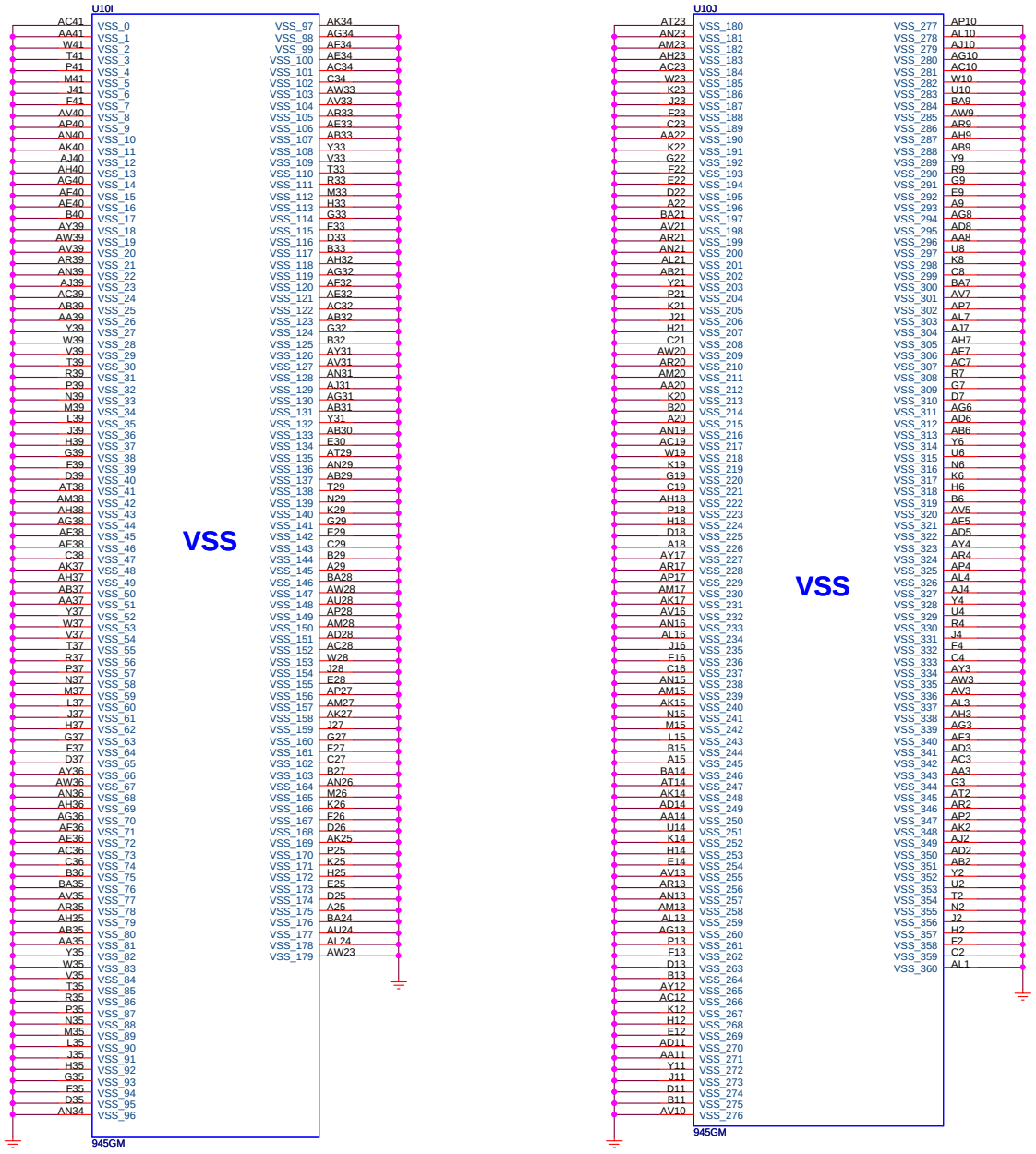


MICRO-STAR INt'L CO. , LTD.			
Title: GMCH3-MEM			
Size: Custom	Document Number: MS-9642 v2.0		Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 8 of 38		

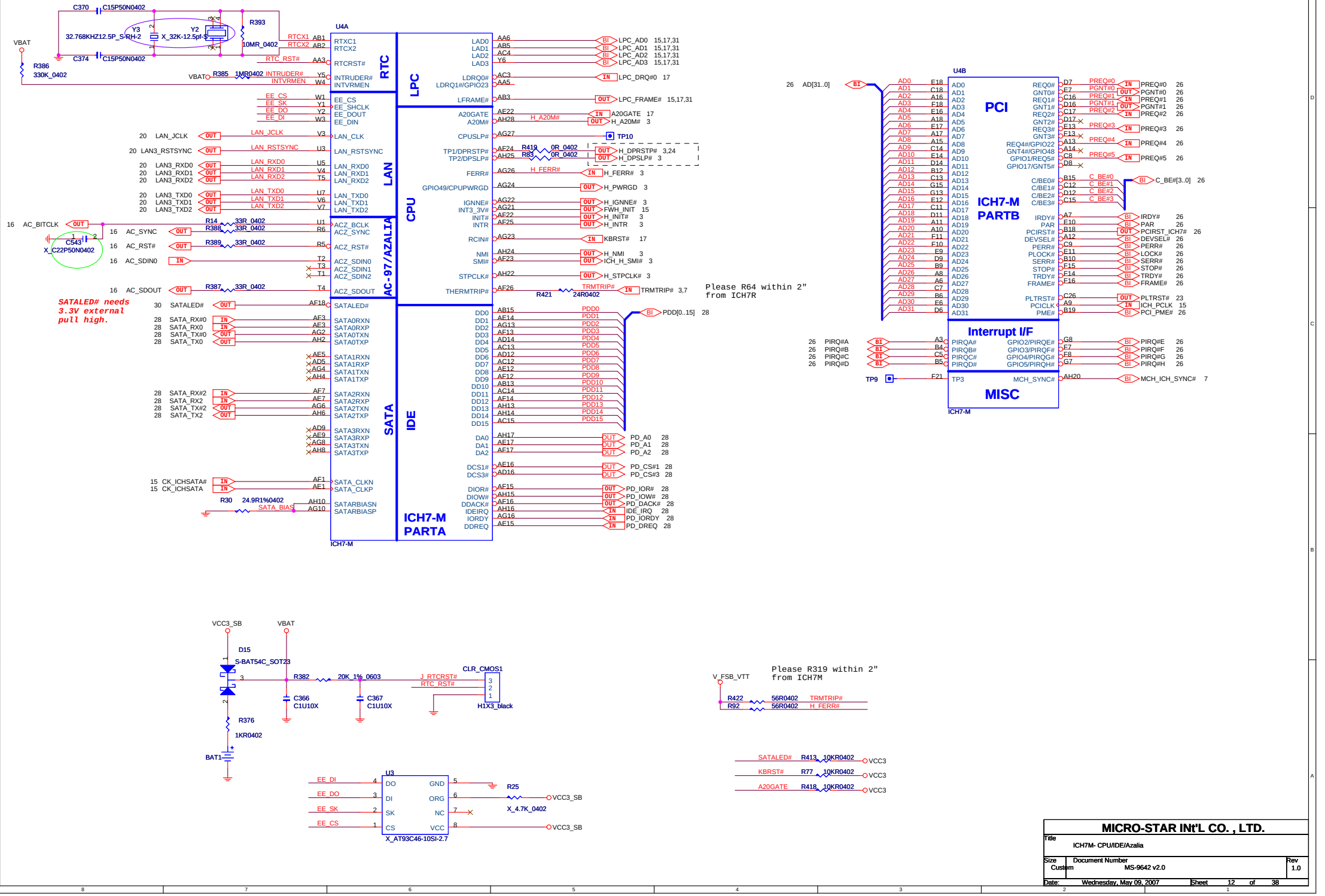


Company	MICRO-STAR INt'L CO. , LTD.
Title	GMCH4 - Power
Size	Custom
Document Number	MS-9642 v2.0
Rev	1.0
Date	Tuesday, May 08, 2007
Sheet	9 of 38

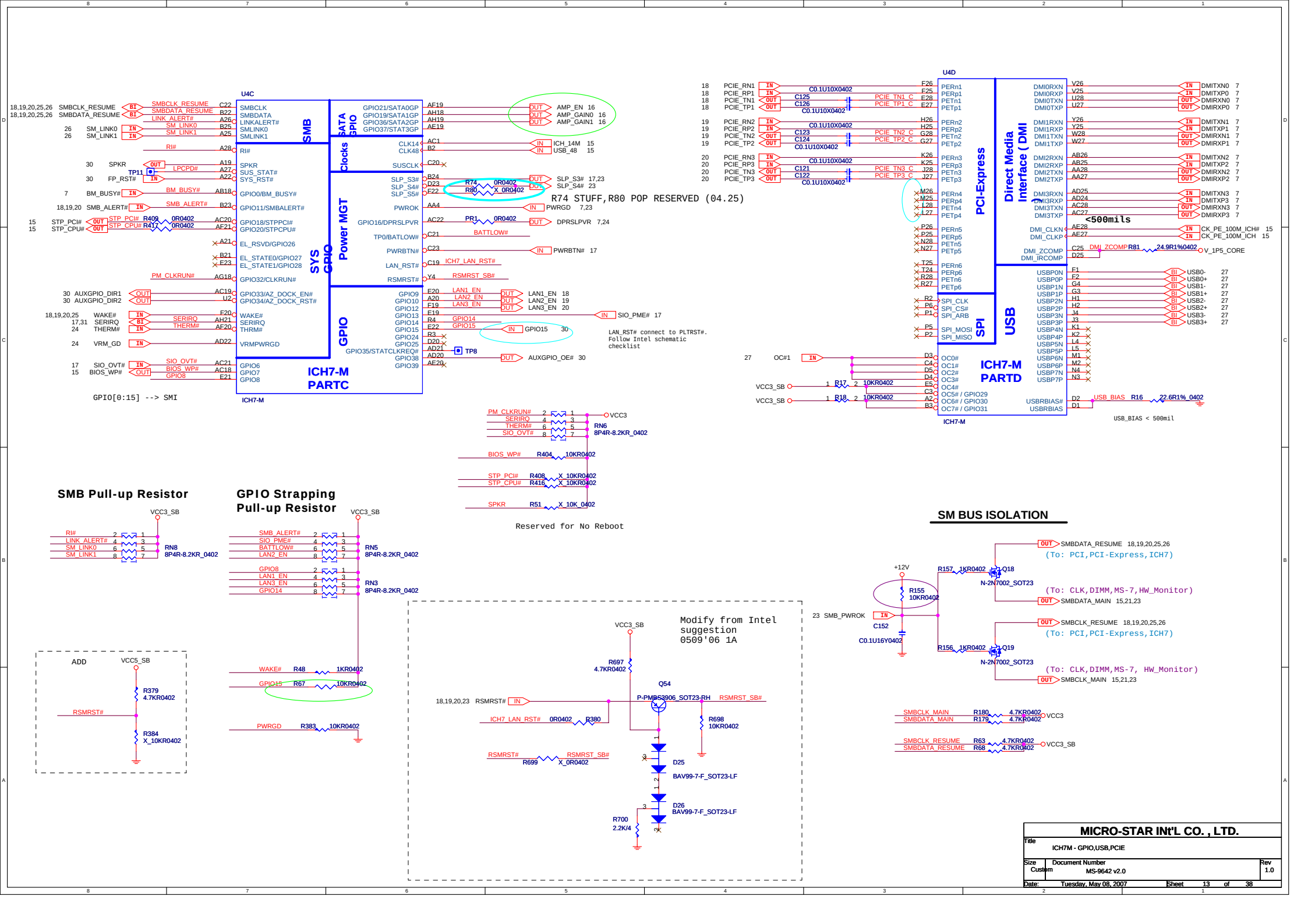

70mA
POWER
U10H
945GM
Modify TV Disable Circuit.
All TV power signals connect to 1.5V.
945GM Design Guide page 188.
2005.11.3
Place under the chip.
MICRO-STAR INt'L CO. , LTD.
Title
GMCH5 - Strap / GND
Size
Custom
Document Number
MS-9642 v2.0
Rev
1.0
Date:
Wednesday, May 09, 2007
Sheet
10
of
38

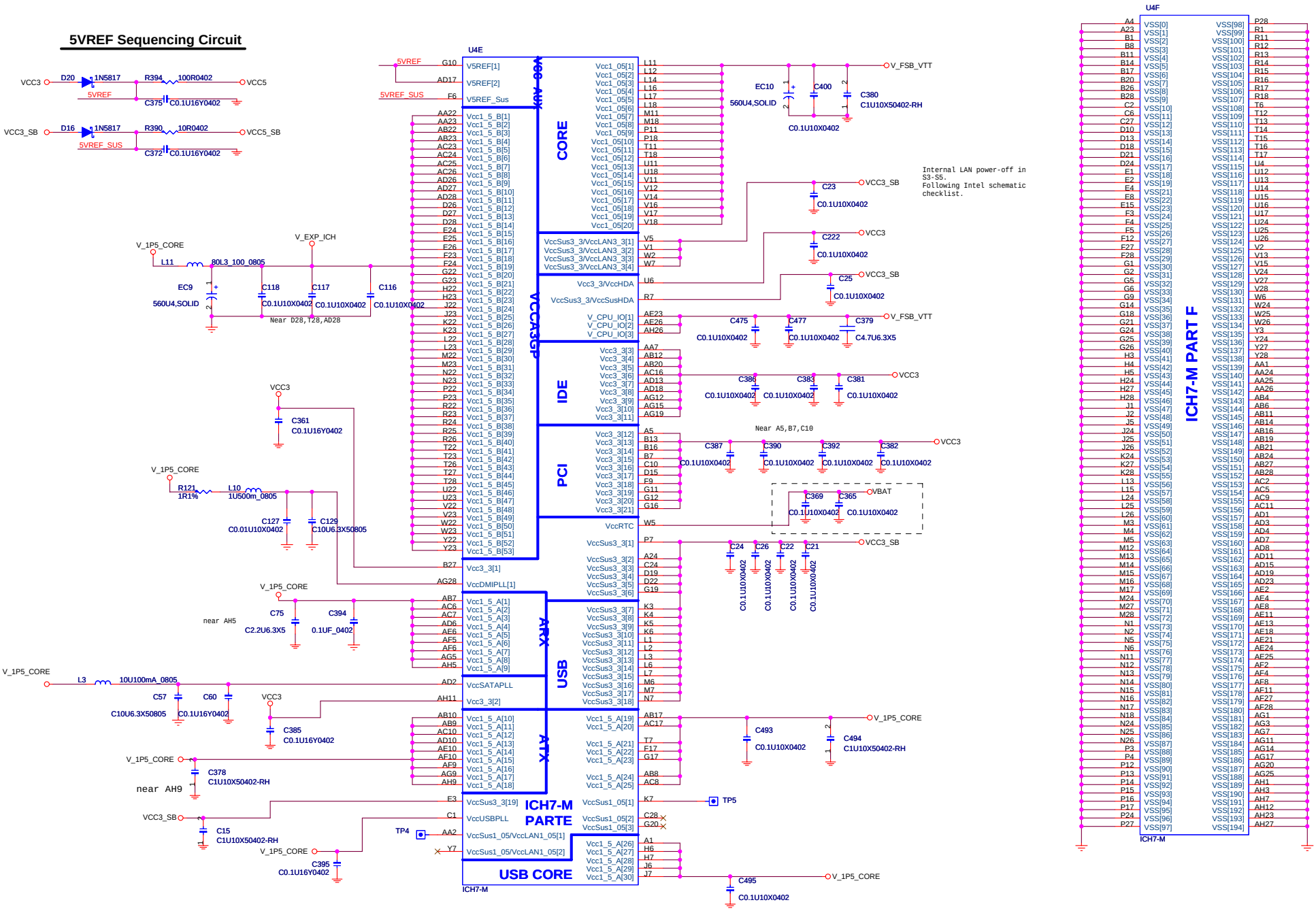


MICRO-STAR INt'L CO. , LTD.		
Title: GMCH5 - Strap / GND		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 11 of 38	



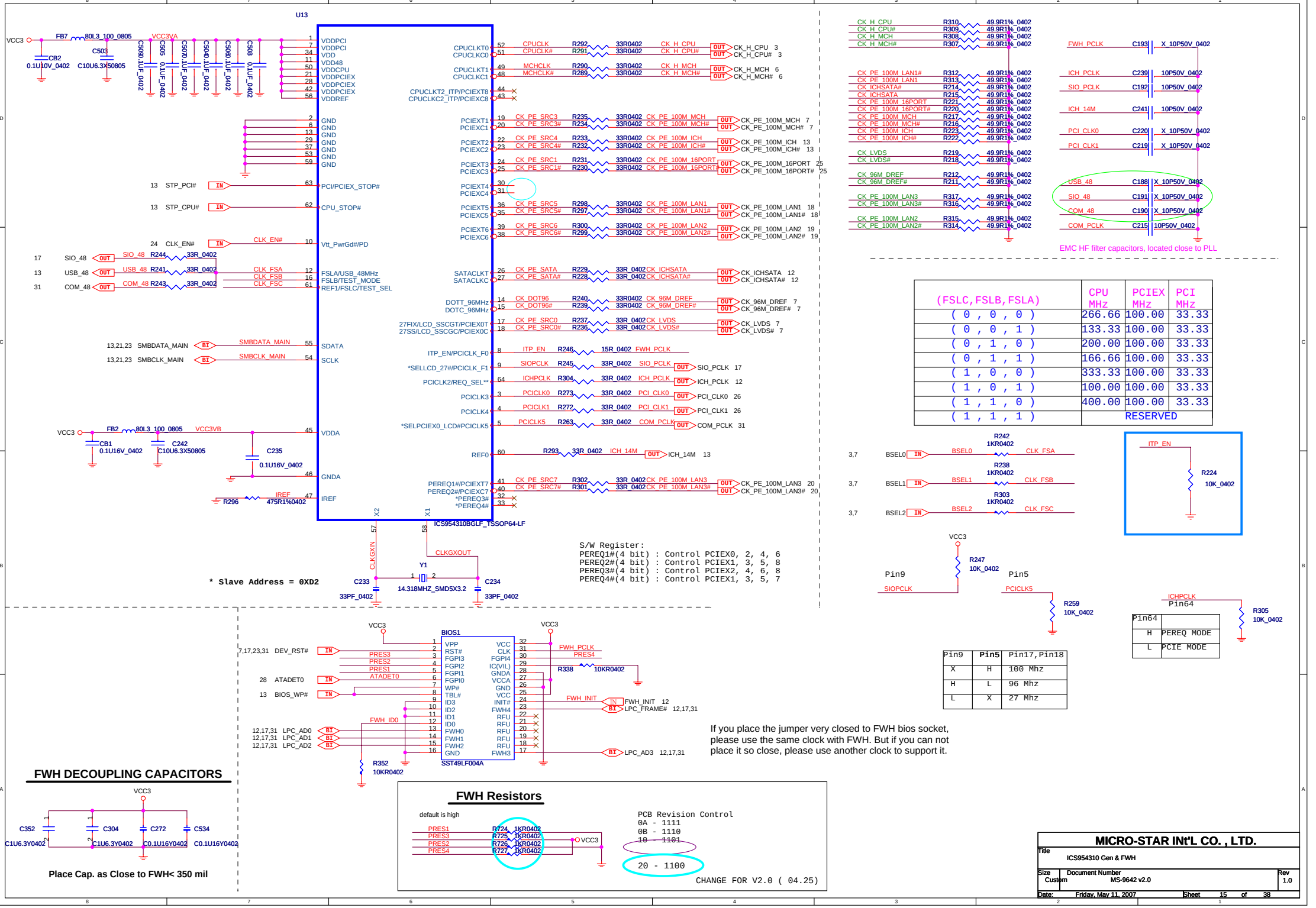
MICRO-STAR INt'L CO. , LTD.	
Title	ICH7M- CPU/IDE/Azalia
Size: Custom	Document Number: MS-9642 v2.0
Rev	1.0
Date: Wednesday, May 09, 2007	Sheet 12 of 38


U4C
SMB
SATA GPIO
Clocks
Power MGT
SYS GPIO
GPIO
ICH7-M PARTC
ICH7-M
SMBCLK_RESUME
SMBDATA_RESUME
LINK_ALERT#
SM_LINK0
SM_LINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
BM_BUSY#
SMB_ALERT#
STP_PCI#
STP_CPU#
PM_CLKRUN#
AUXGPIO_DIR1
AUXGPIO_DIR2
WAKE#
SERIRQ
THERM#
VRM_GD
SIO_OVT#
BIOS_WP#
GPIO8
GPIO6
GPIO7
GPIO[0:15] --> SMI
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/STAT3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35/STATCLKREQ#
GPIO38
GPIO39
AMP_EN
AMP_GAIN0
AMP_GAIN1
ICH_14M
USB_48
R74 0R0402
R80 X_0R0402
R74 STUFF,R80 POP RESERVED (04.25)
PWRGD
DPRSLPVR
BATTLOW#
PWRBTN#
ICH7_LAN_RST#
RSMRST_SB#
LAN1_EN
LAN2_EN
LAN3_EN
SIO_PME#
GPIO14
GPIO15
TP8
AUXGPIO_OE#
LAN_RST# connect to PLTRST#.
Follow Intel schematic
checklist
U4D
PCI-Express
Direct Media Interface (DMI
USB
SPI
ICH7-M PARTD
ICH7-M
PCIE_RN1
PCIE_RP1
PCIE_TN1
PCIE_TP1
PCIE_RN2
PCIE_RP2
PCIE_TN2
PCIE_TP2
PCIE_RN3
PCIE_RP3
PCIE_TN3
PCIE_TP3
C0.1U10X0402
PCIE_TN1_C
PCIE_TP1_C
PCIE_TN2_C
PCIE_TP2_C
PCIE_TN3_C
PCIE_TP3_C
C125
C126
C123
C124
C121
C122
PERn1
PERp1
PETn1
PETp1
PERn2
PERp2
PETn2
PETp2
PERn3
PERp3
PETn3
PETp3
PERn4
PERp4
PETn4
PETp4
PERn5
PERp5
PETn5
PETp5
PERn6
PERp6
PETn6
PETp6
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMITXN0
DMITXP0
DMIRXN0
DMIRXP0
DMITXN1
DMITXP1
DMIRXN1
DMIRXP1
DMITXN2
DMITXP2
DMIRXN2
DMIRXP2
DMITXN3
DMITXP3
DMIRXN3
DMIRXP3
<500mils
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
R81 24.9R1%0402
V_1P5_CORE
CK_PE_100M_ICH#
CK_PE_100M_ICH
SPI_CLK
SPI_CS#
SPI_ARB
SPI_MOSI
SPI_MISO
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USB0-
USB0+
USB1-
USB1+
USB2-
USB2+
USB3-
USB3+
USBRBIAS#
USBRBIAS
USB_BIAS R16 22.6R1%_0402
USB_BIAS < 500mil
OC#1
OC0#
OC1#
OC2#
OC3#
OC4#
OC5# / GPIO29
OC6# / GPIO30
OC7# / GPIO31
R17 10KR0402
R18 10KR0402
VCC3_SB
PM_CLKRUN#
SERIRQ
THERM#
SIO_OVT#
RN6
8P4R-8.2KR_0402
VCC3
BIOS_WP# R404 10KR0402
STP_PCI# R408 X_10KR0402
STP_CPU# R416 X_10KR0402
SPKR R51 X_10K_0402
Reserved for No Reboot
SMB Pull-up Resistor
RI#
LINK_ALERT#
SM_LINK0
SM_LINK1
RN8
8P4R-8.2KR_0402
GPIO Strapping Pull-up Resistor
SMB_ALERT#
SIO_PME#
BATTLOW#
LAN2_EN
RN5
8P4R-8.2KR_0402
GPIO8
LAN1_EN
LAN3_EN
GPIO14
RN3
8P4R-8.2KR_0402
WAKE# R48 1KR0402
GPIO15 R67 10KR0402
PWRGD R383 10KR0402
ADD
VCC5_SB
R379 4.7KR0402
RSMRST#
R384 X_10KR0402
Modify from Intel suggestion 0509'06 1A
R697 4.7KR0402
Q54
P-PMBS3906_SOT23-RH
ICH7_LAN_RST# 0R0402 R380
R698 10KR0402
RSMRST# RSMRST_SB# R699 X_0R0402
D25
BAV99-7-F_SOT23-LF
D26
BAV99-7-F_SOT23-LF
R700 2.2K/4
SM BUS ISOLATION
+12V
R155 10KR0402
SMB_PWROK
C152
C0.1U16Y0402
R157 1KR0402
R156 1KR0402
Q18
Q19
N-2N7002_SOT23
SMBDATA_RESUME
SMBDATA_MAIN
SMBCLK_RESUME
SMBCLK_MAIN
(To: PCI,PCI-Express,ICH7)
(To: CLK,DIMM,MS-7,HW_Monitor)
(To: PCI,PCI-Express,ICH7)
(To: CLK,DIMM,MS-7, HW_Monitor)
SMBCLK_MAIN R180 4.7KR0402
SMBDATA_MAIN R179 4.7KR0402
SMBCLK_RESUME R63 4.7KR0402
SMBDATA_RESUME R68 4.7KR0402
MICRO-STAR INt'L CO. , LTD.
Title
ICH7M - GPIO,USB,PCIE
Size
Custom
Document Number
MS-9642 v2.0
Rev
1.0
Date: Tuesday, May 08, 2007
Sheet 13 of 38



MICRO-STAR INt'L CO. , LTD.

Title	ICH7M - Power	
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 14 of 38	


U13
ICS954310BGLF_TSSOP64-LF
* Slave Address = 0XD2
S/W Register:
PEREQ1#(4 bit) : Control PCIEX0, 2, 4, 6
PEREQ2#(4 bit) : Control PCIEX1, 3, 5, 8
PEREQ3#(4 bit) : Control PCIEX2, 4, 6, 8
PEREQ4#(4 bit) : Control PCIEX1, 3, 5, 7
EMC HF filter capacitors, located close to PLL
(FSLC,FSLB,FSLA) | CPU MHz | PCIEX MHz | PCI MHz
(0 , 0 , 0) | 266.66 | 100.00 | 33.33
(0 , 0 , 1) | 133.33 | 100.00 | 33.33
(0 , 1 , 0) | 200.00 | 100.00 | 33.33
(0 , 1 , 1) | 166.66 | 100.00 | 33.33
(1 , 0 , 0) | 333.33 | 100.00 | 33.33
(1 , 0 , 1) | 100.00 | 100.00 | 33.33
(1 , 1 , 0) | 400.00 | 100.00 | 33.33
(1 , 1 , 1) | RESERVED
Pin9 | Pin5 | Pin17,Pin18
X | H | 100 Mhz
H | L | 96 Mhz
L | X | 27 Mhz
Pin64 |
H | PEREQ MODE
L | PCIE MODE
BIOS1
SST49LF004A
If you place the jumper very closed to FWH bios socket, please use the same clock with FWH. But if you can not place it so close, please use another clock to support it.
FWH DECOUPLING CAPACITORS
Place Cap. as Close to FWH< 350 mil
FWH Resistors
default is high
PCB Revision Control
0A - 1111
0B - 1110
10 - 1101
20 - 1100
CHANGE FOR V2.0 (04.25)
MICRO-STAR INt'L CO. , LTD.
Title
ICS954310 Gen & FWH
Size
Custom
Document Number
MS-9642 v2.0
Rev
1.0
Date:
Friday, May 11, 2007
Sheet
15
of
38

Realtek ALC888 CODEC

ADD FOR EMI:
FB12.FB13.FB14.
FB15.FB16.FB17.
FB18.FB19.FB20.
FB21.FB24.FB25.
07.17.06'

Trace Width 20mils.

FOR ALC883

REALTEK

ALC888

ALC888GR

AUDIO CODE REGULATORS

U15 YLT1087S-0.8A

SOT223

Modify audio power circuit 2005.10.3

EMI Solution

add in 0427

Front Audio Connector

CHANGE AVDD5 TO VCC5 IN V2.0 (04.25)

JAUD1

H2X7_black

JAMP1

H1X4_black-RH

ADD PIN13.PIN14 FOR 7.1CH:
IT NEEDS TO APPLY 2X9 PIN HEADER FOR ROHS
NEW-PN AND NEW FOOTPRINT
07.13.06'
2X9 CHANGE TO ONE 2X7 AND ONE 1X4
2X7 PIN HEADER FOR ROHS SHOULD APPLY
NEW-PN AND NEW FOOTPRINT
07.17.06'

R320.R322.R318.R324
NON-POP
07.19.06'

Rear Audio Jack

AUDIO1

L_OUT_IN_MIC

R281.R283.R287 Close to codec

TPA3005D2

As close as chip possible

GAIN1	GAIN0	AV(dB)
0	0	15.3
0	1	21.2
1	0	27.2
1	1	31.8

MICRO-STAR INt'L CO. , LTD.

Title: Audio - ALC888

Size: Custom | Document Number: MS-9642 v2.0 | Rev: 1.0

Date: Wednesday, May 09, 2007 | Sheet 16 of 38

COM1

SERIAL PORT 1

U1 GD75232_TSSOP20

CONN1B CONN-VGA_COM-3.18mm

CN2 8P4C-220P50N

CN1 8P4C-220P50N

PARALLAL PORT

JLPT1 BH2X13_black-2pitch -15u-in

CN8 8P4C-220P50N

CN9 8P4C-220P50N

CN10 8P4C-220P50N

CN7 8P4C-220P50N

Use 3 pin PWM FAN

LPC I/O STRAPPING RESISTOR

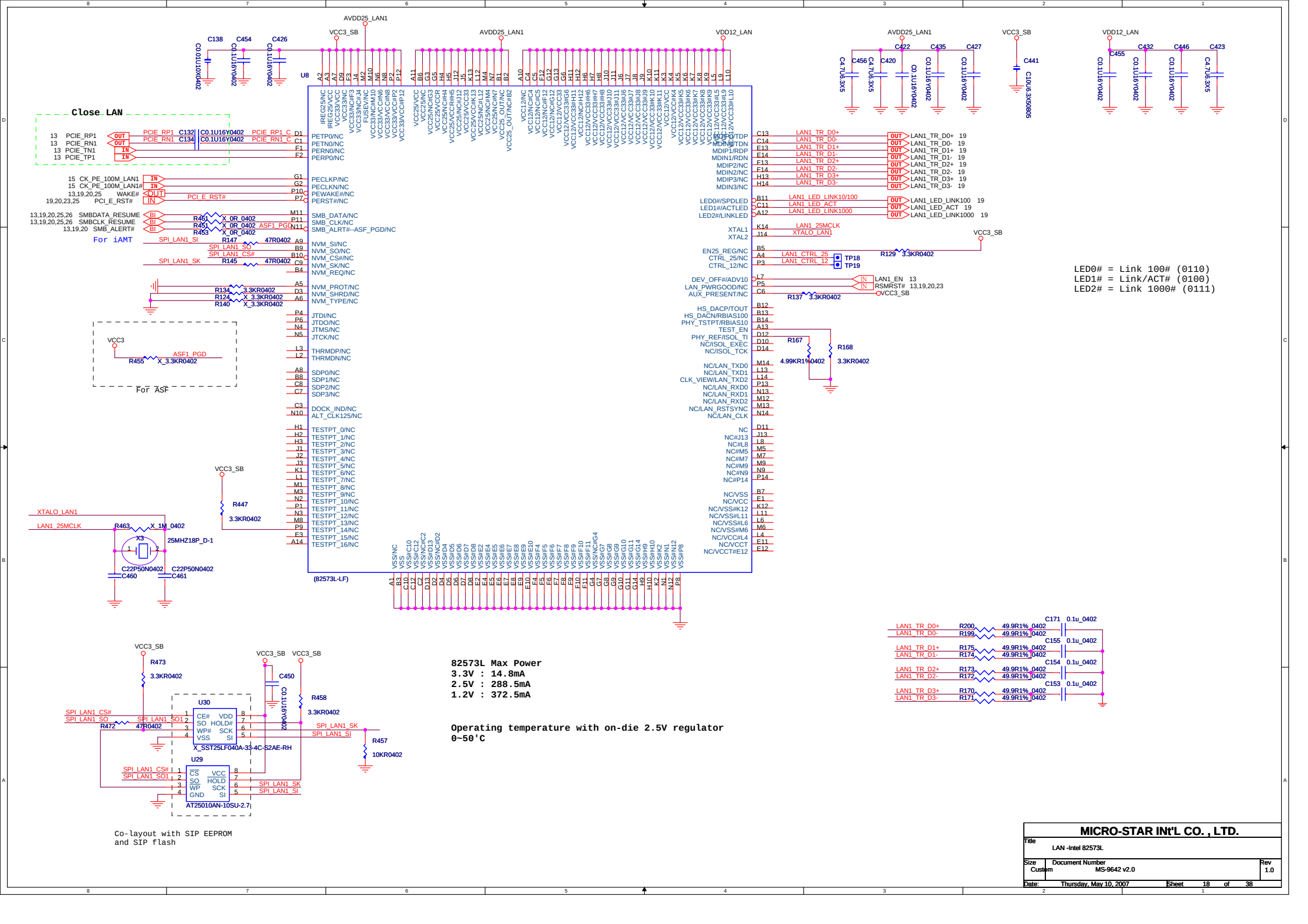
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: Disable SPI	H: Enable SPI
EN_VRM10	L: TTL Level	L: VRM10 Level

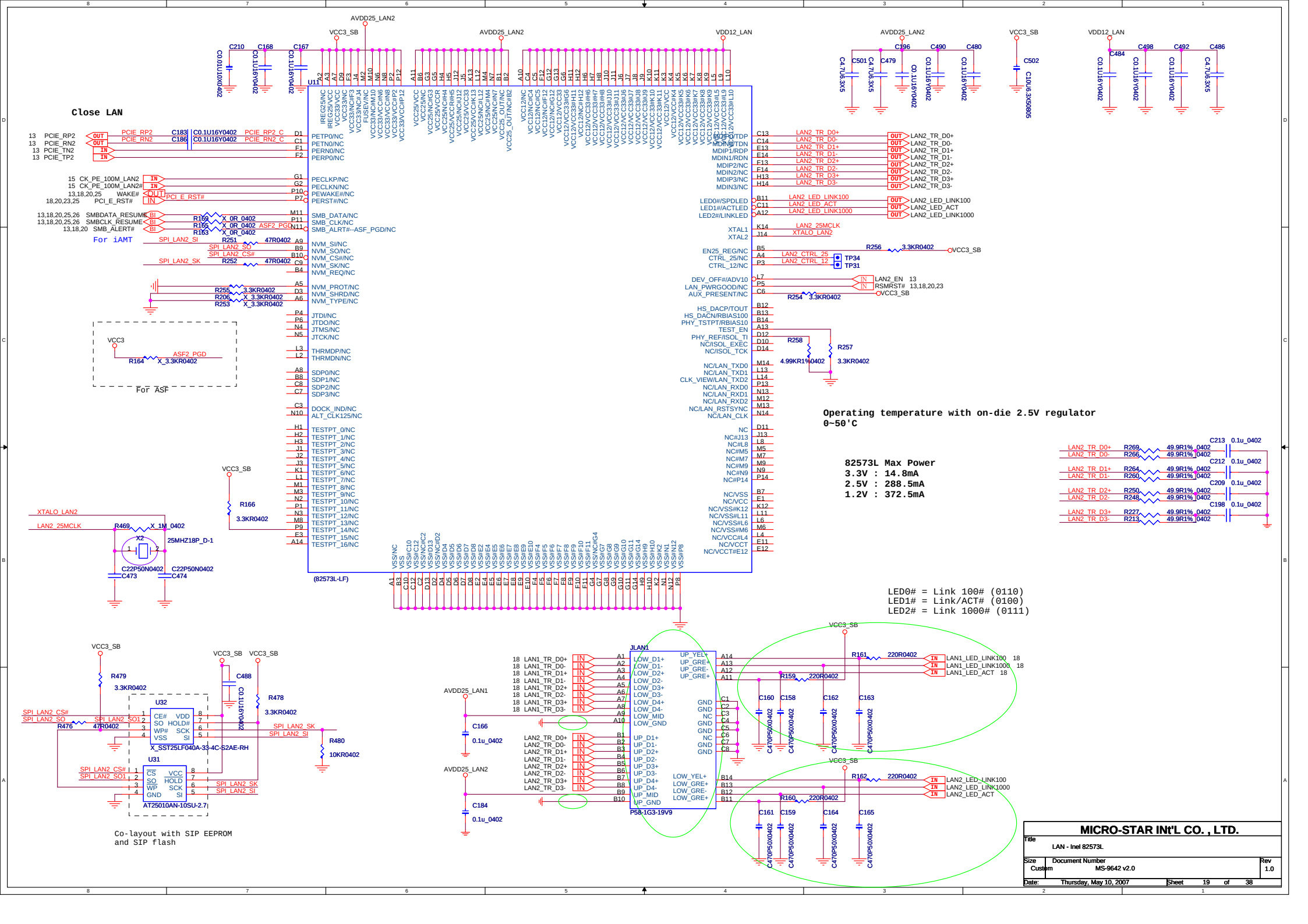
Chasis Intrusion

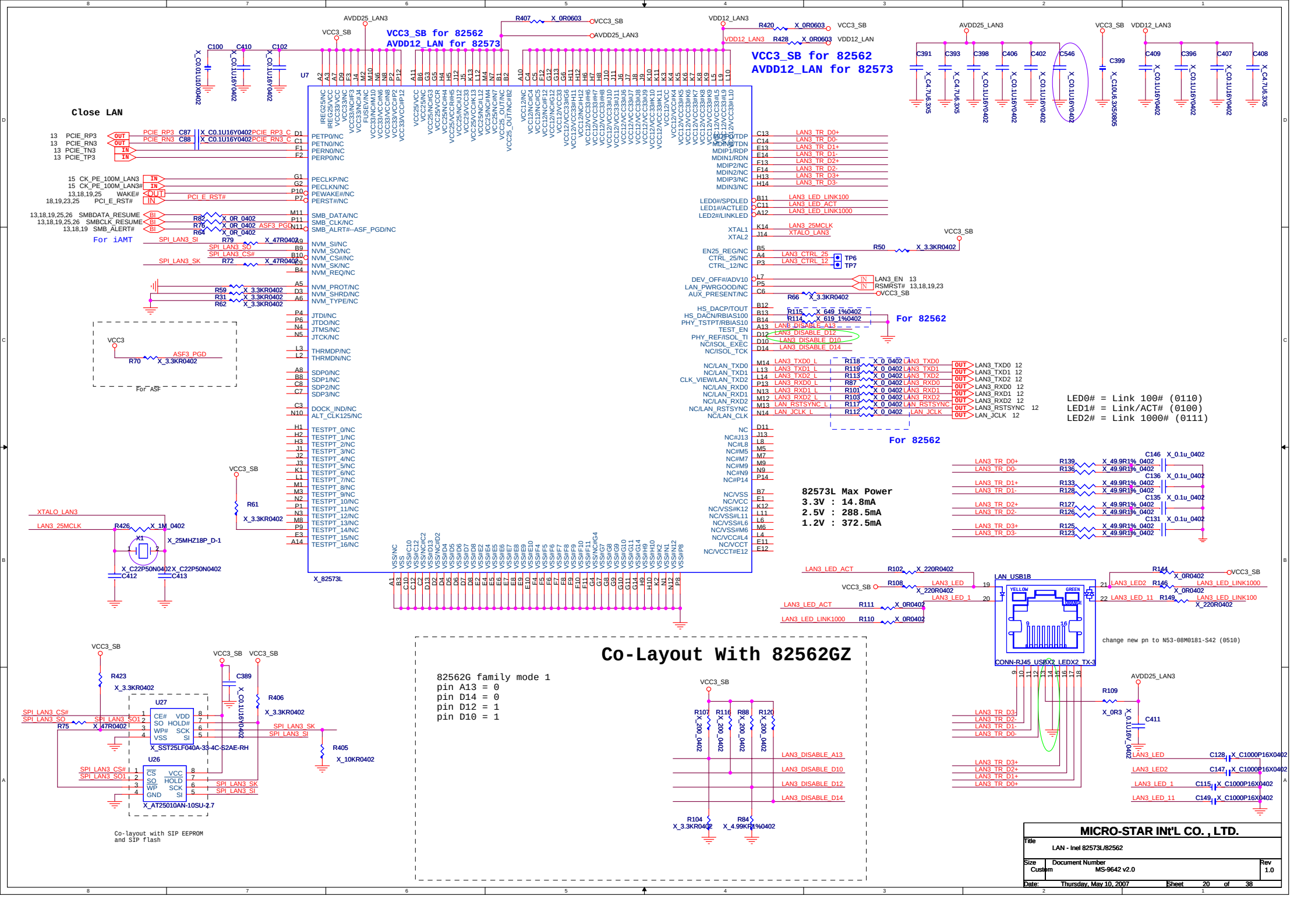
PS2 KEYBOARD & MOUSE CONNECTOR

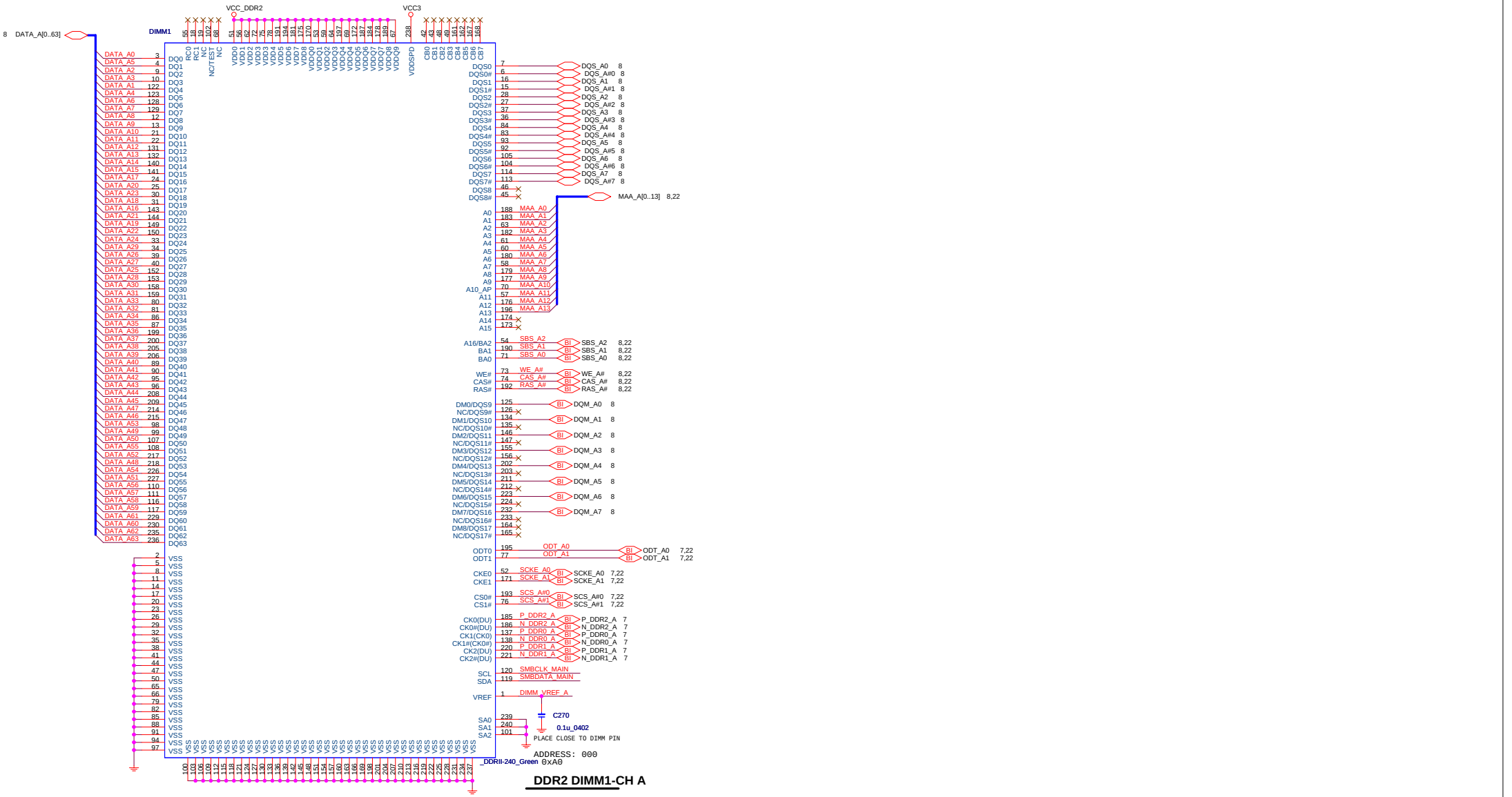
NOTE: LOCATE CLOSE STATUS PANEL

Title	LPC - W83627THF
Company	MICRO-STAR INt'L CO. , LTD.
Size	Custom
Document Number	MS-9642 v2.0
Rev	1.0
Date:	Wednesday, May 09, 2007
Sheet	17 of 38


Close LAN
For iAMT
For ASF
U8
(82573L-LF)
U30
X_SST25LF040A-33-4C-S2AE-RH
U29
AT25010AN-10SU-2.7
X3
25MHZ18P_D-1
LED0# = Link 100# (0110)
LED1# = Link/ACT# (0100)
LED2# = Link 1000# (0111)
82573L Max Power
3.3V : 14.8mA
2.5V : 288.5mA
1.2V : 372.5mA
Operating temperature with on-die 2.5V regulator
0~50'C
Co-layout with SIP EEPROM
and SIP flash
MICRO-STAR INt'L CO. , LTD.
LAN -Intel 82573L
MS-9642 v2.0
Thursday, May 10, 2007

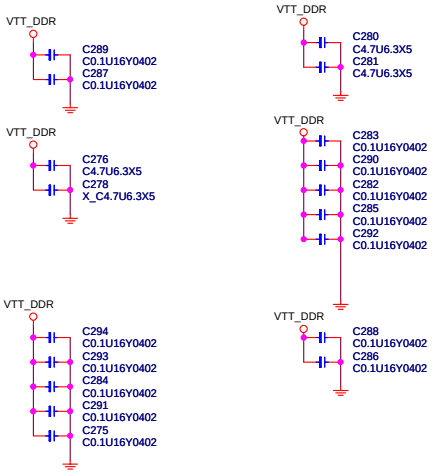

Close LAN
For iAMT
For ASF
(82573L-LF)
Operating temperature with on-die 2.5V regulator
0~50'C
82573L Max Power
3.3V : 14.8mA
2.5V : 288.5mA
1.2V : 372.5mA
LED0# = Link 100# (0110)
LED1# = Link/ACT# (0100)
LED2# = Link 1000# (0111)
Co-layout with SIP EEPROM
and SIP flash
X_SST25LF040A-33-4C-S2AE-RH
AT25010AN-10SU-2.7
P58-1G3-19V9
MICRO-STAR INt'L CO. , LTD.
LAN - Inel 82573L
MS-9642 v2.0
Thursday, May 10, 2007

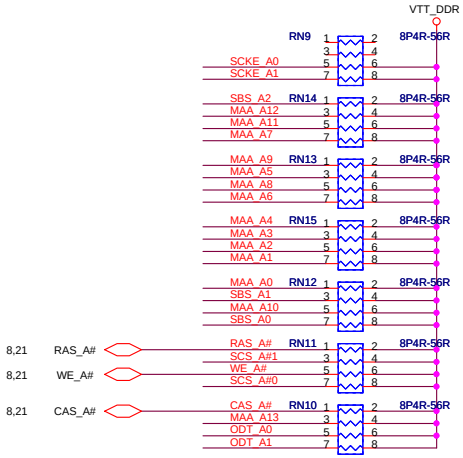

VCC3_SB for 82562
AVDD12_LAN for 82573
VCC3_SB for 82562
AVDD12_LAN for 82573
Close LAN
For iAMT
For ASF
For 82562
For 82562
82573L Max Power
3.3V : 14.8mA
2.5V : 288.5mA
1.2V : 372.5mA
LED0# = Link 100# (0110)
LED1# = Link/ACT# (0100)
LED2# = Link 1000# (0111)
Co-Layout With 82562GZ
82562G family mode 1
pin A13 = 0
pin D14 = 0
pin D12 = 1
pin D10 = 1
Co-layout with SIP EEPROM and SIP flash
change new pn to N53-08M0181-S42 (0510)
MICRO-STAR INt'L CO. , LTD.
LAN - Inel 82573L/82562
Custom
MS-9642 v2.0
Rev 1.0
Thursday, May 10, 2007
Sheet 20 of 38

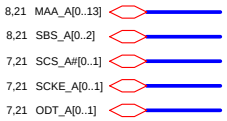


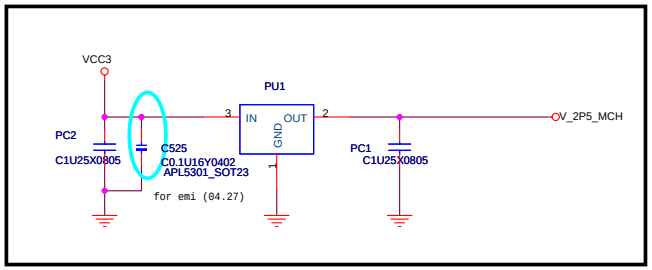
MICRO-STAR INT'L CO. , LTD.		
Title: DDR2 DIMM1		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 21 of 38	

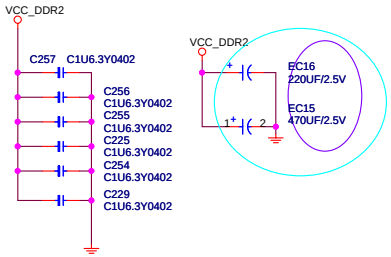
CHANNEL A V_SM_VTT DECOULPING CAPS

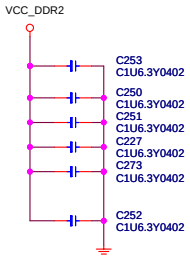












MICRO-STAR INt'L CO. , LTD.		
Title: DDR2 Terminator		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Wednesday, May 09, 2007	Sheet 22 of 38	

ACPI Controller

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

Connect to GND 2005.3.16

DDR AND DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

THIS PIN IS OPEN DRAIN OUTPUT

CHARGE PUMP VOLTAGE OUTPUT

Irripple=20*0.6*0.8/1=9.6A
2.22*3*1.7=11.322A>9.6A

High-side MOS
AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-005

Irms(MAX) of VCC_DDR=20A

C265 change to no pop. 2006.5.26

CONNECT TO CHOKE OUTPUT

CLOSE TO DEVICE FB

R267 R275 CHANGE TO 2K 5/17/06'

Low-side MOS
change to (RoHS):
D03-4119N00-005
05/19/06'

L/DCR=R*C
Rcsp >= (0.22uH/1.9m ohm)/1uF
>=115 ohm=R849

ocp* DCR_max = Ix*Rcsn
Rcsn >= (15amp * 2.5 m ohm)/80uA
>= 468 ohm=R851

V_1P5_CORE

Wide Trace

Close to MS11

5V DUAL Power

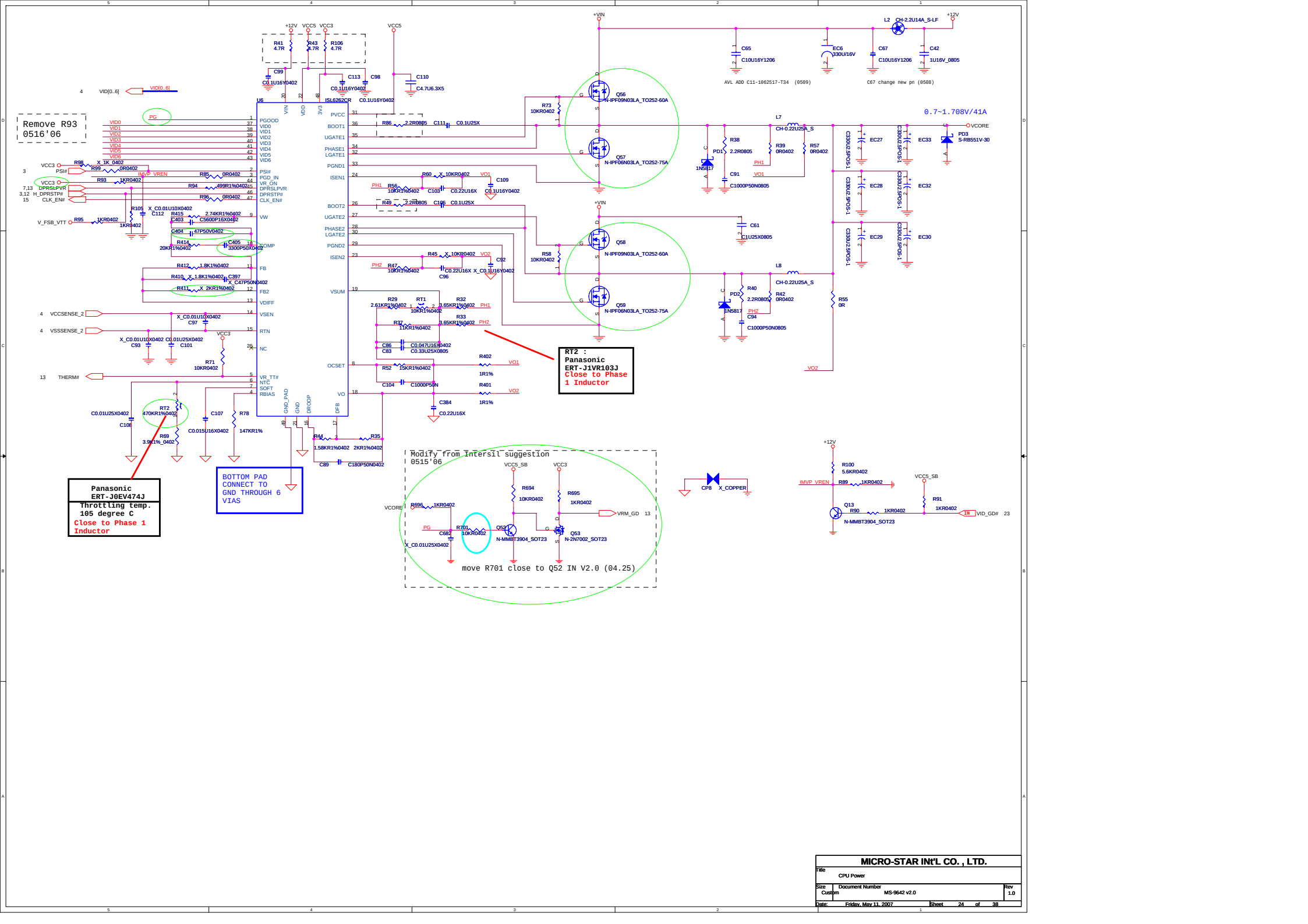
FRONT

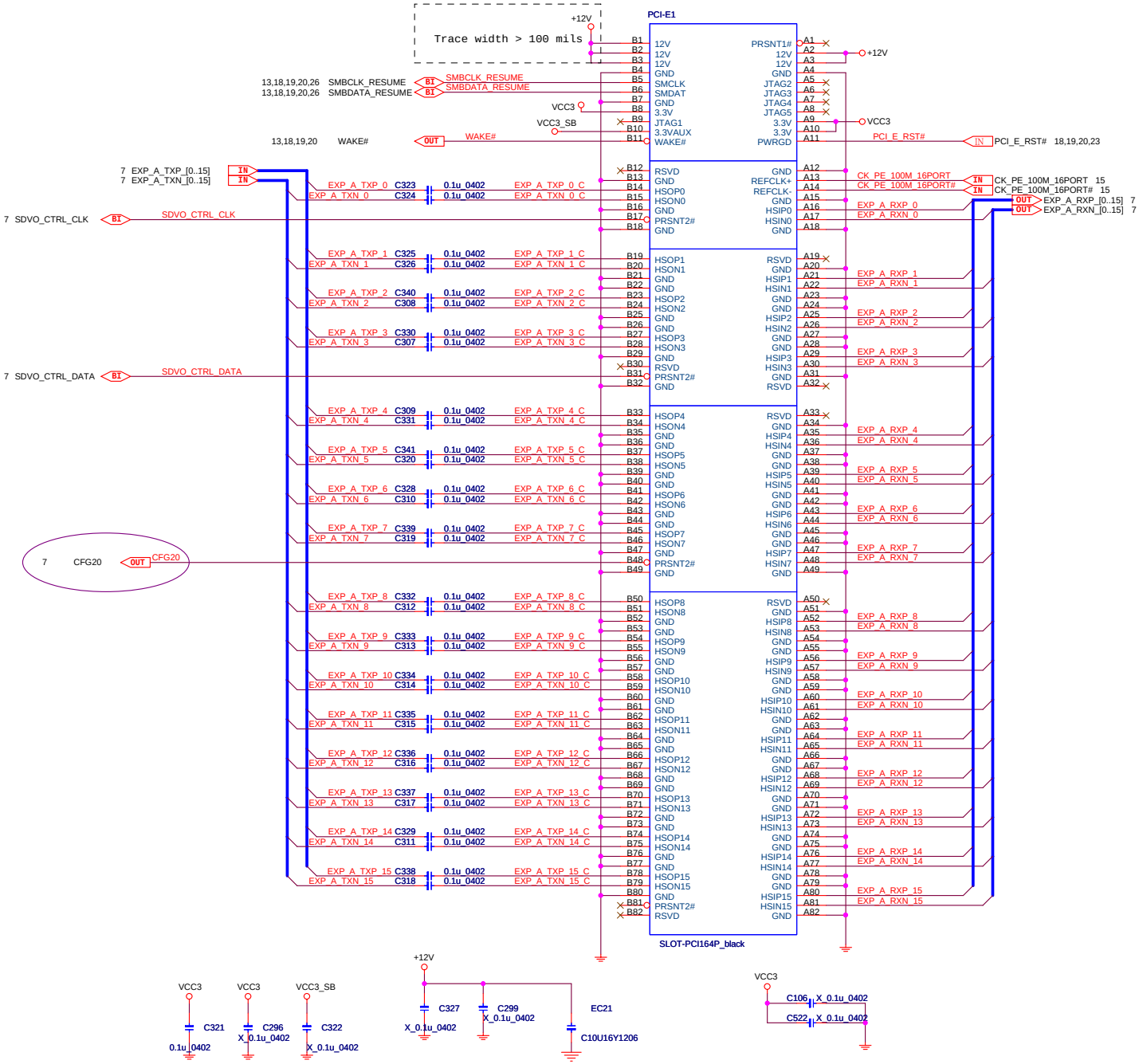
DDR VTT Power

CHANGE EC17.EC18.EC9.EC10 TO OS-CON BUT NOT CHANGE FOOTPRINT 07.18.06'

Max Power:
2.5V : 288.5mA*3 = 0.8A
1.2V : 372.5mA *3 = 1.12A
Power = 1.2 * (3.3-1.2) = 2.62W

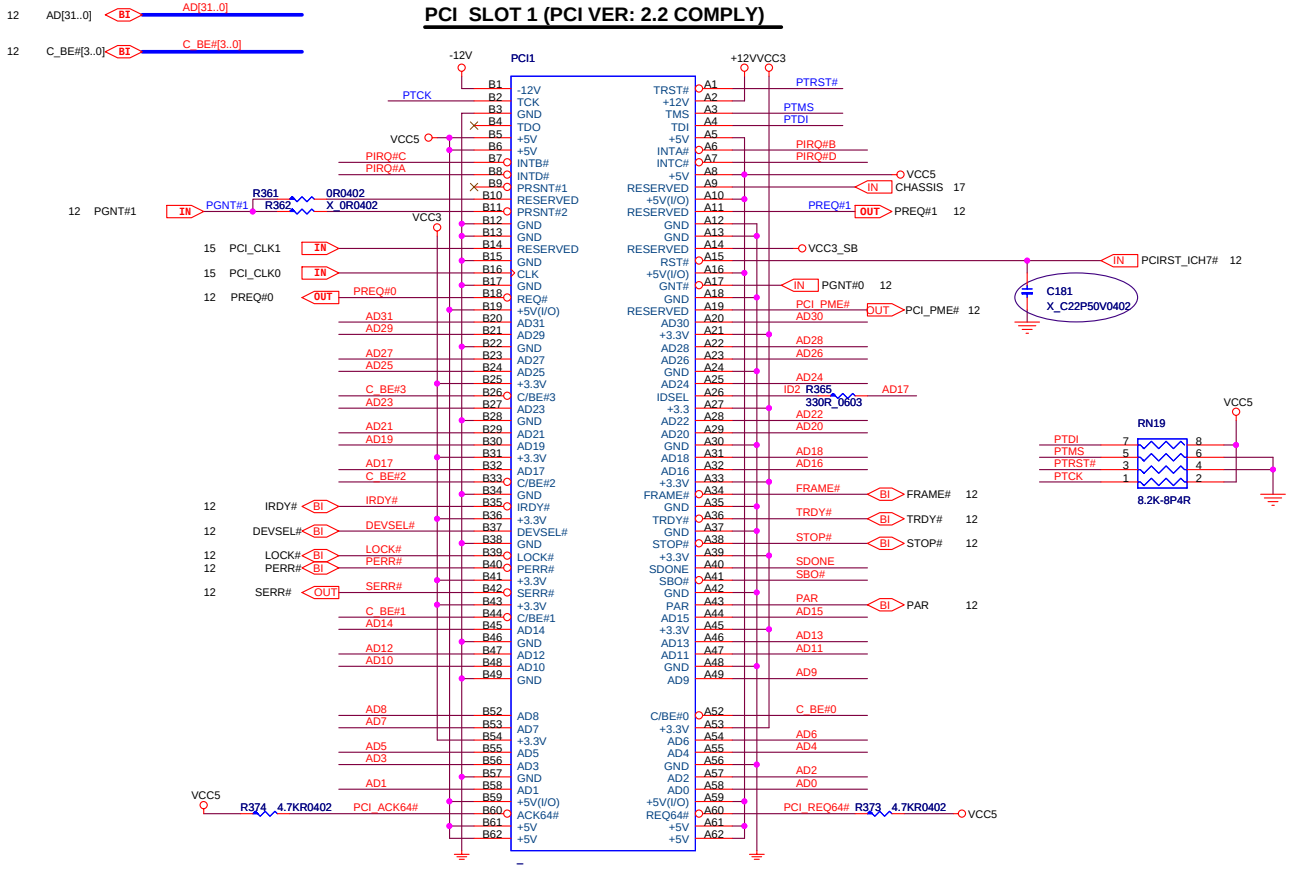
MICRO-STAR INt'L CO. , LTD.			
Title: MS7 - ACPI Controller			
Size: C	Document Number: MS-9642 v2.0		Rev: 1.0
Date: Thursday, May 10, 2007	Sheet 23 of 38		


Remove R93
0516'06
U6
ISL6262CR
0.7~1.708V/41A
VCORE
RT2 :
Panasonic
ERT-J1VR103J
Close to Phase
1 Inductor
Panasonic
ERT-J0EV474J
Throttling temp.
105 degree C
Close to Phase 1
Inductor
BOTTOM PAD
CONNECT TO
GND THROUGH 6
VIAS
Modify from Intersil suggestion
0515'06
move R701 close to Q52 IN V2.0 (04.25)
AVL ADD C11-1062517-T34 (0509)
C67 change new pn (0508)
MICRO-STAR INT'L CO. , LTD.
Title
CPU Power
Size
Custom
Document Number
MS-9642 v2.0
Rev
1.0
Date:
Friday, May 11, 2007
Sheet
24
of
38



MICRO-STAR INt'L CO. , LTD.		
Title: PCI Express 16 Port		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Wednesday, May 09, 2007	Sheet 25 of 38	

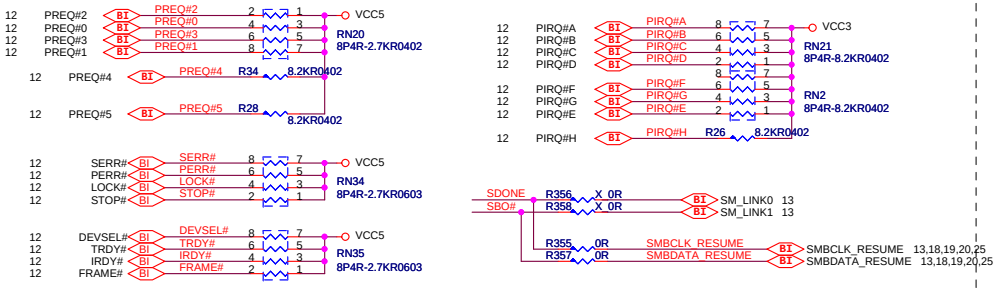
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



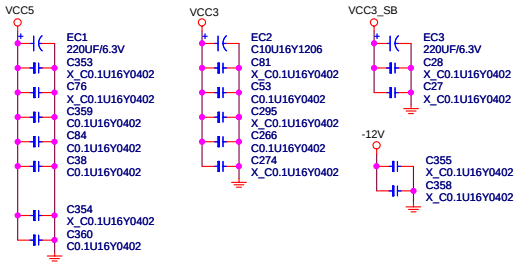
change the new PN in 2.0

IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

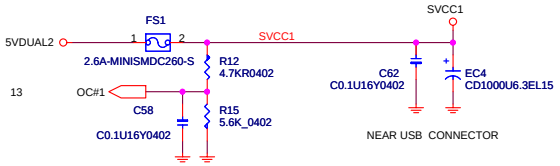


PCI SLOT DECOUPLING CAPACITORS



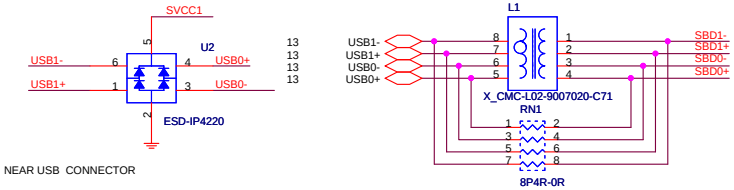
MICRO-STAR INt'L CO. , LTD.		
Title: PCI Slot		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Friday, May 11, 2007	Sheet 26 of 38	

POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)

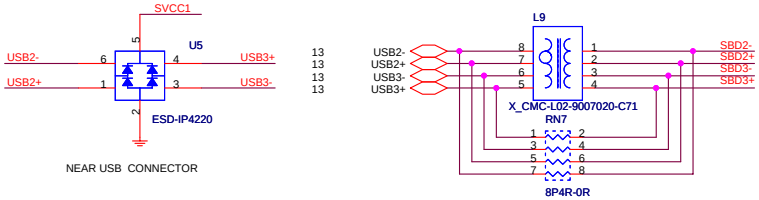


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

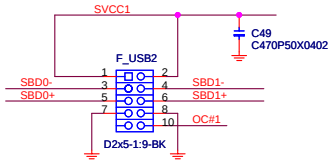
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

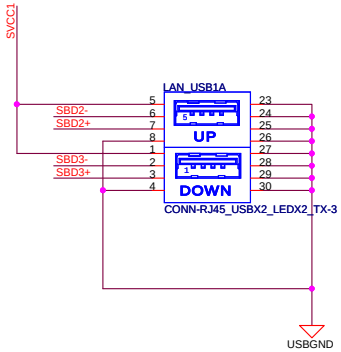


REAR PANEL USB CONNECTOR FOR USB PORT 2,3



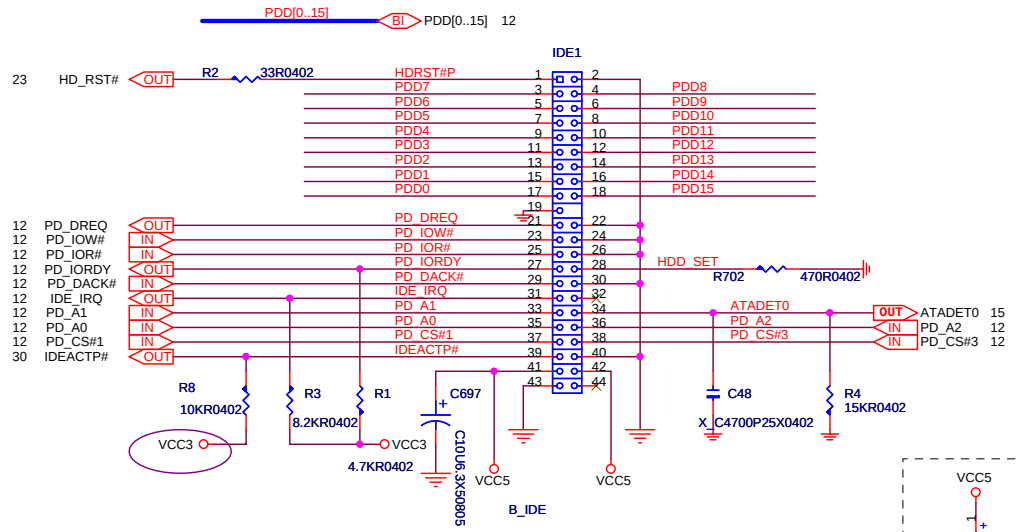
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

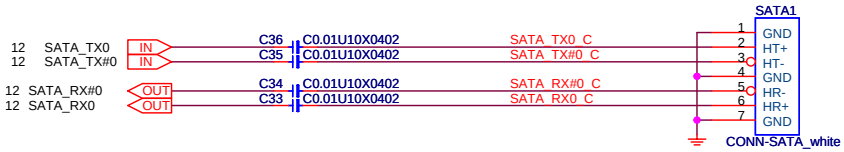


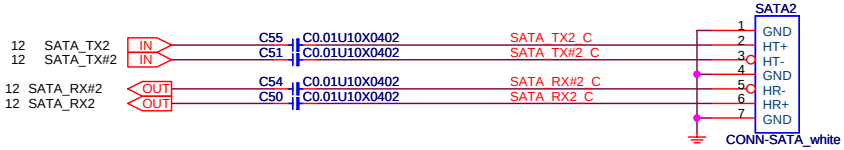


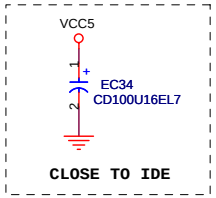
MICRO-STAR INt'L CO. , LTD.		
Title: USB Connector		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Thursday, May 10, 2007	Sheet 27 of 38	

44 Pin IDE Connectors



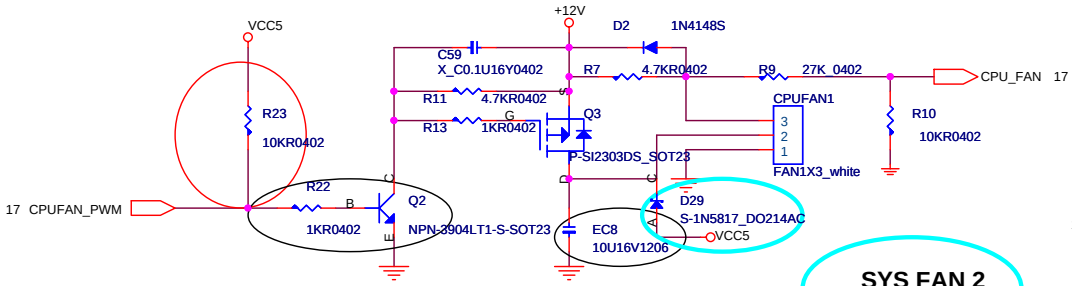






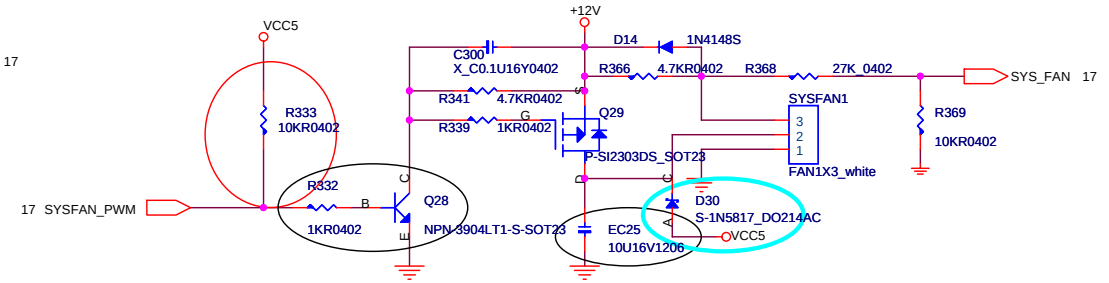
CPU FAN PWM MODE

Ver. C : Remove R23
Ver. H : Solder R23

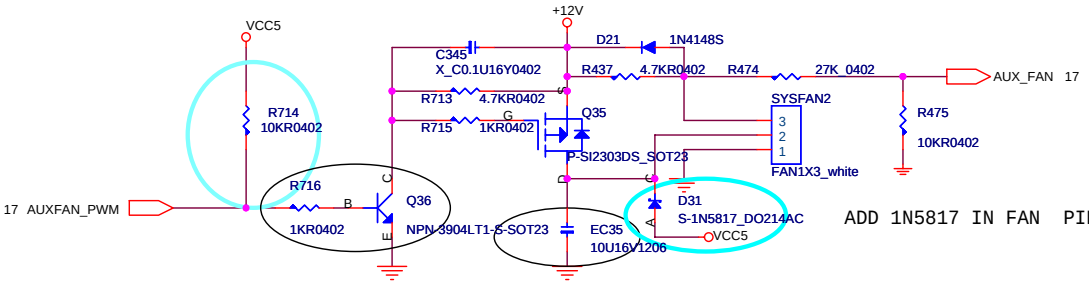


SYS FAN 1 PWM MODE

Ver. C : Remove R333
Ver. H : Solder R333



SYS FAN 2 PWM MODE

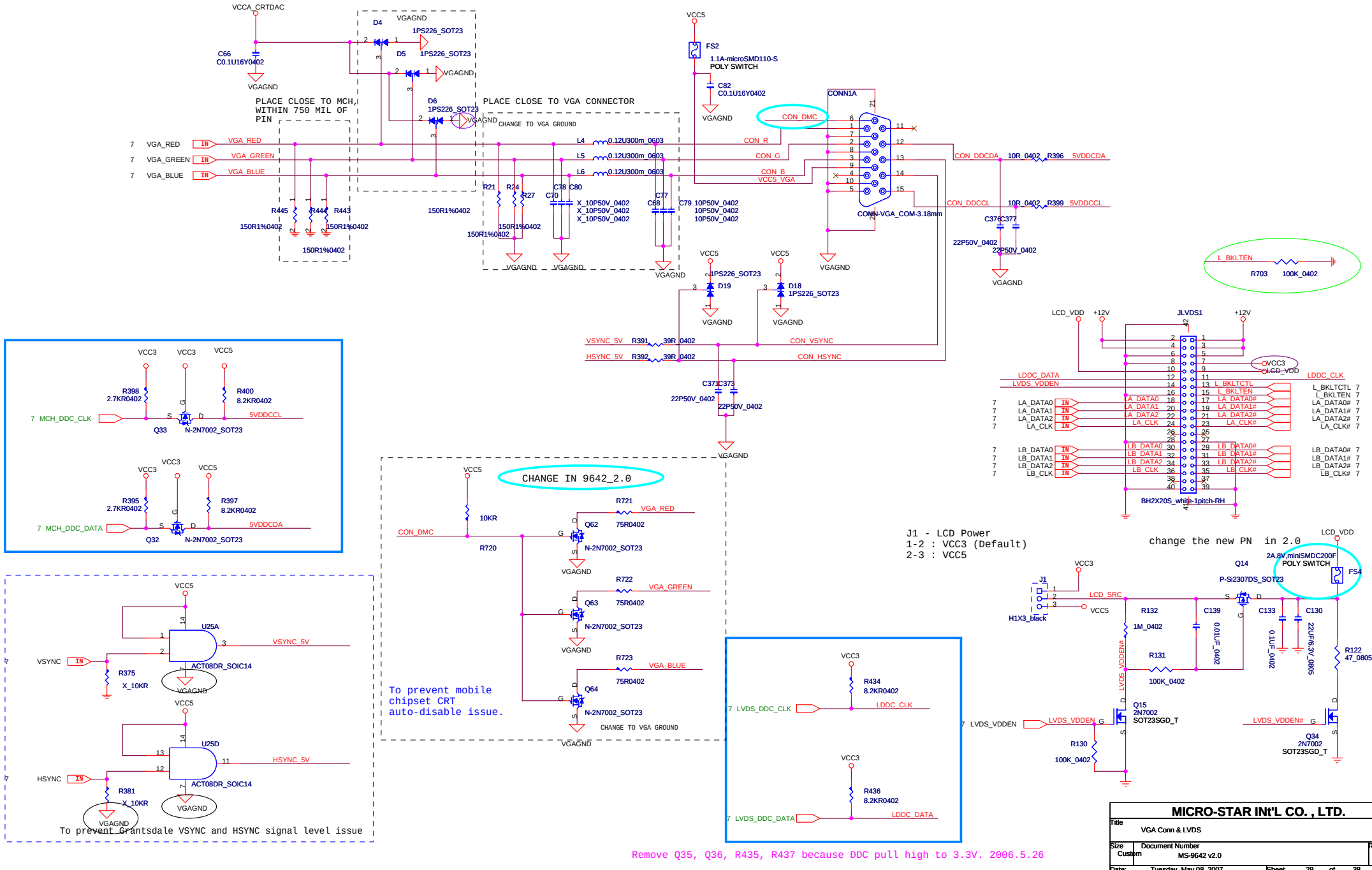


ADD 1N5817 IN FAN PIN 2(04.25)

MICRO-STAR INt'L CO. , LTD.		
Title: FAN & IDE Connectors		
Size: B	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 28 of 38	

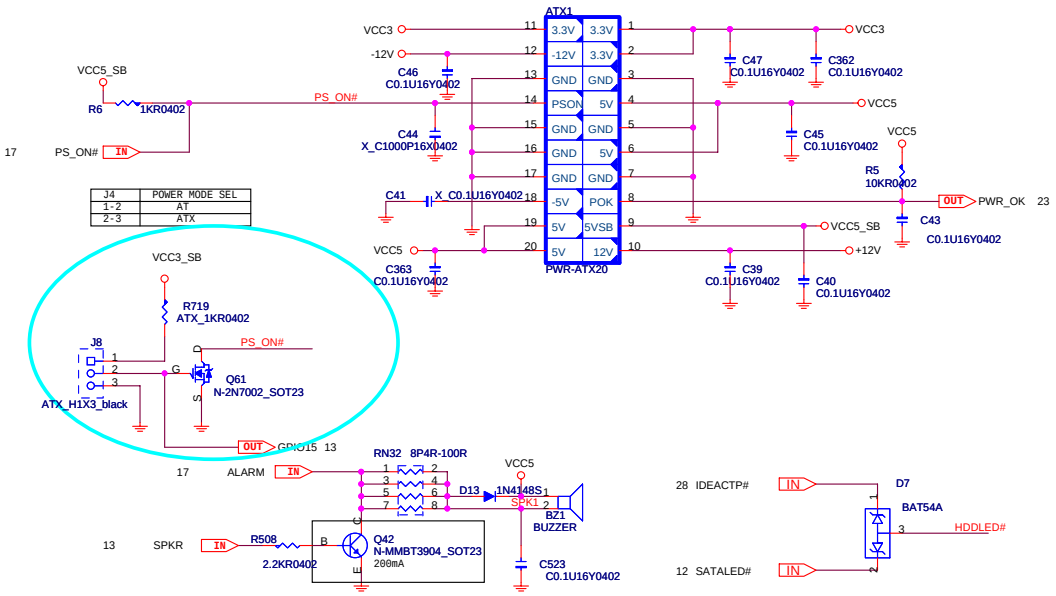
Video Connector

PLACE CLOSE TO MCH



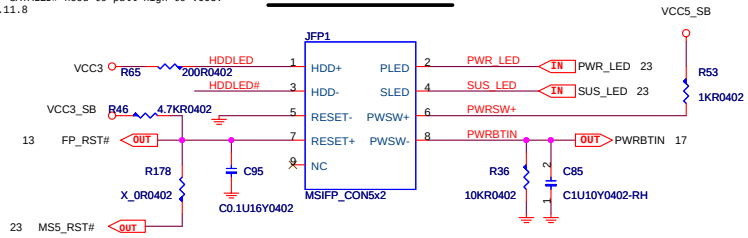
MICRO-STAR INt'L CO. , LTD.		
Title: VGA Conn & LVDS		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 29 of 38	

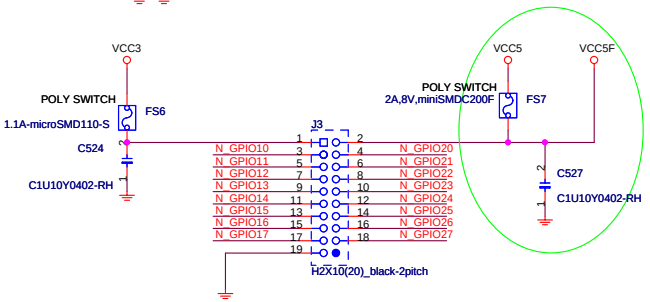
ATX Connector

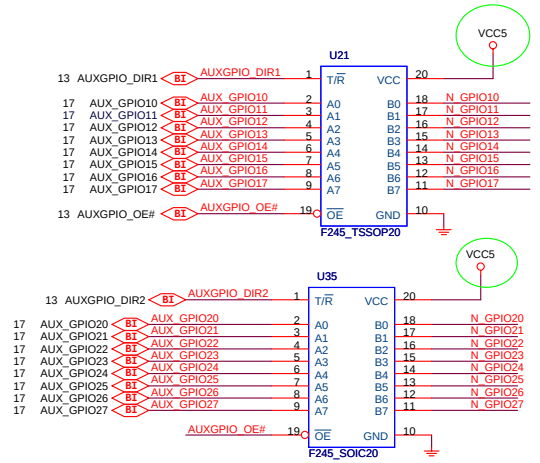


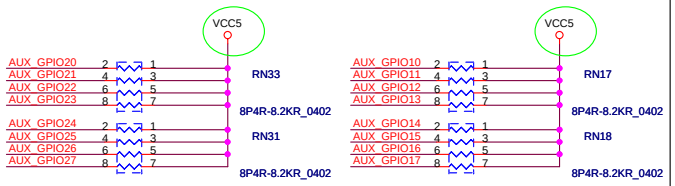
Changed HDD+ from VCC5 to VCC3 because ICH7 SATALED# need to pull high to VCC3. 2005.11.8

Intel Front Panel



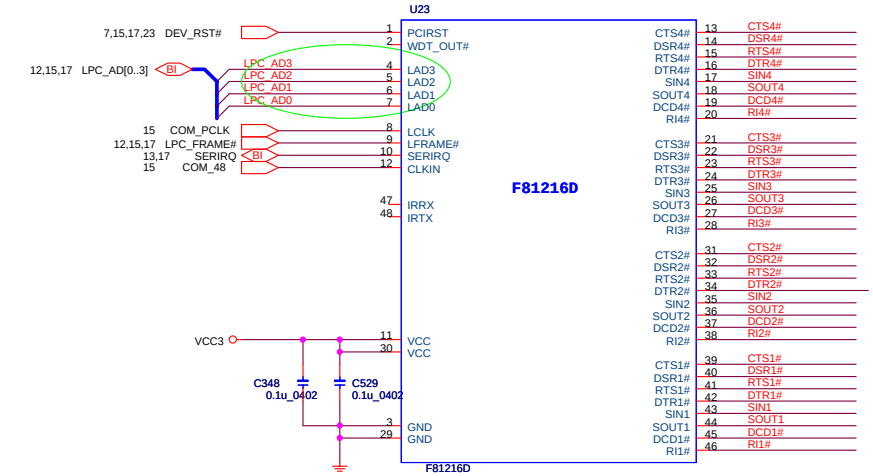


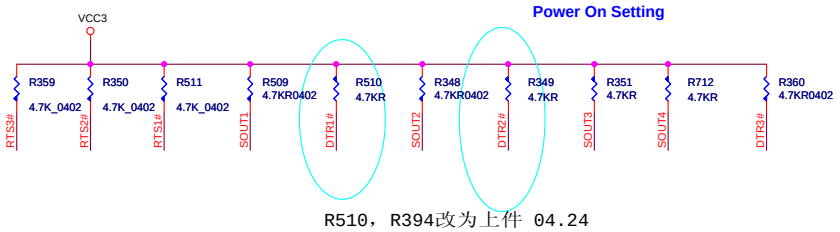




Title	ATX Connector & Front Panel
Size	Custom
Document Number	MS-9642 v2.0
Rev	1.0
Date:	Tuesday, May 08, 2007
Sheet	30 of 38

MICRO-STAR INt'L CO. , LTD.





R510，R394改为上件 04.24

RTS2#	RTS3#	RTS1#	Address	Entry Key
0	0	0	0x4E/0x4F	0x77
0	0	1	0x2E/0x2F	0x77
0	1	0	0x4E/0x4F	0xA0
0	1	1	0x2E/0x2F	0xA0
1	0	0	0x4E/0x4F	0x87
1	0	1	0x2E/0x2F	0x87
1	1	0	0x4E/0x4F	0x67
1	1	1	0x2E/0x2F	0x67

SOUT1 1 and DTR1# 0: UART 1 addr:0x3f8 irq3; SOUT1 0 and DTR1# 1: UART 1 addr:0x3e0 IRQ3; SOUT1 0 and DTR1# 0: UART 1 disabled.

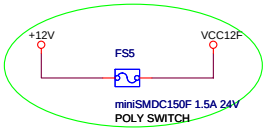
SOUT2 1 and DTR2# 0: UART 2 addr:0x2f8 irq4;SOUT2 0 and DTR2# 1 : UART 2 addr:0x2e0 IRQ4; SOUT2 0 and DTR2# 0: UART 2 disabled.

SOUT3 1: UART 3 addr:0x3e8 IRQ5; SOUT3 0:UART 3 disabled.

SOUT4 1: UART 4 addr:0x2e8 IRQ9; SOUT4 0:UART 4 disabled.

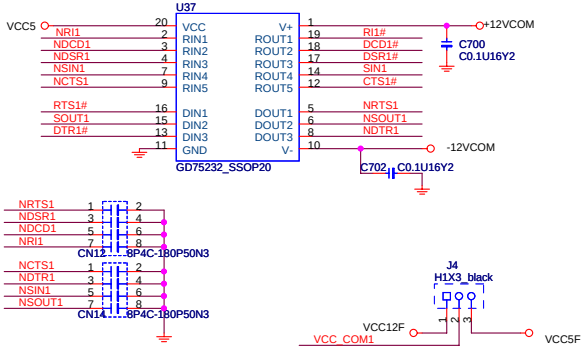
DTR3# 1: Watch Dog Timer enabled and setting to 10 second when the clock input is 24Mhz. If the clock input is 48Mhz , the timer is setting to 5 second. DTR3# 0 :disabled.

CHANGE THE NEW PN AND FOOTPRINT FOR COM PORT 2~5

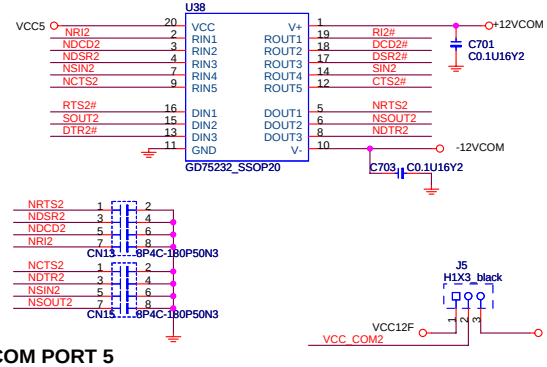


change the new PN and footprint in 2.0

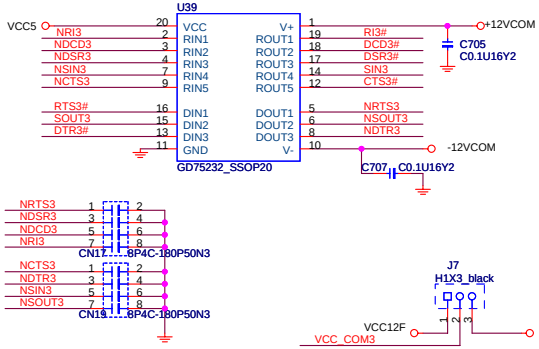
COM PORT 2



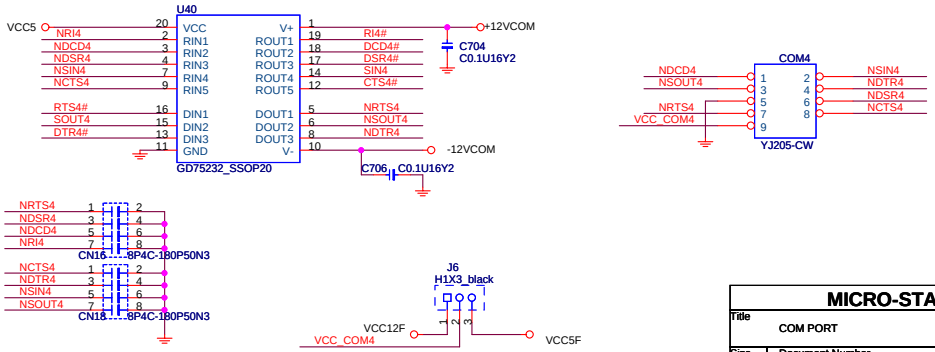
COM PORT 3



COM PORT 4

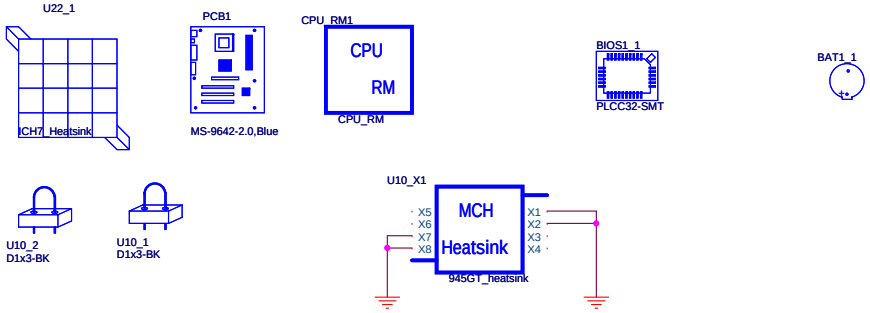


COM PORT 5

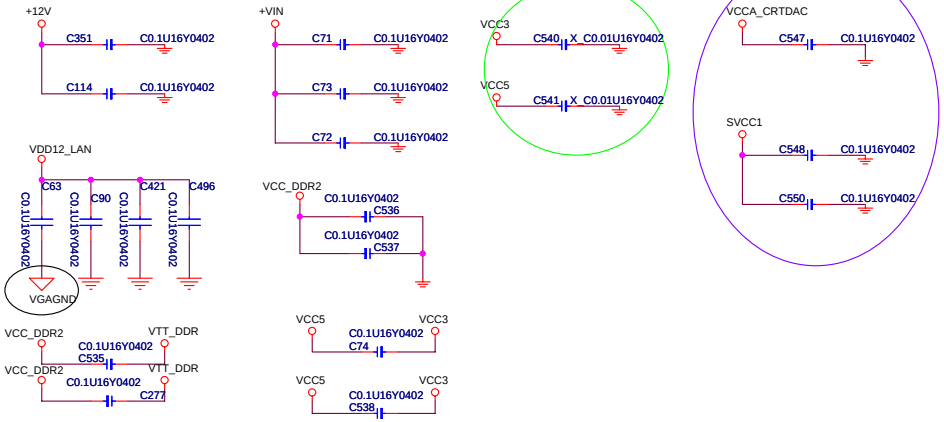


MICRO-STAR INt'L CO. , LTD.		
Title: COM PORT		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 31 of 38	

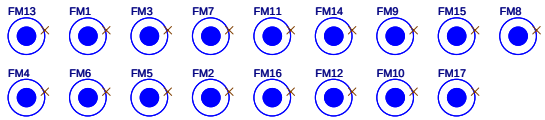
MANUAL PART



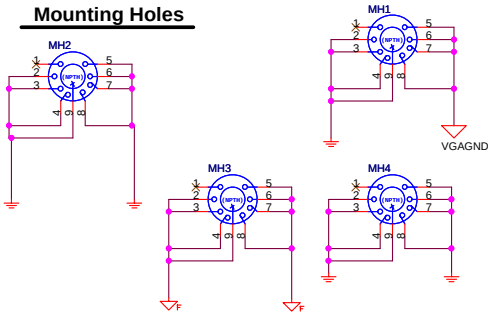
FOR EMI



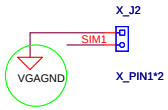
Optical Fiducial Marks



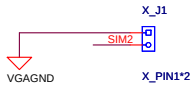
Mounting Holes



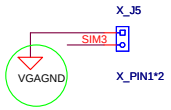
Layer1 / 5mil / 55ohm



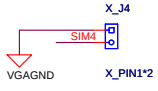
Layer3 / 4mil / 55ohm



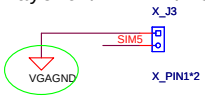
Layer8 / 5mil / 55ohm



Layer4 / 4mil / 55ohm



Layer6 / 4mil / 55ohm



MICRO-STAR INt'L CO. , LTD.		
Title: Manual Part/for EMI		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Wednesday, May 09, 2007	Sheet 32 of 38	

ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Alt	Rickles Signal Name
GPIO[0]	BM_BUSY#	AB18	I	VCC3p3	N	Y	3.3	N/A		BM_BUSY#
GPIO[1]	PCIREQ[5]#	C8	I	V5REF	Y	N	5	N/A		PREQ#5
GPIO[2]	PIRQE#	G8	I	V5REF	Y	N	5	N/A		PIRQ#E
GPIO[3]	PIRQF#	F7	I	V5REF	Y	N	5	N/A		PIRQ#F
GPIO[4]	PIRQG#	F8	I	V5REF	Y	N	5	N/A		PIRQ#G
GPIO[5]	PIRQH#	G7	I	V5REF	Y	N	5	N/A		PIRQ#H
GPIO[6]	unmuxed	AC21	I	Vcc3p3	Y	Y	3.3	N/A		SIO_OVT#
GPIO[7]	BIOS_WP#	AC18	I	Vcc3p3	Y	N	3.3	N/A		BIOS_WP#
GPIO[8]	unmuxed	E21	I	VccSus3p3	Y	Y	3.3	N/A		VCC3_SB
GPIO[9]	unmuxed	E20	I	VccSus3p3	Y	N	3.3	N/A		LAN1_EN
GPIO[10]	unmuxed	A20	I	VccSus3p3	Y	N	3.3	N/A		LAN2_EN
GPIO[11]	SMBALERT#	B23	I	VccSus3p3	Y	Y	3.3	N/A		SMB_ALERT#
GPIO[12]	unmuxed	F19	I	VccSus3p3	Y	N	3.3	N/A		LAN3_EN
GPIO[13]	unmuxed	E19	I	VccSus3p3	Y	Y	3.3	N/A		SIO_PME#
GPIO[14]	NC	R4	I	VccSus3p3	Y	Y	3.3			NC
GPIO[15]	NC	E22	I	VccSus3p3	N	N	3.3	1		AT/ATX SELECT
GPIO[16]	DPRSLPVR	AC22	O	Vcc3p3	N	N	3.3	1		DPRSLPVR
GPIO[17]	PCIGNT[5]#	D8	O	Vcc3p3	N	N	3.3	1		NC
GPIO[18]	STPPCI#	AC20	O	Vcc3p3	N	N	3.3	1		NC
GPIO[19]	AMP_GAIN0	AH18	I	Vcc3p3	D	N	3.3	1		AMP_GAIN0
GPIO[20]	STPCPU#	AF21	O	Vcc3p3	N	N	3.3	O		NC
GPIO[21]	AMP_EN	AF19	I	Vcc3p3	N	N	3.3	0		AMP_EN
GPIO[22]	REQ4#	A13	I	Vcc3p3	N	N	3.3	0		REQ4#
GPIO[23]	LDRQ1#	AA5	O	Vcc3p3	N	N	3.3			NC
GPIO[24]	NC	B3	O	VccSus3p3	Y	N	3.3	1		NC
GPIO[25]	NC	D20	O	VccSus3p3	N	N	3.3	N/A		NC
GPIO[26]	EL_RSVD	A21	O	VccSus3p3	N	N	3.3	0		NC
GPIO[27]	EL_STAT0	B21	O	VccSus3p3	N	N	3.3	0		NC
GPIO[28]	EL_STAT1	E23	O	VccSus3p3	N	N	3.3	0		NC
GPIO[29]	OC#5	C3	I	VccsUS3p3	Y	N	3.3			VCC3_SB
GPIO[30]	OC#6	A2	I	VccsUS3p3	Y	N	3.3			VCC3_SB
GPIO[31]	OC#7	B3	I	VccsUS3p3	Y	N	3.3			VCC3_SB
GPIO[32]	CLKRUN#	AG18	O	Vcc3p3	N	N	3.3	1		NC
GPIO[33]	AZ_DOCK_EN#	AC19	O	Vcc3p3	N	N	3.3	1		AUXGPIO_DIR1
GPIO[34]	AZ_DOCK_RST#	U2	O	Vcc3p3	N	N	3.3	0		AUXGPIO_DIR2
GPIO[35]	SATACLKREQ#	AD21	O	Vcc3p3	N	N	3.3	0		NC
GPIO[36]	AMP_GAIN1	AH19	I	Vcc3p3	N	N	3.3	0		AMP_GAIN1
GPIO[37]	NC	AE19	I	Vcc3p3	N	N	3.3	0		NC
GPIO[38]	unmuxed	AD20	I	Vcc3p3	Y	N	3.3	1		AUXGPIO_OE#
GPIO[39]	unmuxed	AE20	I	Vcc3p3	Y	N	3.3	1		NC
GPIO[48]	GNT4#	A14	O	Vcc3p3	N	N	3.3	1		NC
GPIO[49]	H_PWRGD	AG24	OD	V_FSB_VTT	Y	N	3.3	1		H_PWRGD

Note: All inputs are sticky. The status bit remains set as long as the input was asserted for two clocks. GPI's are sampled on PCI clocks in S0/S1. GPIs are sampled on RTC clocks in S3/S4/S5.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	ATADET0
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

FPGI4,3,2,1 V2.0 1100

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQB PIRQC PIRQD PIRQA	PCI_REQ#0 PCI_GNT#0	AD17	PCICLK0
Riser Card (PCI Slot 1)		PCI_REQ#1 PCI_GNT#1		PCICLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	(000)	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A

JUMPER SETTING

RTCRST	(1-2)CLEAR	(2-3)NORMAL

PCI Reset

DEVICE	Device
PLTRST# (ICH7M)	MS-7
PCIRST_ICH7# (ICH7M)	PCI Slot1
PCI_E_RST# (MS-7)	LAN Controller PCI-E X16 Slot
HD_RST# (MS-7)	IDE1
DEV_RST# (MS-7)	945GM(GMCH) Clock Gen Firmware Hub Super IO

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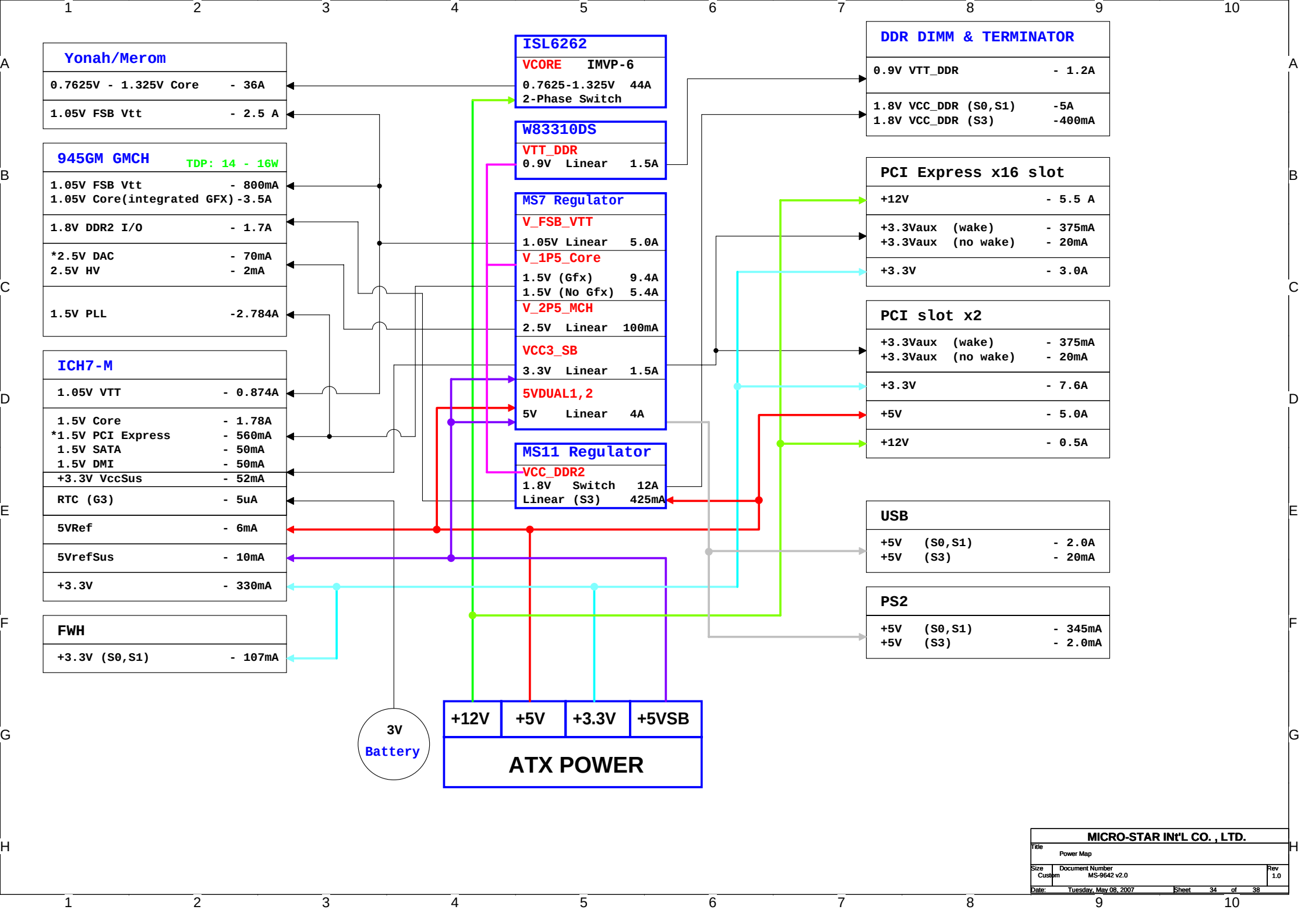
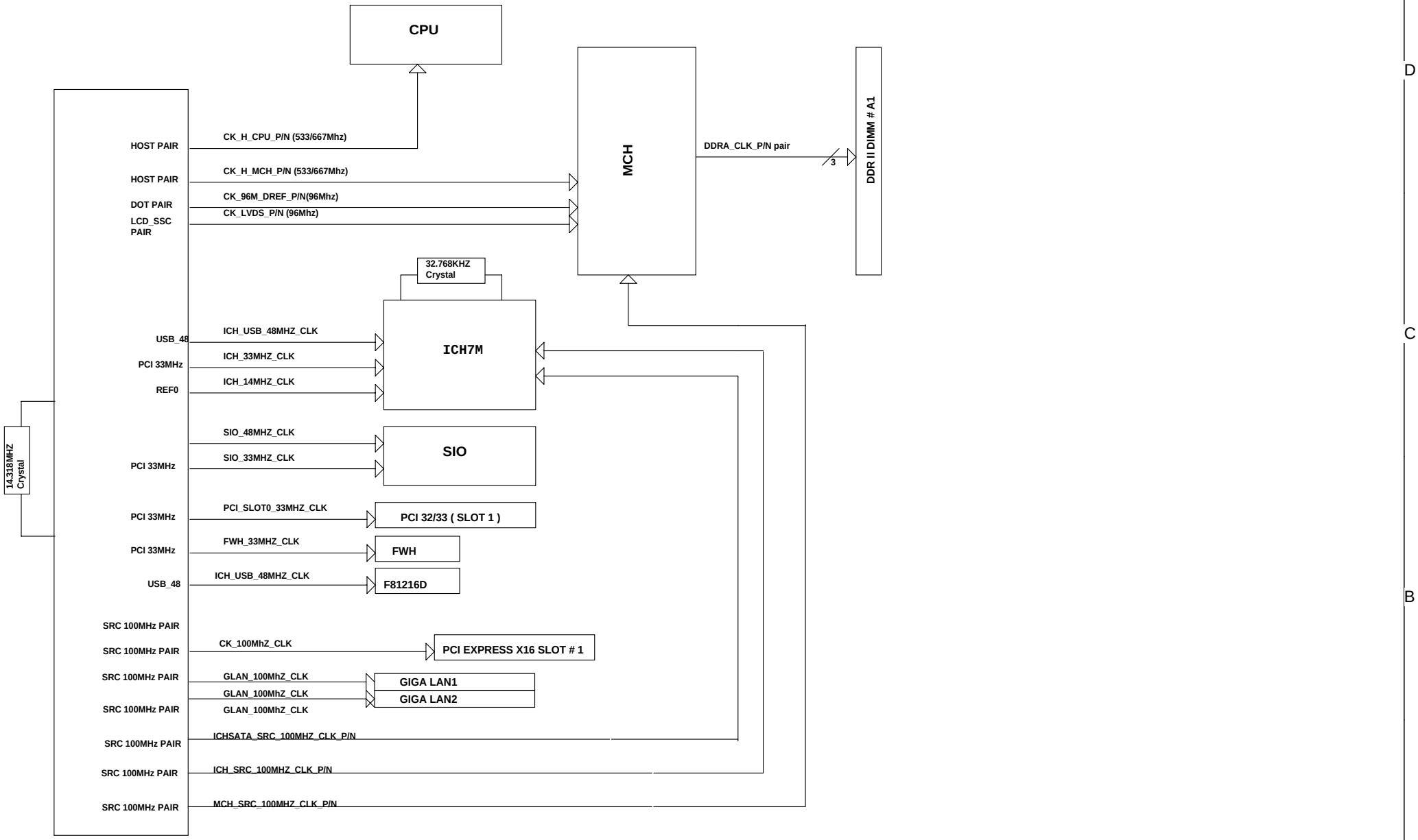
Title: General Purpose Spec & JUMPER SETTING

Size: D | Document Number: MS-9642 v2.0 | Rev: 1.0

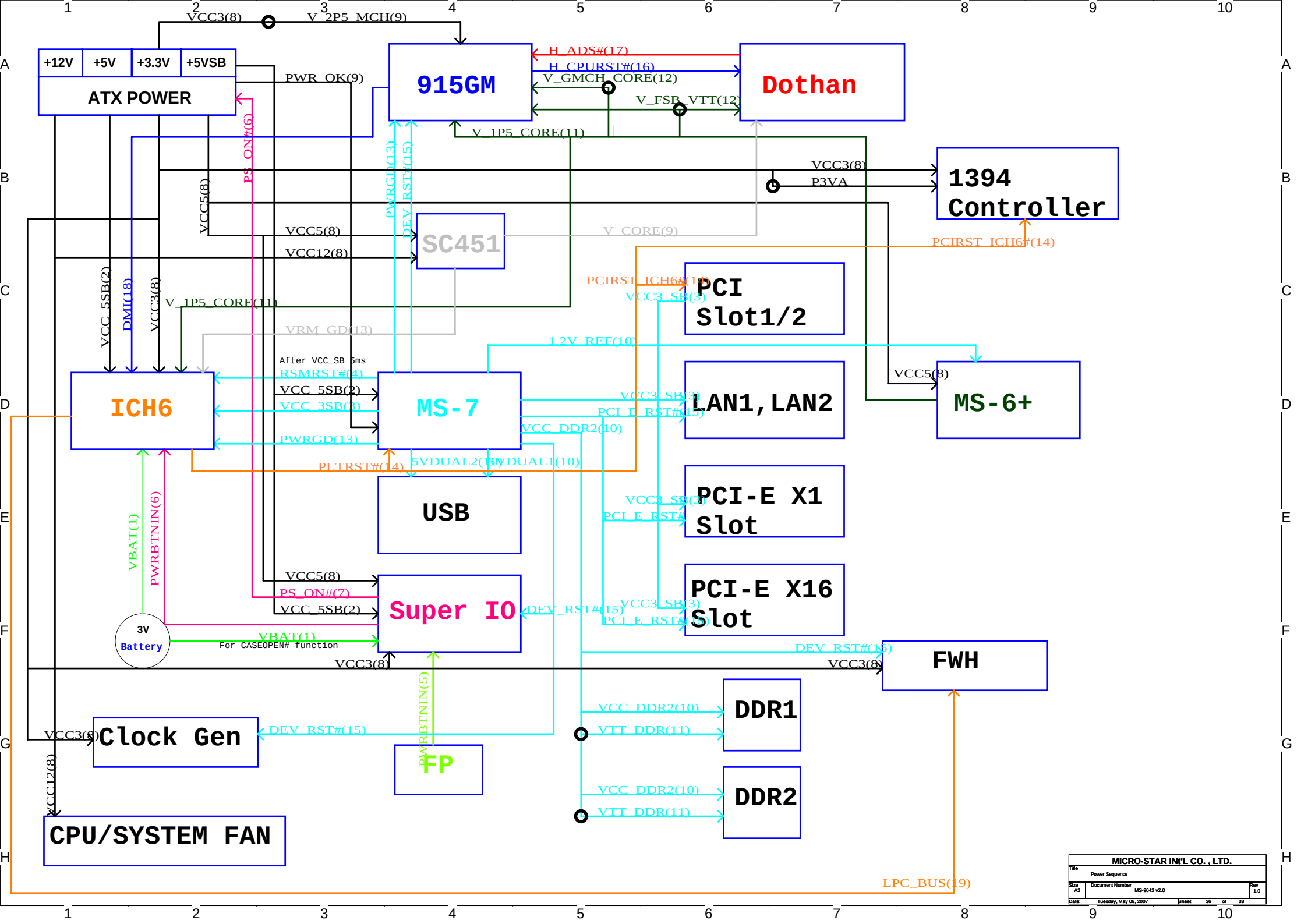
Date: Tuesday, May 08, 2007 | Sheet 33 of 38

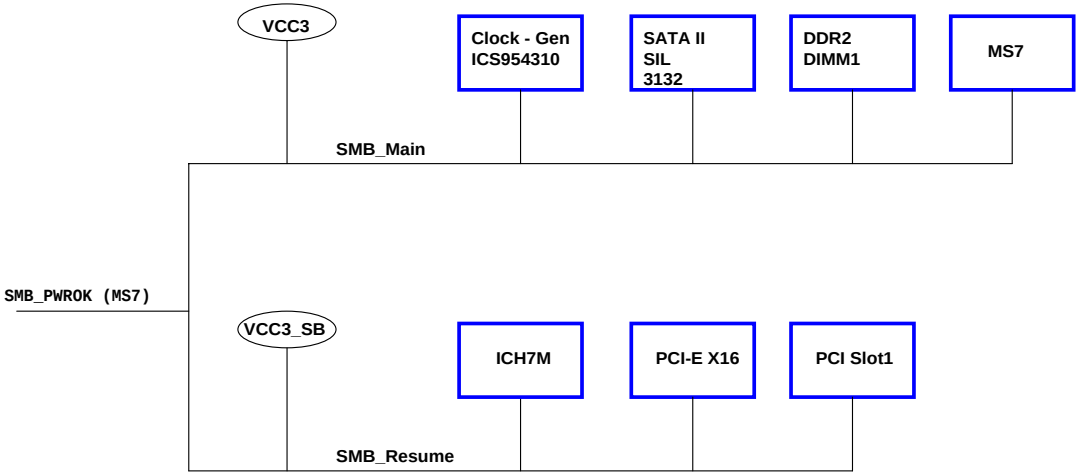

Yonah/Merom
0.7625V - 1.325V Core - 36A
1.05V FSB Vtt - 2.5 A
945GM GMCH TDP: 14 - 16W
1.05V FSB Vtt - 800mA
1.05V Core(integrated GFX) -3.5A
1.8V DDR2 I/O - 1.7A
*2.5V DAC - 70mA
2.5V HV - 2mA
1.5V PLL -2.784A
ICH7-M
1.05V VTT - 0.874A
1.5V Core - 1.78A
*1.5V PCI Express - 560mA
1.5V SATA - 50mA
1.5V DMI - 50mA
+3.3V VccSus - 52mA
RTC (G3) - 5uA
5VRef - 6mA
5VrefSus - 10mA
+3.3V - 330mA
FWH
+3.3V (S0,S1) - 107mA
ISL6262
VCORE IMVP-6
0.7625-1.325V 44A
2-Phase Switch
W83310DS
VTT_DDR
0.9V Linear 1.5A
MS7 Regulator
V_FSB_VTT
1.05V Linear 5.0A
V_1P5_Core
1.5V (Gfx) 9.4A
1.5V (No Gfx) 5.4A
V_2P5_MCH
2.5V Linear 100mA
VCC3_SB
3.3V Linear 1.5A
5VDUAL1,2
5V Linear 4A
MS11 Regulator
VCC_DDR2
1.8V Switch 12A
Linear (S3) 425mA
3V
Battery
+12V
+5V
+3.3V
+5VSB
ATX POWER
DDR DIMM & TERMINATOR
0.9V VTT_DDR - 1.2A
1.8V VCC_DDR (S0,S1) -5A
1.8V VCC_DDR (S3) -400mA
PCI Express x16 slot
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI slot x2
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 7.6A
+5V - 5.0A
+12V - 0.5A
USB
+5V (S0,S1) - 2.0A
+5V (S3) - 20mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
MICRO-STAR INt'L CO. , LTD.
Title
Power Map
Size
Custom
Document Number
MS-9642 v2.0
Rev
1.0
Date:
Tuesday, May 08, 2007
Sheet
34
of
38

MS-9642 CLOCK BLOCK DIAGRAM



MICRO-STAR INt'L CO. , LTD.		
Title: CLOCK MAP		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 35 of 38	


+12V
+5V
+3.3V
+5VSB
ATX POWER
915GM
Dothan
1394 Controller
SC451
PCI Slot1/2
ICH6
MS-7
LAN1,LAN2
MS-6+
USB
PCI-E X1 Slot
PCI-E X16 Slot
Super IO
3V Battery
FWH
Clock Gen
DDR1
DDR2
FP
CPU/SYSTEM FAN
VCC3(8)
V_2P5_MCH(9)
PWR_OK(9)
H_ADS#(17)
H_CPURST#(16)
V_GMCH_CORE(12)
V_FSB_VTT(12)
V_1P5_CORE(11)
PS_ON#(6)
PWRGD(13)
DEV_RST#(15)
VCC5(8)
VCC12(8)
P3VA
V_CORE(9)
PCIRST_ICH6#(14)
VCC_5SB(2)
DMI(18)
VRM_GD(13)
1.2V_REF(10)
After VCC_SB 5ms
RSMRST#(4)
VCC_3SB(3)
PWRGD(13)
PLTRST#(14)
5VDUAL2(10)
5VDUAL1(10)
VCC_DDR2(10)
PCI_E_RST#(15)
VBAT(1)
PWRBTNIN(6)
PS_ON#(7)
For CASEOPEN# function
PWRBTNIN(5)
VTT_DDR(11)
LPC_BUS(19)
MICRO-STAR INt'L CO. , LTD.
Power Sequence
MS-9642 v2.0
Tuesday, May 08, 2007



MICRO-STAR INt'L CO. , LTD.		
Title: <Title>		
Size: Custom	Document Number: MS-9642 v2.0	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 37 of 38	

ADD R724,725,726,727,REMOVE RN16 FOR V2.0 IN P15 (04.25)

JAUD1 PIN1 CONNECT TO VCC5 (04.25)

ADD IN5817 FOR SYS,CPU,AUX FAN CONNECTER (04.25)

R717,718,486,495 CHANGE TO RESERVE (04.25)

POLY SWITCH CHANGE THE NEW PN FOR 2.0A CURRENT ,FS4,6,7 (04.25)

GLAN3 CHANGE TO RESERVED (04.25)

R74 STUFF,R80,RESERVED (04.25)

add 2 copper in p16 (04.27)

remove R717,718,486,495 (04.27)

ADD 0.1UF FOR PU1

C53,C74,C321,C266,C359,C84,C38,C56 上件0.1uF

L4,L5,L6上件120nH

C70,C78,C80不上件 FOR EMI (04.27)

FS5 CHANGE TO D08-0200230-R02 (04.27)

R11-0103022-W08 change to R11-0103012-W08

R11-0472022-W08 change to R11-0472012-W08

R11-0273022-W08 change to R11-0273012-W08

CPU_RM1 change to E91-0000084-L06

Title	<Title>	
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, May 08, 2007	Sheet 38 of 38	