Tracking Generator Module Assembly (Option)

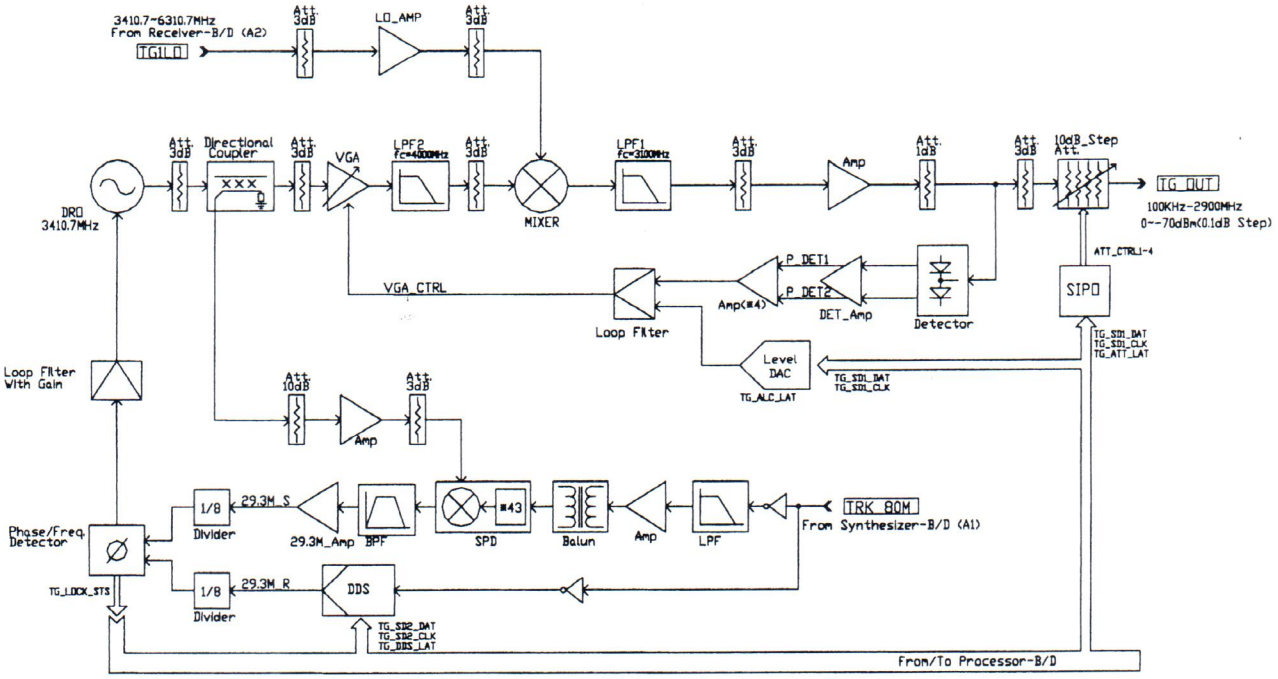

Fig. 2-10

1. Overview

The Tracking Generator is the RF Signal Source. The output frequency, which can be set or swept by TG1LO (3410.7 ~ 6310.7 ㎒), can come out within the range from 100 ㎑ to 2.9 ㎓. The output power, which can be controlled by the setting of 10dB Step Attenuator and Level DAC, is within the range from 0dBm to -70dBm. Its output frequency equals the subtraction of 3410.7 ㎒ from the TG1LO. By Providing LO signal the same that LO of Spectrum Analyzer for LO port of the Tracking Generator, the frequency of TG OUT is synchronized with the received frequency of Spectrum Analyzer. Largely divided in the respect of function, Tracking Generator has 2 blocks. One is ALC (Automatic Level Control) which stabilizes the level of TG OUT, the other is PLL (Phase Locked Loop) which does the frequency of TG OUT.

2. ALC (Automatic Level Control)

(1) Generator description as to ALC

A 3410.7 ㎒ signal is generated in the DRO (Dielectric Resonant Oscillator) block and coupled to VGA (Variable Gain Amplifier) block by the DC (directional coupler). The input power level of the VGA is about -13dBm, which is determined by the coupling coefficient of the DC and DRO output power. The controlled voltage (VGA CTRL) adjusts the gain of the VGA and its level is determined by the output of the Detector and Level DAC. The Detector discriminates the quantity of output power and converts voltage proportioned to it, while the Level DAC sets the reference voltage proportioned to desired output power. The detected voltage is differentially amplified, added, amplified and sent to the Loop Filter, which compares the reference voltage at a specified output power level with the detected voltage, amplifies and filters. The TG output frequency is determined by the frequency of the LO. The 3410.7 ㎒ (VGA Output Frequency) and LO frequency are mixed with each other. This mixed output frequency (IF) is filtered by LPF1, amplified by 2 stages of 20dB Amps and attenuated by the 3dB Attenuator at the input and output of the 20dB Amp. This amplified output is sent to the Detector directly and to the TG OUT, passing through the 3dB Attenuator and 10dB Step Attenuator.

(2) VGA (Variable Gain Amplifier)

The VGA is composed of two amplifiers and two PIN (attenuators). This block has about 30dB fixed gain and variable attenuation, which is controlled by the voltage (VGA CTRL). The voltage (VGA CTRL) sets the DC bias current of the PIN diode, which, subsequently determines the amount of attenuation of the PIN (attenuators).

(3) Mixer

The Mixer has two inputs (LO & RF) and one output (IF). The RF signal (3410.7 ㎒) comes from the DRO and the LO signal (3410.7 to 6310.7 ㎒) comes from the TG1LO. The frequency of the IF depends on that of the LO as the RF signal frequency is constant and the LO signal frequency is variable. TG1LO is amplified sufficiently enough to drive LO of the Mixer by the LO AMP. The Mixer is composed of a Schottky diode, Microstrip Coplanar waveguide and a Microstrip Slot line. To satisfy wide band characteristic at the LO port, a Balun is designed taking advantage of the Coplanar waveguide. This LO signal is arrived at the Schottky diode by the transition form the Coplanar waveguide to the Slot line. The RF and IF signals are separated by the Microstip T-Junction. The frequency of TG OUT is the same as the IF output.

(4) Detector and Amplifiers

The main role of this block is to detect the RF power level. Positive and negative signals detected are respectively amplified 4 times and added.

(5) Loop Filter and Level DAC

The power level of TG OUT is determined according to respectively established DAC Code. Of which the range exist from 0.0dBm to -9.9dBm and the resolution is 0.1dB. This Code is reference voltage to be compared with the detected voltage. The difference of them is amplified, filtered and result in voltage (VGA CTRL).

3. PLL (Phase Locked Loop)

(1) General description as to PLL

3410.7 ㎒ is oscillated in the DRO Block. DR is the initial of the dielectric resonator, used main component of the DR Oscillator. Phase locked frequency is as following equation; Fo = (Ref × N) – DDS_F. In the 2399 Spectrum Analyzer, the reference frequency is 80 ㎒ and multiplying number (N) is 43. The output frequency of the DDS (Direct Digital Synthesizer) can be set and adjusted by 32bit digital binary code. For the purpose of making Fo, 3410.7 ㎒, DDS_F should be 29.3 ㎒. In SPD (Sampling Phase Detector) Block, detected is the difference of an eighth of the mixed output frequency and an eighth of the DDS_F. In Loop Filter with gain block, the detected output is amplified and filtered to be a voltage(DRO-CTRL), which controls the frequency of the DRO.

(2) VTO (Voltage Tuned Oscillator)

TR has potentially of being unstable by using series feedback, and the DRO (Dielectric Resonator) is magnetically coupled with microstripline, which is connected to input of the amplifier. The lengths of microstriplines connected base and emitter are designed to satisfy the condition that can be oscillate. The output of TR, namely collector, has matched microstripline circuit to make maximum output power. The DRO is magnetically coupled with microstripline and varactor. As the voltage (DRO_CTRL) of varactor changes, the capacitance of it does and consequently output frequency of DRO does. Also, to adjust the frequency manually, the cover of DRO has tuning screw of which the height determines it.

(3) SPD (Sampling Phase Detector)

High frequency signal having high stability and low noise generally can be acquired from the harmonics of stable low frequency like Crystal Oscillator. SPD block has 2 functions. One is frequency multiplier, which makes 43 times of the 80 ㎒. For this application, SRD (Step Recovery Diode) is used. It has very high capacity on the state of positive bias, has small on the state of reverse and can be thought as high efficient switch controlled by the electric charge. Having very short transition time (about a number of pico sec), it can generate acute impulse to have very high efficiency at high order harmonics. The other is frequency mixer, which mixes 3440 ㎒ (43 × 80 ㎒) with 3410.7 ㎒ (the frequency of DRO) and yields the different frequency between them. In front of the SPD block, there is a Balun Transformer to sustain 180 ° phase difference at single balanced mixer. The output frequency of the SPD passes Band pass Filter and is amplified with about 54 dB gain at 29.3 ㎒. The other IF frequency, 50.7 ㎒, should be sufficiently suppressed. To accomplish this end, the IF (29.3 ㎒) passes through the Band pass Filter to have about 30 dB attenuation at 50.7 ㎒.

(4) DDS (Direct Digital Synthesizer)

A frequency output is controlled by 32-bit binary code and its dada is determined by this equation; (Fout/80 ㎒) × 2^32. Except the frequency of DDS output, many other frequencies come out like this; Fin ± Fout, 2Fin = Fout, 3Fin ± Fout. The level of these frequencies is about -3 ~ -10 dBc. But, it was designed to suppressed fully by the placing of 5-pole elliptic LPF which is recommended on the selected DDS Datasheet.