SM4A 4-Bit Microcomputer (LCD Driver)

■ Description

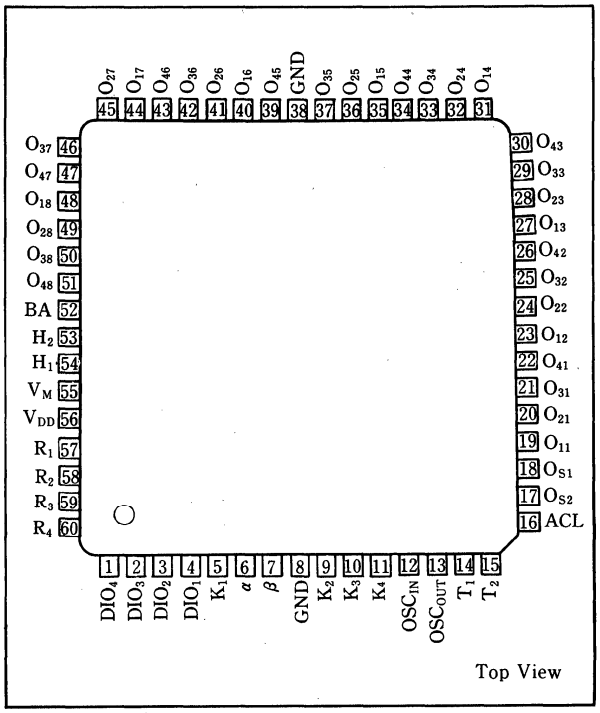
The SM4A is a CMOS 4-bit microcomputer which integrates a 4-bit parallel procesing function, a 2,268-byte ROM, a 96-word RAM, a 15-stage divider, and a 68-segment LCD driver circuit in a single chip.

This microcomputer is applicable to the system having multiple LCD segment, with low power consumption.

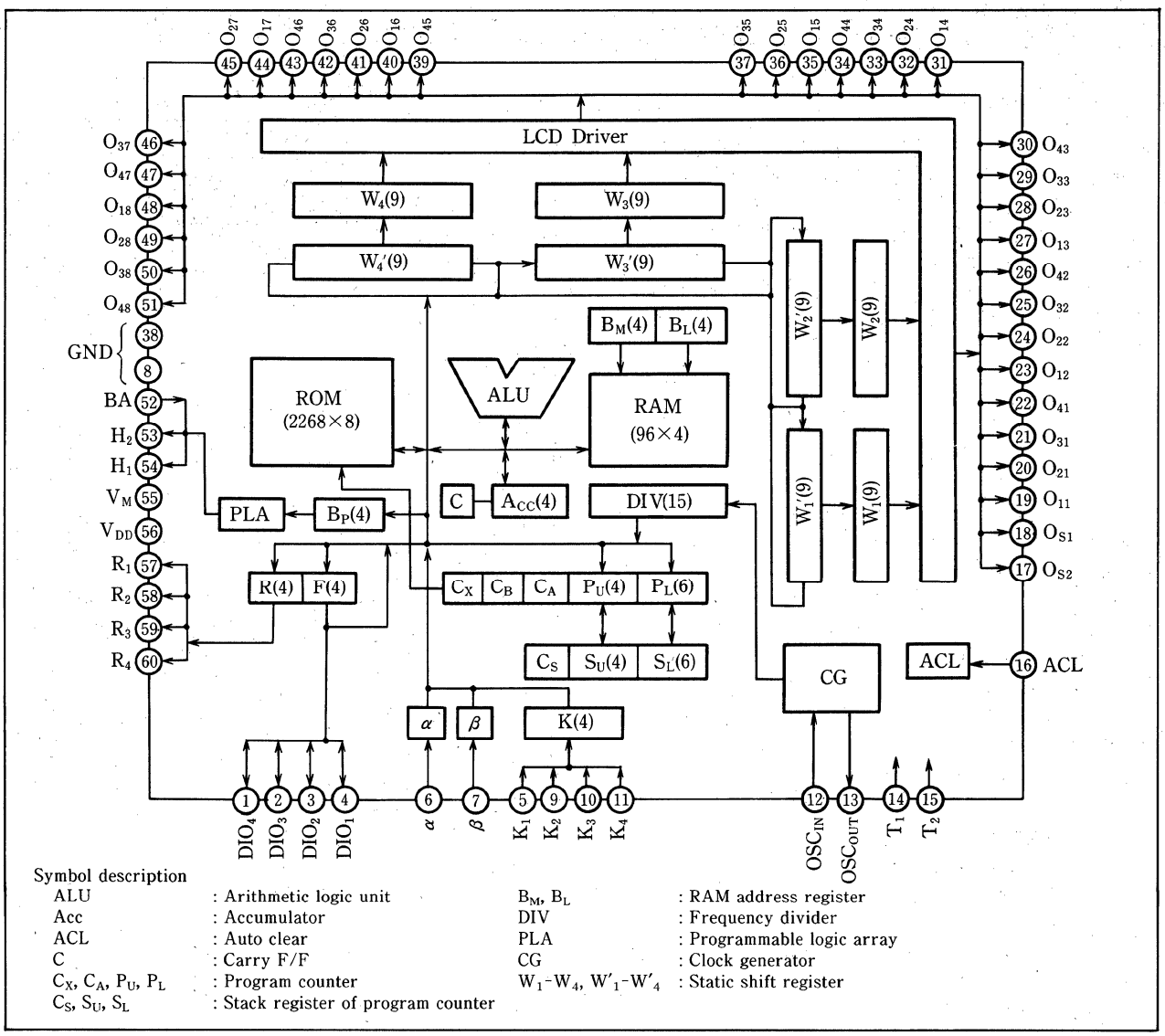
■ Features

1. CMOS process
2. ROM capacity: 2,268×8 bits
3. RAM capacity: 96×4 bits
4. Instruction set: 54
5. Subroutine nesting: 1 level
6. Instruction cycle: 61 μs (TYP.)
7. Input/output ports
   - I/O ports: 4
   - Input ports: 6
   - Output ports: 4
   - LCD output ports: 34 for segment
     2 for common
8. On-chip clock divider
9. On-chip crystal oscillator
10. External RAM access
11. LCD driver circuit
    (68-segment, 1/2 bias, 1/2 duty)
12. Standby function
13. Single power supply: −3V (TYP.)
14. 60-pin QFP (QFP60-P-1414)

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	B_M, B_L	: RAM address register
Acc	: Accumulator	DIV	: Frequency divider
ACL	: Auto clear	PLA	: Programmable logic array
C	: Carry F/F	CG	: Clock generator
C_X, C_A, P_U, P_L	: Program counter	W_1-W_4, W'_1-W'_4	: Static shift register
C_S, S_U, S_L	: Stack register of program counter		

Pin Description

Symbol	I/O	Circuit type	Function
K_1-K_4	I	Pull down	Acc←K_1-K_4
α	I	Pull down	Set by ↑, reset after test instruction execution
β	I	Pull down	Input signal is held for 1 instruction cycle, test possible
DIO_1-DIO_4	I/O	3-state output	Acc←→DIO_1-DIO_4
R_1-R_4	O	Complementary	R_1-R_4←Acc
O_{11}-O_{48} OS_1,OS_2	O		W and W′ registers output: used for LCD segment output
H_1, H_2	O		3-state level output possible, used for LCD common output
BA	I	Pull up	For test the input signal of High or Low
T_1, T_2	I		For test (Connected to V_{DD} normally)
ACL	I		Auto clear
OSC_{IN}, OSC_{OUT}			For clock oscillation
V_M			Power supply for LCD driver
GND, V_{DD}			Power supply for logic circuit

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−3.5 to +0.3	V	1
	V_M	−3.5 to +0.3	V	
	V_{IN}	V_{DD}−0.3 to +0.3	V	
Operating temperature	Topr	−5 to +55	℃	
Storage temperature	Tstg	−55 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−3.2 to −2.6	V
	V_M	V_{DD}/2 (TYP.)	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD}=−3.2 to −2.6V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−0.6			V	1
	V_{IL1}				V_{DD}+0.6	V	
	V_{IH2}		−0.3			V	2
	V_{IL2}				V_{DD}+0.3	V	
Output voltage	V_{OH1}	I_{OUT}=50 μA to V_{DD}	−0.5			V	3
	V_{OL1}	I_{OUT}=5 μA to GND			V_{DD}+0.5	V	
	V_{OH2}	I_{OUT}=50 μA to V_{DD}	−0.5			V	4
	V_{OL2}	I_{OUT}=30 μA to GND			V_{DD}+0.5	V	
	V_{OH3}	I_{OUT}=50 μA to V_{DD}	−0.5			V	5
	V_{OL3}	I_{OUT}=50 μA to GND			V_{DD}+0.5	V	
	V_{OA}	No load	−0.3			V	6
	V_{OB}	V_{DD}=−3.0V		−1.5		V	
	V_{OC}	V_M=−1.5V			−2.7	V	
Output current	I_{SO}	V_{OUT}=−0.2V	100			μA	7
	I_{SIN}	V_{OUT}=V_{DD}+0.2V	100			μA	
Supply current	I_{DA}	During full-range operation		50	100	μA	
	I_{DS}	When system clock is stationary		10	20	μA	

Note 1: Applied to pins K_1, K_2, K_3, K_4, α, β
Note 2: Applied to pin ACL
Note 3: Applied to pins O_{48}-O_{11}, O_{S1}, O_{S2}
Note 4: Applied to pins DIO_1-DIO_4
Note 5: Applied to pins R_2, R_3, R_4
Note 6: Applied to pins H_1, H_2
Note 7: Applied to pin R_1

■ Pin Functions

(1) K_1-K_4 (Inputs)

The input ports K_1-K_4 are connected to the accumulator Acc. The contents of the K_1-K_4 are loaded into the Acc.

(2) α, β (Inputs)

The input ports α and β can be independently tested. The α input latches the α F/F at the rising edge of the input, and can be tested by the TA instruction. The α F/F is reset after the test. The β is used to put the input signal into the β F/F for the interval of one instruction, and can be tested by the TB instruction.

(3) DIO_1-DIO_4 (I/O ports)

The DIO_1-DIO_4 pins normally output the contents of the F_1-F_4 F/F. The F_1-F_4 F/F data can be changed on transferring the accumulator Acc by the ATF instruction. Connecting the DIO_1-DIO_4 with the Acc allows the data transfer between the Acc and an external RAM by the READ and WRITE instructions. The output buffer of the F_1-F_4 F/F is designed to be a three-state output, and it is kept high impedance when the DIO input is loaded into the Acc by the READ instruction.

(4) R_1-R_4 (Outputs)

Connecting the DIO_1-DIO_4 with the Acc outputs the contents of the Acc. And selecting the programmable logic array PLA generates a sound output, and allows a segment output on pins O_{S3} and O_{S4}.

(5) O_{ij} (i=1 to 4, j=1 to 8), O_{S1}, O_{S2} (Outputs)

34-bits of output ports O_{ij}, O_{S1} and O_{S2} are used to output the contents of the static shift register W'_{in}, W_{in} (i=1 to 4, n=0 to 8). The output signal can be used as a segment signal for a 1/2 duty scheme, and a strobe signal for the key-scan, according to the display mode. These ports output the address of the external RAM upon execution of the READ or WRITE instruction.

(6) H_1, H_2 (Output)

The H_1 and H_2 are used to output the common signal of an LCD with 1/2 bias, 1/2 duty scheme in a three output level inculding V_{DD}, GND and V_M.

(7) BA (Inputs)

The BA pin is used to test the input level of High or Low by instructions.

■ Hardware Cnfiguration

(1) Program memory (ROM)

The on-chip ROM has a 2,268 byte organized as 36 pages×63 steps×8 bits. The program counter consists of 1-bit registers C_X and C_A, a 4-bit register P_U, and a 6-bit polynomial counter P_L. The P_L is used to specify the steps, the P_U specify the pages, and the C_A specify the fields. The C_X register is only used to specify the subroutine pages.

Page↓ / →Field	C_X=0		C_X=1
	C_A=0	C_A=1	—
0	0	16	32
1	1	17	33
2	2	18	34
3	3	19	35
4	4	20	
5	5	21	
6	6	22	
7	7	23	
8	8	24	
9	9	25	
10	10	26	
11	11	27	
12	12	28	
13	13	29	
14	14	30	
15	15	31	

Fig. 1 ROM configuration (fields and pages)

(2) Data memory (RAM)

Data memory has a 6×16 word×4-bit configuration, and is addressed by a 4-bit B_L and a 4-bit B_M.

(3) Oscillator circuit

An on-chip crystal oscillator allows the oscillation with the external circuit shown in Fig. 3.

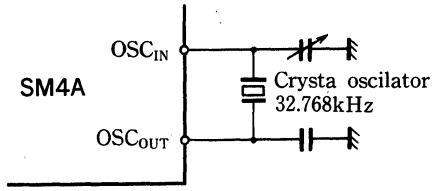


Fig. 3

(4) Divider

A 15-stage resettable divider outputs a 1 Hz signal at the lowest stage when a 32.768kHz crystal oscillator is used. The output on each stage can be loaded into the accumulator Acc on an 4-bit basis.

(5) Reset function (ACL)

An on-chip reset circuit may sometimes require a capacitor between the ACL pin and GND pin. It takes 1 sec on an internal timer from the beginning of oscillation to clear the ACL mode when power on.

	BM_3	0				1	
	BM_2	0	0	1	1	—	
	BM_1	0	1	0	1	0	1
B_L	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	10						
	11						
	12						
	13						
	14						
	15						
		X	Y	Z	M	U	T

Fig. 2 RAM configuration

■ Instruction Set

Mnemonic	Machine code I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1	Operation
SBM	02	$1 \rightarrow B_{M3}$ ($B_{M3}=1$ for next step only)
LB	40-4F	$I_4, I_3 \rightarrow B_{L2}, B_{L1}$ $I_2, I_1 \rightarrow B_{M2}, B_{M1}$
LBL	5F 00-FF	I_8-$I_5 \rightarrow B_{M4}$-B_{M1} I_4-$I_1 \rightarrow B_{L4}$-B_{L1}
INCB	64	$B_L+1 \rightarrow B_L$ if $B_L=a$; skip
DECB	6C	$B_L-1 \rightarrow B_L$ if $B_L=b$; skip
RM	04-07	$0 \rightarrow Mi$ ($i=I_2\ I_1$)
SM	0C-0F	$1 \rightarrow Mi$ ($i=I_2\ I_1$)
ATPL	03	$Acc \rightarrow P_{L4}$-P_{L1}
ADD	08	$Acc+M \rightarrow Acc$
ADD11	09	$Acc+M+C \rightarrow Acc$ $C_4 \rightarrow C$ if $C_4=1$; skip
COMA	0A	$\overline{Acc} \rightarrow Acc$
EXBLA	0B	$Acc \leftrightarrow B_L$
EXC	10-13	$Acc \leftrightarrow M$ $B_{M2}, B_{M1} \oplus I_2, I_1 \rightarrow B_{M2}, B_{M1}$
EXCI	14-17	$Acc \rightarrow M$ $B_{M2}, B_{M1} \oplus I_2, I_1 \rightarrow B_{M2}, B_{M1}$ $B_L+1 \rightarrow B_L$ if $B_L=a$; skip
EXCD	1C-1F	$Acc \rightarrow M$ $B_{M2}, B_{M1} \oplus I_2, I_1 \rightarrow B_{M2}, B_{M1}$ $B_L-1 \rightarrow B_L$ if $B_L=b$; skip
LDA	18-1B	$M \rightarrow Acc$ $B_{M2}, B_{M1} \oplus I_2, I_1 \rightarrow B_{M2}, B_{M1}$
LAX	20-2F	I_4-$I_1 \rightarrow Acc$
ADX	30-3F	I_4-$I_1+Acc \rightarrow Acc$ if $C_4=1$; skip
DC	3A	$10+Acc \rightarrow Acc$
DTA	5E 04-07	$DIV \rightarrow Acc$
ROT	6B	$C \rightarrow A_4 \rightarrow A_3 \rightarrow A_2 \rightarrow A_1 \rightarrow C$
ATBP	01	$Acc \rightarrow Bp$
ATW	5D	$Acc \rightarrow W'_{i8}$ ($i=1$ to 4) W'in Right Shift ($i=1$ to 4, $n=7$ to 0)
PATW	00	$Acc \rightarrow W'_{i8}$ $W'_{i8} \rightarrow W'_{i7}$ ($i=1$ to 4)
ATF	60	$Acc \rightarrow F$
ATR	61	$Acc \rightarrow R$
READ	68	$DIO \rightarrow Acc$
WRITE	69	$Acc \rightarrow DIO$
KTA	6A	$K_i \rightarrow Acc$
RC	66	$0 \rightarrow C$
SC	67	$1 \rightarrow C$

Mnemonic	Machine code I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1	Operation
TW	5C	$W'_{in} \rightarrow W_{in}$ (i=1 to 4, n=8 to 0)
PTW	59	$W'_{in} \rightarrow W_{in}$ (i=1 to 4, n=8,7)
WR	62	$0 \rightarrow W'_{48}$ W_{in} Right Shift
WS	63	$1 \rightarrow W'_{48}$ W_{in} Right Shift
IDIV	65	$0 \rightarrow$DIV
TA	50	if $\alpha = 1$; skip
TB	51	if $\beta = 1$; skip
TC	52	if C=0; skip
TAM	53	if Acc=M; skip
TM	54-57	if Mi=1 (i=I_2 I_1); skip
TA0	5A	if Acc=0; skip
TABL	5B	if Acc=B_L; skip
TIS	58	if 1S=0; skip
② TAL	5E 02	if BA=1; skip
② CEND	5E 00	Clock stop
② ST	5E 03	$1 \rightarrow$T
COMCB	6D	$\overline{C_B} \rightarrow C_B$
SSR	70-7F	I_4-$I_1 \rightarrow S_{U4}$-S_{U1} $1 \rightarrow$E (next step only)
TR0	80-BF	if R=0; I_6-$I_1 \rightarrow P_{L6}$-P_{L1} $S_U \rightarrow P_U$ $C_B \rightarrow C_A$ if R=1; I_6-$I_1 \rightarrow P_{L6}$-P_{L1}
TR1	C0-FF	if R=0, E=0; I_6-$I_1 \rightarrow P_{L6}$-P_{L1} $0 \rightarrow P_U \rightarrow S_U$ $P_L+1 \rightarrow S_L$ $1 \rightarrow$R $1 \rightarrow C_A \rightarrow C_S$ $1 \rightarrow$D if R=0, E=1; I_6-$I_1 \rightarrow P_{L6}$-P_{L1} $P_U \leftrightarrow S_U$ $P_L+1 \rightarrow S_L$ $C_B \rightarrow C_A \rightarrow C_S$ $1 \rightarrow$R if R=1; I_6, $I_5 \rightarrow P_{U2}$, P_{U1} I_4-$I_1 \rightarrow P_{L4}$-P_{L1}
RTN0	6E	$C_S \rightarrow C_A$ $S_U \rightarrow P_U$ $S_L \rightarrow P_L$ $0 \rightarrow$R
RTN1	6F	$C_S \rightarrow C_A$ $S_U \rightarrow P_U$ $S_L \rightarrow P_L$ $0 \rightarrow$R skip next step
JUMP	00-FF	if D=1 I_8-$I_6 \rightarrow P_{U4}$, P_{U3}, P_{U1} I_5-$I_1 \rightarrow P_{L5}$-P_{L1}

System Configuration Example (Radio PLL controller)