FY6600 Registers Overview

Reg.	Purpose				
HEX	Channel	Function	Comment 1	Comment 2	Action
1	1	FreqLSW	CH1 Freq =100 000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
2	1	FreqMSW	CH1 Freq =100 000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
3	2	FreqLSW	CH2 Freq =100 000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
4	2	FreqMSW	CH2 Freq =100 000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
5	1,2	Channel Functions Mode	Bit 5-4-3 = 000 = 0 : CH2 Flash Functions Bit 5-4-3 = 001 = 1 : CH2 Square Bit 5-4-3 = 010 = 2 : CH2 CMOS Bit 5-4-3 = 011 = 3 : CH2 DC Bit 5-4-3 = 100 = 4 : CH2 OFF Bit 2-1-0 = 000 = 0 : CH1 Flash Functions Bit 2-1-0 = 001 = 1 : CH1 Square Bit 2-1-0 = 010 = 2 : CH1 CMOS Bit 2-1-0 = 011 = 3: CH1 Adj-Pulse Bit 2-1-0 = 100 = 4: CH1 DC	CH1 OFF is DC Mode with Amplitude&Offset = 0	
6	1,2	Relays Control + Config bits	Bit 0 = CH2 JD3 Relay ON/OFF (0/1) Bit 1 = CH2 JD1 Relay ON/OFF (0/1) Bit 2 = CH1 JD4 Relay ON/OFF (0/1) Bit 3 = CH1 JD2 Relay ON/OFF (0/1) Bit 4 = AC/DC Input Coupled Mode (0/1) Bit 5 = Uplink ON/OFF (0/1) Bit 6 = Uplink Mode Master/Slave (0/1)	CH1 Low Range = JD4=ON, JD2=OFF CH1 Mid Range = JD4=OFF, JD2=OFF CH1 High Range = JD4=OFF, JD2=ON CH2 Low Range = JD3=ON, JD1=OFF CH2 Mid Range = JD3=OFF, JD1=OFF CH2 High Range = JD3=OFF, JD1=ON	Bit5 & Bit6 seem to be linked strangely: To be checked
8	1	PhaseDW	Phase = 360*(1-PhaseDW/1048575)	PhaseDW=(1-Phase/360)*1048575	
9	2	PhaseDW	Phase = 360*(1-PhaseDW/1048575)	PhaseDW=(1-Phase/360)*1048575	
A					
B					
C	Input	Input_measure_Request value	01 = ? 03 = Request Frequency 07 = Request counter 0B = Request +WIDE 0F = ? 1B = Request -WIDE 1A = ? 1E = ? 1F = ?	Work in progress	
D	Input	Input_measure_Requested value	Read value requested by Reg 0x0C		
E	1,2	Flash to FP Read_Value_Read	Return one single value read from flash (one waveform sample but not only)	Address has to be written in reg0x12 before and triggered with Reg 0x0F	
F	1,2	Flash to FP Read_Trigger	Write 1 to trigger Read then write 0 (Reset Trigger)		
10			Request with value from 0 to F written then read reg 0x1A: Read 16 parameters	Seen only in startup sequence	To be identified. Low priority
11	1,2	Flash to FPGA Read_Channel Number	CH1=1 , CH2=2, 0=?	Set which channel to load the Waveform for	
12	1,2	Memory Address	Waveform Sample Memory address	Set Address in register and fire trigger (0F, 13, 14 or 16)	
13	1,2	Flash to FPGA Read_Trigger	Write 1 to trigger Read then write 0 (Reset Trigger)		
14		FP to Flash Write_Trigger	write 1 to trigger , 0 to reset (rearm trigger)	Written with 0 before flash read operation	
15		FP to Flash Write_Value	Value to write to Flash		
16		FP to Flash Write_Page_Erase_Trigger	Write 1 to trigger , 0 to reset (rearm trigger)	Reg0x12 contains address of page to be erased. 1 waveform = 4 pages	
17		FP to Flash Write_Start_Address_Trigger	Write 1 to trigger , 0 to reset (rearm trigger)	Trigger Start of block address to FPGA	
18		Flash operation Status Request	Ask for cyclic flash operation status update	FPGA returns 1/0 for pending/no pending operation. Cyclic	
19			Trigger reg 0x1B value	Seen only in startup sequence	To be identified. Low priority
1A			? Answer of request from reg 0x10	Seen only in startup sequence	To be identified. Low priority
1B			0 to F? : Write 16 parameters. Parameters Initialization ?	Seen only in startup sequence	To be identified. Low priority
1C	1	Manual Source for FSK/ASK/PSK/BURST	0= Start, 1=Stop	For burst :Write 0 followed by 1 immediately	
1D	1	Modulation Source & Burst Number	Reg 0x1D = 00AB BBBB A = FSK / ASK / PSK / BURST Source 0 = FSK / ASK / PSK / BURST Not Selected 1 = CH2 2 = Ext.(AC) 3 = MANU 4 = Ext.(DC) B BBBB= Burst Numbers = 1 to F4240 (1 to 1 000 000)	Set FSK/ASK/PSK /Burst Source + Burst number	
1E	Input	Measure status Request	Read 1 for Frequency available Read 2 for not data available Read 3 for min/max available		To be checked
1F					
20					
21	1	Pulse Width	10ns = 2, 4 000 000 000 ns = 3B9A CA00 -> 1 step = 4 ns	CH1 Only	
22	1	FSK HOP/ FM BIAS FreqLSW	Freq =100000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
23	1	FSK HOP/ FM BIAS FreqMSW	Freq =100000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
24	1	Modulation Mode	No Modulation = 10 0:BURST = 10, Burst Number (Reg 0x1D) then 0 1:PSK = 1 two times 2:FSK = 2, Hop frequency(Reg 0x23 & 0x22) then 82 4:ASK = 4 two times 8:AM with CH2 source = 8, Mod Rate(Reg 0x36) then 8 18:AM with EXT. (VCO-IN) source = 18, Mod Rate(Reg 0x36) then 18 20/A0:FM with CH2 source = 20 two times, FM BIAS (Reg 0x23 & 0x22) then A0 two times 30/B0:FM with EXT. (VCO-IN) source = 30 two times, FM BIAS (Reg 0x23 & 0x22) then B0 two times 40:PM with CH2 source = 40, PM BIAS (Reg 0x3A) then 40 50:PM with EXT. (VCO-IN) source = 50, PM BIAS (Reg 0x3A) then 50	2 identical writes looks useless for some modes	
25			Written with 0x02FA F080 (= 50 000 000)	Seen only in startup sequence	To be identified. Low priority
26			Written with 0x1DCD 6500 (= 500 000 000)	Seen only in startup sequence	To be identified. Low priority
27			Written with 0x01	Seen only in startup sequence	To be identified. Low priority
28			Written with 0x2A05 F200	Seen only in startup sequence	To be identified. Low priority
29			Written with 0xE35F	Seen only in startup sequence	To be identified. Low priority
2A			Written with 0xA931 A000	Seen only in startup sequence	To be identified. Low priority
2B	1	OffsetDW	Voltage DC	Low Range : OffsetDW=2047+(4094/0,62)*Offset Mid Range : OffsetDW=2047+(4094/6,21)*Offset High Range : OffsetDW=2047+(4094/24)*Offset	4094 is a best match but not logical (DAC has 4096 steps)
2C	2	OffsetDW	Voltage DC	Low Range : OffsetDW=2047+(4094/0,62)*Offset Mid Range : OffsetDW=2047+(4094/6,21)*Offset High Range : OffsetDW=2047+(4094/24)*Offset	4094 is a best match but not logical (DAC has 4096 steps)
2D	1	AmpDW	LowRange: Amp=0.5xAmpDW/3685 Mid Range: Amp=5xAmpDW/3685 High Range: Amp=20xAmpDW/3685	Low Range: AmpDW=Amp*3685/0,5 Mid Range: AmpDW=Amp*3685/5 High Range: AmpDW=Amp*3685/20	Just for offset = 0. Ranges depend on offset value too
2E	2	AmpDW	LowRange: Amp=0.5xAmpDW/3685 Mid Range: Amp=5xAmpDW/3685 High Range: Amp=20xAmpDW/3685	Low Range: AmpDW=Amp*3685/0,5 Mid Range: AmpDW=Amp*3685/5 High Range: AmpDW=Amp*3685/20	Just for offset = 0. Ranges depend on offset value too
2F	1	DutyDW	0.000%= 0, 100.000% = 1FFFF		
30	2	DutyDW	0.000%= 0, 100.000% = 1FFFF		
31					
32					
33					
34					
35					
36	1	Modulation AM Mod.Rate	0.0%=0, 100.0% = 3FFF		
37	1,2	Phase Trigger	Write 1 to trigger , 0 to reset (rearm trigger)	Written after Phase update	
38	1	Square Wave: Rise time /Fall time	0b0000RRRR RRRRRRRR RRFFFFFF FFFFFFFF Min = 4ns-> 0b00RR RRRR RRRR RRRR= 0x3FFF Max = 10 000ns-> 0b00RR RRRR RRRR RRRR= 0x0006	0b00RR RRRR RRRR RRRR=ENT(65532/Rise) 0b00FF FFFF FFFF FFFF=ENT(65532/Fall)	Multiple of 4ns, default=8ns Stored on 14 bits
39	2	Square Wave Rise time /Fall time	0b0000RRRR RRRRRRRR RRFFFFFF FFFFFFFF Min = 4ns-> 0b00RR RRRR RRRR RRRR= 0x3FFF Max = 10 000ns-> 0b00RR RRRR RRRR RRRR= 0x0006	0b00RR RRRR RRRR RRRR=ENT(65532/Rise) 0b00FF FFFF FFFF FFFF=ENT(65532/Fall)	Multiple of 4ns, default=8ns
3A	1	Modulation: PM BIAS	0.00°=0, 360.00° = 1FFFE		