FY6600 Registers Overview

2018/01/29

Reg.	Purpose				
HEX	Channel	Function	Comment 1	Comment 2	Action
1	1	FreqLSW	CH1 Freq =100 000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
2	1	FreqMSW	CH1 Freq =100 000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
3	2	FreqLSW	CH2 Freq =100 000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
4	2	FreqMSW	CH2 Freq =100 000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
5	1,2	Channel state	bit2 = CH2=ON/OFF (0/1) bit3 = ? bit5 = CH1 ON/OFF (0/1)	Reg 0x05 = 8 at some point. To be checked	
6	1,2	Relays Control + Config bits	Bit 0 = CH2 JD3 Relay ON/OFF (0/1) Bit 1 = CH2 JD1 Relay ON/OFF (0/1) Bit 2 = CH1 JD4 Relay ON/OFF (0/1) Bit 3 = CH1 JD2 Relay ON/OFF (0/1) Bit 4 = AC/DC Input Coupled Mode (0/1) Bit 5 = Uplink ON/OFF (0/1) Bit 6 = Uplink Mode Master/Slave (0/1)	Bit5 & Bit6 seem to be linked strangely: To be checked	
8	1	PhaseDW	Phase = 360*(1-PhaseDW/1048575)	PhaseDW=(1-Phase/360)*1048575	
9	2	PhaseDW	Phase = 360*(1-PhaseDW/1048575)	PhaseDW=(1-Phase/360)*1048575	
A					
B					
C	Input	Input_measure_Request value	01 = ? 03 = Request Frequency 07 = Request counter 0B = Request +WIDE 0F = ? 1B = Request -WIDE 1A = ? 1E = ? 1F = ?	Work in progress	
D	Input	Input_measure_Requested value	Read value requested by Reg 0x0C		
E	1,2	Flash to FP Read_Value_Read	Return one single value read from flash (one waveform sample but not only)	Address has to be written in reg0x12 before and triggered with Reg 0x15	
F	1,2	Flash to FP Read_Trigger	Write 1 to trigger Read then write 0 (Reset Trigger)		
10			Request with value from 0 to F written then read reg 0x1A: Read 16 parameters	Seen only in startup sequence	To be identified. Low priority
11	1,2	Flash to FPGA Read_Channel Number	CH1=1 , CH2=2, 0=?	Set which channel to load the Waveform for	
12	1,2	Memory Address	Waveform Sample Memory address	Set value in register and read reg 0x0E	
13	1,2	Flash to FPGA Read_Trigger	Write 1 to trigger Read then write 0 (Reset Trigger)		
14		FP to Flash Write_Trigger	write 1 to trigger , 0 to reset (rearm trigger)	Written with 0 before flash read operation	
15		FP to Flash Write_Value	Value to write to Flash		
16		FP to Flash Write_Page_Erase_Trigger	Write 1 to trigger , 0 to reset (rearm trigger)	Reg0x12 contains address of page to be erased. 1 waveform = 4 pages	
17		FP to Flash Write_Start_Address_Trigger	Write 1 to trigger , 0 to reset (rearm trigger)	Trigger Start of block address to FPGA	
18		Flash operation Status Request	Ask for cyclic flash operation status update	FPGA returns 1/0 for pending/no pending operation. Cyclic	
19			Trigger reg 0x1B value	Seen only in startup sequence	To be identified. Low priority
1A			? Answer of request from reg 0x10	Seen only in startup sequence	To be identified. Low priority
1B			0 to F? : Write 16 parameters. Parameters Initialization ?	Seen only in startup sequence	To be identified. Low priority
1C	1	Manual Source for FSK/ASK/PSK/BURST	0= Start, 1=Stop	For burst :Write 0 followed by 1 immediately	
1D	1	Modulation Source & Burst Number	Reg 0x1D = 00AB BBBB A = FSK / ASK / PSK / BURST Source 0 = FSK / ASK / PSK / BURST Not Selected 1 = CH2 2 = Ext.(AC) 3 = MANU 4 = Ext.(DC) B BBBB= Burst Numbers = 1 to F4240 (1 to 1 000 000)	Set FSK/ASK/PSK /Burst Source + Burst number	
1E	Input	Measure status Request	Read 1 for Frequency available Read 2 for not data available Read 3 for min/max available		To be checked
1F					
20					
21	1	Pulse Width	10ns = 2, 4 000 000 000 ns = 3B9A CA00 -> 1 step = 4 ns	CH1 Only	
22	1	FSK HOP/ FM BIAS FreqLSW	Freq =100000*FreqMSW + FreqLSW µHz	FreqMSW = ENT(Freq/100 000)	
23	1	FSK HOP/ FM BIAS FreqMSW	Freq =100000*FreqMSW + FreqLSW µHz	FreqLSW = Freq - 100 000*FreqMSW	
24	1	Modulation Mode	No Modulation = 0 PSK = 1 two times FSK = 2, Hop frequency(Reg 0x23 & 0x22) then 82 ASK = 4 two times AM with CH2 source = 8, Mod Rate(Reg 0x36) then 8 AM with EXT. (VCO-IN) source = 18, Mod Rate(Reg 0x36) then 18 BURST = 10, Burst Number (Reg 0x1D) then 0 FM with CH2 source = 20 two times, FM BIAS (Reg 0x23 & 0x22) then A0 two times FM with EXT. (VCO-IN) source = 30 two times, FM BIAS (Reg 0x23 & 0x22) then B0 two times PM with CH2 source = 40, PM BIAS (Reg 0x3A) then 40 PM with EXT. (VCO-IN) source = 50, PM BIAS (Reg 0x3A) then 50	2 identical writes looks useless for some modes	
25			Written with 0x02FA F080 (= 50 000 000)	Seen only in startup sequence	To be identified. Low priority
26			Written with 0x1DCD 6500 (= 500 000 000)	Seen only in startup sequence	To be identified. Low priority
27			Written with 0x01	Seen only in startup sequence	To be identified. Low priority
28			Written with 0x2A05 F200	Seen only in startup sequence	To be identified. Low priority
29			Written with 0xE35F	Seen only in startup sequence	To be identified. Low priority
2A			Written with 0xA931 A000	Seen only in startup sequence	To be identified. Low priority
2B	1	OffsetDW		[-1V;1V] : OffestDW=2047+(4094/6,21)*Offset outside]-1;1V[: OffsetDW=2047+(4094/24)*Offset	4094 is a best match but not logical (DAC has 4096 steps)
2C	2	OffsetDW			
2D	1	AmpDW	[0V;0.5000V]: Amp=0.5xAmpDW/3685 [0.5001V;5.0000V]: Amp=5xAmpDW/3685 [5.0001V;20.0000V]: Amp=20xAmpDW/3685	[0V;0.5000V]: AmpDW=Amp*3685/0,5 [0.5001V;5.0000V]: AmpDW=Amp*3685/5 [5.0001V;20.0000V]: AmpDW=Amp*3685/20	Just for offset = 0. Ranges depend on offset value too
2E	2	AmpDW	[0V;0.5000V]: Amp=0.5xAmpDW/3685 [0.5001V;5.0000V]: Amp=5xAmpDW/3685 [5.0001V;20.0000V]: Amp=20xAmpDW/3685	[0V;0.5000V]: AmpDW=Amp*3685/0,5 [0.5001V;5.0000V]: AmpDW=Amp*3685/5 [5.0001V;20.0000V]: AmpDW=Amp*3685/20	Just for offset = 0. Ranges depend on offset value too
2F	1	DutyDW	0.000%= 0, 100.000% = 1FFFF		
30	2	DutyDW	0.000%= 0, 100.000% = 1FFFF		
31					
32					
33					
34					
35					
36	1	Modulation AM Mod.Rate	0.0%=0, 100.0% = 3FFF		
37					
38			Written with 7FF DFFF	written after Reg 0x05 Channel state	To be identified
39			Written with 7FF DFFF	written after Reg 0x05 Channel state	To be identified
3A	1	Modulation: PM BIAS	0.00°=0, 360.00° = 1FFFE		