1.5.2.1 IC113, IC114, and IC115 and their associated components form the microprocessor interface to modulation control circuitry. Decoder IC113 processes the clock signals (clock, clock selects 0 - 2, and clock enable) from the microprocessor (P104, pins 9, and 1 - 4, respectively) to generate control clocks 0 - 4, the output at pin 10 (Y5), and the strobe signal to the various shift registers shown on the schematic. Control data from the microprocessor (P104, pin 8) is fed simultaneously to each of the shift registers (IC114, IC118, IC119, IC121, IC122, IC124, IC125, and IC127) and clocked bit by bit into a particular register(s) at each pulse of the appropriate clock. The serial data input is transferred into parallel data at the shift register outputs and is latched by the strobe signal.

1.5.2.2 IC115 is an 8 input Nor gate that receives error signals from the Oscillator Assembly circuitry (Main Loop Unlock, LO Loop Unlock, Over Deviation; J101) and Amplifier Assembly (Unlevel; J102) as shown and generates an interrupt request ($\overline{\text{FDB IRQ}}$) to the microprocessor if an error occurs. The output at pin 13 of IC115 is high (logic 1) during normal operation. Input lines to IC115 are low (logic 0). A +5 volt error signal input causes the output ($\overline{\text{FDB IRQ}}$) to go low. Error signals are discussed in the Oscillator Assembly theory of operation (Sections 1.5.7 and 1.5.8). Error signals are also stored in shift register IC114 so that the microprocessor can interrogate the register to determine exactly which error generated the interrupt request (FDB DATA line; pin 3 of IC114 to pin 5 of P104). The 400 Hz test signal input A from the Mod Source/Ref Freq circuitry (Figure 4-2) to pin 1 of IC114 (on Figure 4-3) provides a test signal that also is fed back to the microprocessor (to verify the 400 Hz circuitry as part of the power-up test procedure described in Section 5.5 of the Operating Manual).

1.5.2.3 The AM signal (Reference Point "A") used to amplitude modulate the carrier comes from pin 7 (internal AM) or pin 2 (external AM) of IC130. It is applied through J1304 (pin 1) to the Carrier Level Circuitry on the Doubler Control Board (see Section 1.5.14.2). The AM drive signal from the Carrier Level Circuitry on the Doubler Control Board (J1304, pin 3 of the Main Board) is applied through reference point "C" and J102, pin 3 to the Amplifier Assembly (see Section 1.5.11.1). The AM LEVEL GRN signal from J1304, pin 4 to reference point "D" and J102, pin 4 (to the Amplifier Assembly) ensures that the AM/Level drive signal has the same reference on the Doubler Control Board and Amplifier Assembly.

1.5.2.4 The instrument RF output level is the product of the carrier level/AM drive output at pin 3 of J102 (from the Doubler Control board as described above) and the programmable attenuator controlled by the outputs at pins 3-6 of shift register IC119. These control outputs are sent to Attenuator Driver IC129, which provides +12 volt outputs (powered by regulator IC135) to the Attenuator pad network identified at P103. Attenuator pads are energized as required by the +12 volt signals from IC129. For example, inserting thirty dB of attenuation will result in +12 volt levels at pins 1 and 2 of P103. When the maximum attenuation of 130 dB is realized, pins 1 - 6 of P103 will each have 12 volts applied.

1.5.2.5 Part of the reverse power protection circuitry is shown in Figure 4-3. The actuating signal comes from the reverse power detector in the Programmable Attenuator (see Section 1.5.18) through P8 of P103. It goes from reference point "B" to J1304, pin 2 to the Doubler Control Board (see Section 1.5.14.3). This signal is compared to a reference voltage (on the doubler control board) and it is there that a "trip" signal is generated, if necessary. The trip signal (a high;+5V)