

maining column inputs to IC813 (pins 14, 3, 4, and 5) will be high. The status of the column input lines will be clocked out of IC813 (pin 9) by the keyboard out clock at pin 2 in a serial stream back to the microprocessor to identify the row.

1.5.17.4 If the pressed switch had been in row 2 (S12, for example), setting row 0 or row 1 (or rows 3 - 7) at a logic "0" will not allow a low to be input to IC813. All "1"s will be input because column 3 in which S12 is located will be set at "1" by the microprocessor while columns 2 and 4 - 6 will be high because of the +5 volt pull-up resistors (RN806). The microprocessor will sequentially clock the "0" and seven "1"s in 8-bit bytes (as shown on Figure 4-18) onto the rows until the row in which the pressed switch is located is identified.

1.5.17.5 The column in which the switch is located will be found by setting all row outputs from IC812 equal to a logic "0" and reading the single column at which the low appears into IC813 (either pin 13, 14, 3, 4, or 5). Column information also is provided as an 8-bit byte of data. The pull-up resistor network will maintain highs (logic 1) at all column inputs except the one with the closed (pressed) switch (which will be connected to the one of the lows out of IC812).

1.5.17.6 The 8-bit bytes used to identify the row and column in which each switch is located are shown in a table on Figure 4-18.

1.5.17.7 When pressed, the cursor keys (\uparrow \downarrow) shown as switches S41 and S42 on Figure 4-18 supply a high (+5 V) to pin 5 or pin 6, respectively, of PAL IC811 (Figure 4-17). The +5 volt supplied comes from pin 15 of J803 through either closed switch. The PAL (IC811) decodes the up/down cursor inputs, the KBD IN CLK and KBD DATA OUT signals (see Section 1.5.17.3), and generates the $\overline{\text{UP/DOWN}}$ signal at pin 18 and the KBD DATA IN signal at pin 19.

1.5.18 PROGRAMMABLE ATTENUATOR

The programmable attenuator (see Figure 1-15) contains six attenuator pads, a reverse power detector, and a reverse power relay (breaker). The RF in signal from J600 of the RF Amplifier Module goes through the pad network selected by control signals from the microprocessor via main board P103 (see Section 1.5.2.4) into and through the attenuator relay.

1.5.18.1 The relay is held on by a +12 volt signal (S1) from the reverse power protection circuit on the main board (see Section 1.5.2.5). RF out of the relay is fed to the RF out connector on the 2520 front panel.

1.5.18.2 If an RF power source is inadvertently attached to the RF output, the reverse power detector detects the input and sends a signal to the reverse power protection circuit to trigger the circuit as described in Section 1.5.2.5.

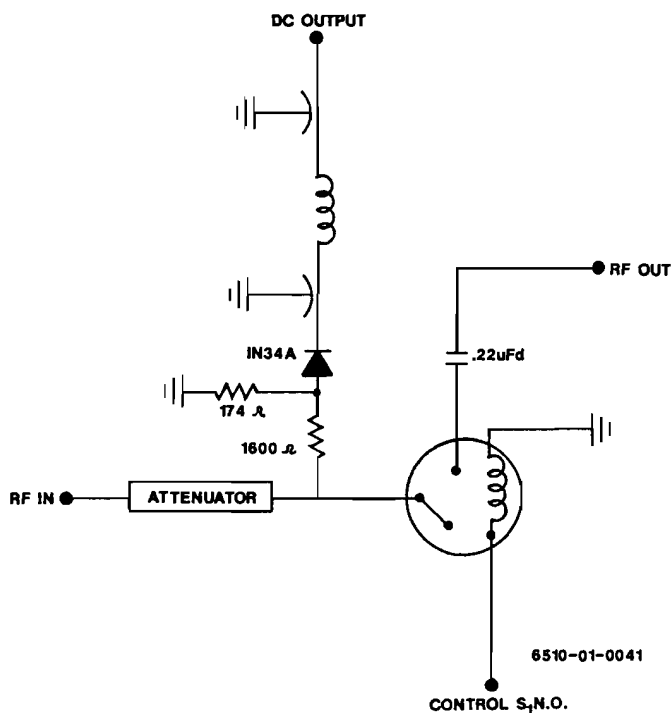


Figure 1-15. Schematic, Programmable Attenuator