reference point "E" to pin 5 of J1304 and then to the Doubler Control Board (see Section 1.5.14.2) for processing. The processed signal is returned to the main board at J1304, pin 6 where it is routed to reference point "F" and then shift register IC114, pin 7, to select the unlevel error signal (either Amplifier or Doubler Unlevel).

1.5.2.14 Output lines "H" and "I" (to sheet 4) are Mode Control lines used only with the FSK Modulator Option. Documentation for the FSK Modulator Option is provided separate to this manual.

1.5.3 MAIN BOARD, FREQ DIV/CONTROL

The Main Board Freq Div/Control schematic (Figure 4-4) shows the Single Side Band (SSB) Mixer, Main Loop Fractional Frequency Divider and its Fraction Control Section, the pulse stretcher network, the Local Oscillator Divider (÷ 500), and the shift registers associated with Oscillator and Amplifier Assembly Control signals.

Figure 1-5 shows the Main Phase Locked Loop (PLL) in block diagram form. The SSB and Main PLL divider circuits are detailed in Figure 4-4. The Direct Digital Synthesis (DDS) circuitry is shown in Figure 4-5. The remaining blocks in Figure 1-5 are described with the Oscillator Assembly (Sections 1.5.7 and 1.5.8).

1.5.3.1 The Single Side Band (SSB) Mixer MX401 (see Figure 4-4) receives input signals from the Oscillator Assembly (from J401 to pin 16 of the SSB mixer) and the Direct Digital Synthesis (DDS) section (at pins 4 and 13 of the SSB mixer). The 275 - 550 MHz fundamental band signal (f_o) from the Oscillator Assembly is mixed with the two identical frequency (but 90° out of phase) 100 - 199.999 kHz signals (f_{DDS}) from the DDS section. Mixed frequency signals (f_{mix}) that are the sum and difference of the two input signals are produced. The relationship is:

$$f_{mix} = f_o \pm f_{DDS}$$

Conversion loss for the lower sideband (the difference of the frequencies) is about 9 dB. Upper sideband (the sum of the frequencies) rejection is an additional 15 dB from the lower sideband. In effect, the lower sideband is passed through to the Main Loop Frequency Divider (from pin 1 of the SSB mixer) while the upper sideband is eliminated.

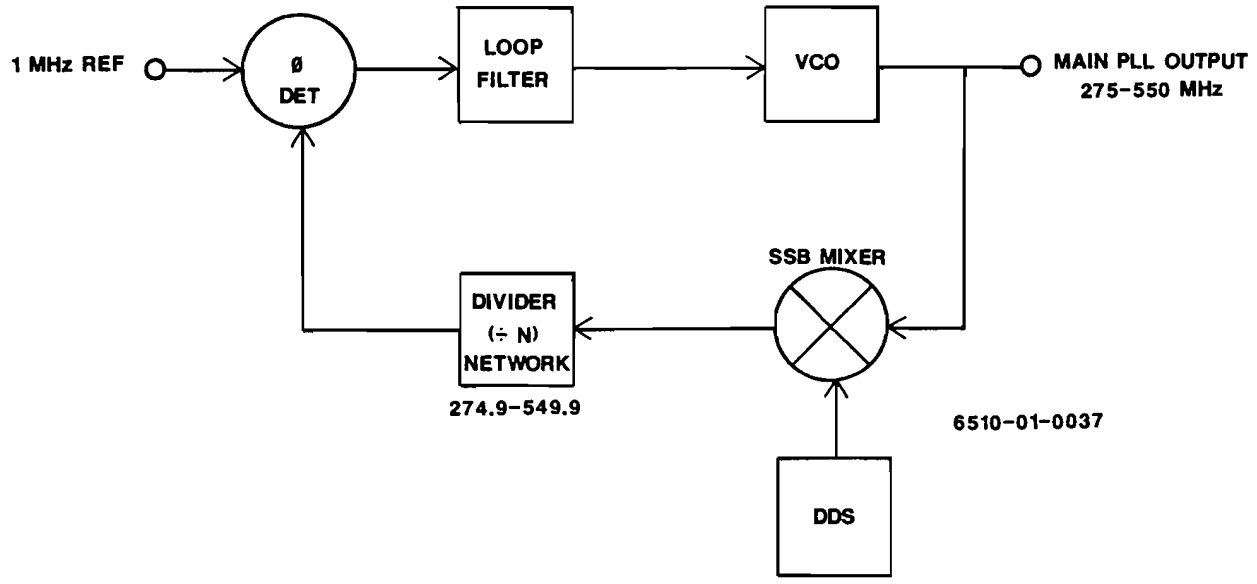

Figure 1-5. Block Diagram, VCO Main Phase Locked Loop (PLL)