

MODEL NAME : *DDP00*  
*DDB00*

PCB NO : *LA-G341P*

BOM P/N :

# Dell/Compal Confidential

## Schematic Document

### Superveloce

#### (Berlinetta CFL 4-Phase Design)

2018-05-10

Rev: Pilot A00

@ : Nopop Component

XDP@ : Nopop Component

CONN@ : Connector Component

TPM@ : TPM funct i on

EMC@ : Pop of EMI parts

VRAMS@ : Samsung GDDR5

VRAMM@ : Micron GDDR5

G0VRAMH@: Samsung GDDR5 for G0-GPU

NDS@@ : Nopop Component

N18PQ1@ : GPU N18PQ1

N18PQ3@ : GPU N18PQ3

N17PG0@ : GPU N17PG0

N17PG1@ : GPU N17PG1

UMA@ : UMA

DIS@ : DIS

UMAP@ : UMA for Presist i on

UMAX@ : UMA for XPS

3PHASEPCB@ : PCB for 3Phase

4PHASEPCB@ : PCB for 4Phase

3PHASE@ : PCB for 3Phase

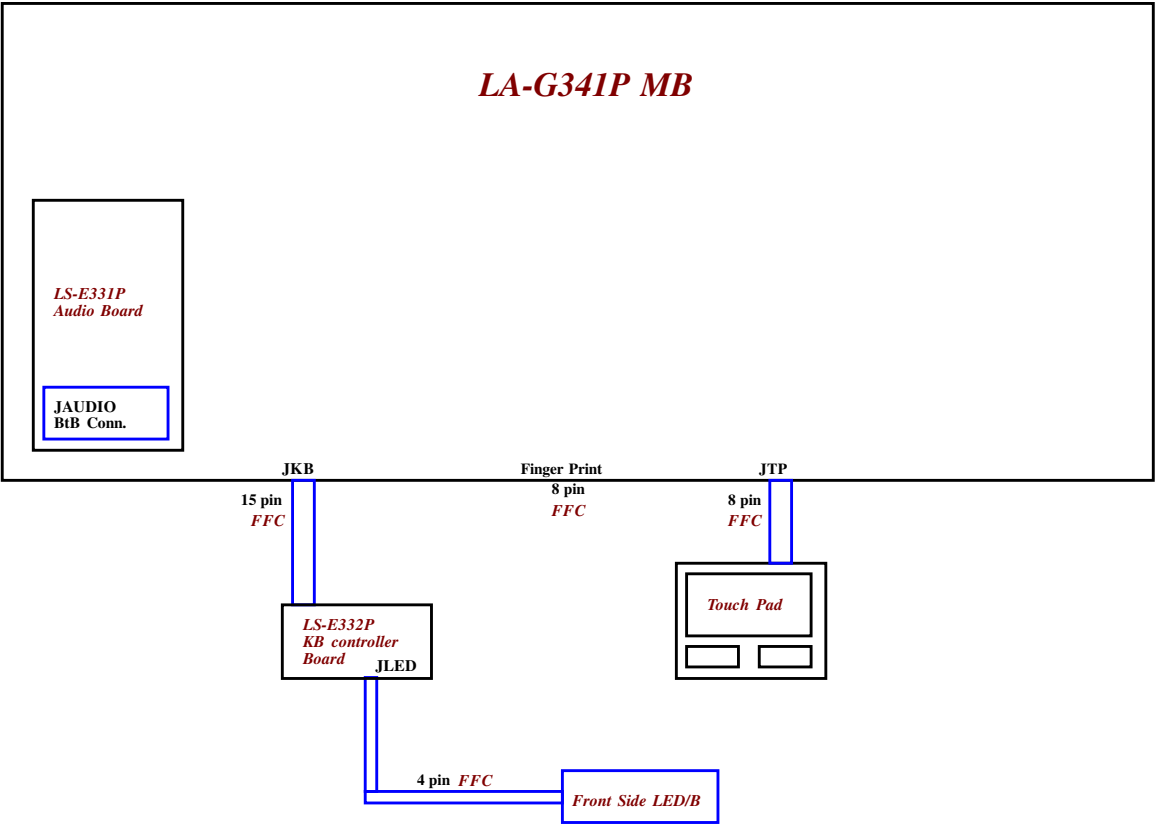
4PHASE@ : PCB for 4Phase

VPRO@ : For VPRO SKU

NVPRO@ : For No-VPRO SKU

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				Document Number	
				Rev	
				LA-G341P	
				Date: Wednesday, June 06, 2018	
				Sheet 1 of 78	





Board ID	Resistor
X00	4.3K
X01	2K
X02	
X03	
A00	1K

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	Touch Screen
10	None
11	None
12	RGB CAMERA

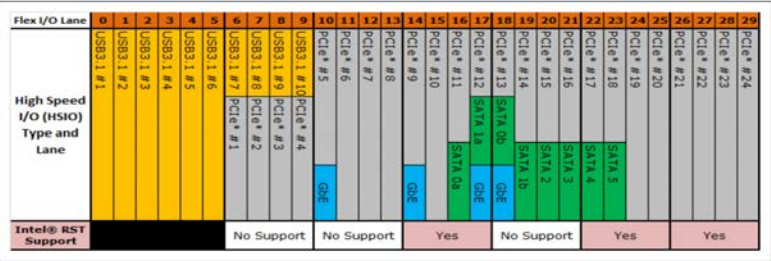
USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	CARD READER		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	2	HDD
Lane 16	None	3	N/A
Lane 17	Alpine Ridge	4	N/A
Lane 18		5	N/A
Lane 19			
Lane 20			

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

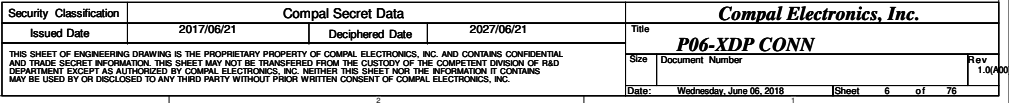


The 30 HSD lanes on PCB-H supports the following configurations:

- Up to 24 PCIe\* Lanes
- A maximum of 16 PCIe\* Ports (or devices) can be enabled
- When a QM Port is enabled, the maximum number of PCIe\* Ports (or devices) that can be enabled reduces based off the following:
  - Max PCIe\* Ports (or devices) = 16 - QM (0 or 1)
  - PCIe\* Lanes 1-4 (PCIe\* Controller #1), 5-8 (PCIe\* Controller #2), 9-12 (PCIe\* Controller #3), 13-16 (PCIe\* Controller #4), 17-20 (PCIe\* Controller #5), and 21-24 (PCIe\* Controller #6) can be individually configured
- Up to 6 SATA Lanes
  - A maximum of 6 SATA Ports (or devices) can be enabled
  - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
  - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
  - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
  - Up to 4 QM Lanes
    - A maximum of 1 QM Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe\* storage devices
  - #2 and #4 PCIe\* NVMe SSD
  - #2 Intel® Optane® Memory Device
  - See the "PCI Express" (PCIe\*) chapter for the 8 ON PCIe\* Controllers configuration, and Lanes that can be used for Intel® Rapid Storage Technology PCIe\* storage support
- For unused SATA/PCIe\* Combo Lanes, Flex I/O Lanes that can be configured as PCIe\* or SATA, the lanes must be statically assigned to SATA or PCIe\* via the SATA/PCIe Combo Port Software discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

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		Size	Document Number
		Date	Wednesday, June 06, 2018
		Sheet	4 of 76





<23> PEG\_HTX\_C\_GRX\_P0\_15] << PEG\_HTX\_C\_GRX\_P0\_15] << PEG\_HTX\_C\_GRX\_N0\_15] << PEG\_HTX\_C\_GRX\_P14 << PEG\_HTX\_C\_GRX\_N14 << PEG\_HTX\_C\_GRX\_P13 << PEG\_HTX\_C\_GRX\_N13 << PEG\_HTX\_C\_GRX\_P12 << PEG\_HTX\_C\_GRX\_N12 << PEG\_HTX\_C\_GRX\_P11 << PEG\_HTX\_C\_GRX\_N11 << PEG\_HTX\_C\_GRX\_P10 << PEG\_HTX\_C\_GRX\_N10 << PEG\_HTX\_C\_GRX\_P9 << PEG\_HTX\_C\_GRX\_N9 << PEG\_HTX\_C\_GRX\_P8 << PEG\_HTX\_C\_GRX\_N8 << PEG\_HTX\_C\_GRX\_P7 << PEG\_HTX\_C\_GRX\_N7 << PEG\_HTX\_C\_GRX\_P6 << PEG\_HTX\_C\_GRX\_N6 << PEG\_HTX\_C\_GRX\_P5 << PEG\_HTX\_C\_GRX\_N5 << PEG\_HTX\_C\_GRX\_P4 << PEG\_HTX\_C\_GRX\_N4 << PEG\_HTX\_C\_GRX\_P3 << PEG\_HTX\_C\_GRX\_N3 << PEG\_HTX\_C\_GRX\_P2 << PEG\_HTX\_C\_GRX\_N2 << PEG\_HTX\_C\_GRX\_P1 << PEG\_HTX\_C\_GRX\_N1 << PEG\_HTX\_C\_GRX\_P0 << PEG\_HTX\_C\_GRX\_N0

+VCCIO

RH24

<18> DMI\_CRX\_PTX\_P0 << DMI\_CRX\_PTX\_N0 <18> DMI\_CRX\_PTX\_P1 << DMI\_CRX\_PTX\_N1 <18> DMI\_CRX\_PTX\_P2 << DMI\_CRX\_PTX\_N2 <18> DMI\_CRX\_PTX\_P3 << DMI\_CRX\_PTX\_N3

To Alpine Ridge

To Alpine Ridge

To DP to HDMI Converter (DM1/P5175B2)

PEG\_GTX\_C\_HRX\_P15 E26 PEG\_GTX\_C\_HRX\_N15 D25 PEG\_GTX\_C\_HRX\_P14 E24 PEG\_GTX\_C\_HRX\_N14 D24 PEG\_GTX\_C\_HRX\_P13 E23 PEG\_GTX\_C\_HRX\_N13 D23 PEG\_GTX\_C\_HRX\_P12 E22 PEG\_GTX\_C\_HRX\_N12 D22 PEG\_GTX\_C\_HRX\_P11 E21 PEG\_GTX\_C\_HRX\_N11 D21 PEG\_GTX\_C\_HRX\_P10 E20 PEG\_GTX\_C\_HRX\_N10 D20 PEG\_GTX\_C\_HRX\_P9 E19 PEG\_GTX\_C\_HRX\_N9 D19 PEG\_GTX\_C\_HRX\_P8 E18 PEG\_GTX\_C\_HRX\_N8 D18 PEG\_GTX\_C\_HRX\_P7 E17 PEG\_GTX\_C\_HRX\_N7 D17 PEG\_GTX\_C\_HRX\_P6 E16 PEG\_GTX\_C\_HRX\_N6 D16 PEG\_GTX\_C\_HRX\_P5 E15 PEG\_GTX\_C\_HRX\_N5 D15 PEG\_GTX\_C\_HRX\_P4 E14 PEG\_GTX\_C\_HRX\_N4 D14 PEG\_GTX\_C\_HRX\_P3 E13 PEG\_GTX\_C\_HRX\_N3 D13 PEG\_GTX\_C\_HRX\_P2 E12 PEG\_GTX\_C\_HRX\_N2 D12 PEG\_GTX\_C\_HRX\_P1 E11 PEG\_GTX\_C\_HRX\_N1 D11 PEG\_GTX\_C\_HRX\_P0 E10 PEG\_GTX\_C\_HRX\_N0 D10

PEG\_ROMP

<18> DMI\_CRX\_PTX\_P0 << DMI\_CRX\_PTX\_N0 <18> DMI\_CRX\_PTX\_P1 << DMI\_CRX\_PTX\_N1 <18> DMI\_CRX\_PTX\_P2 << DMI\_CRX\_PTX\_N2 <18> DMI\_CRX\_PTX\_P3 << DMI\_CRX\_PTX\_N3

Q32

PEG\_ROMP

Q32

Q32

Q32

Q32

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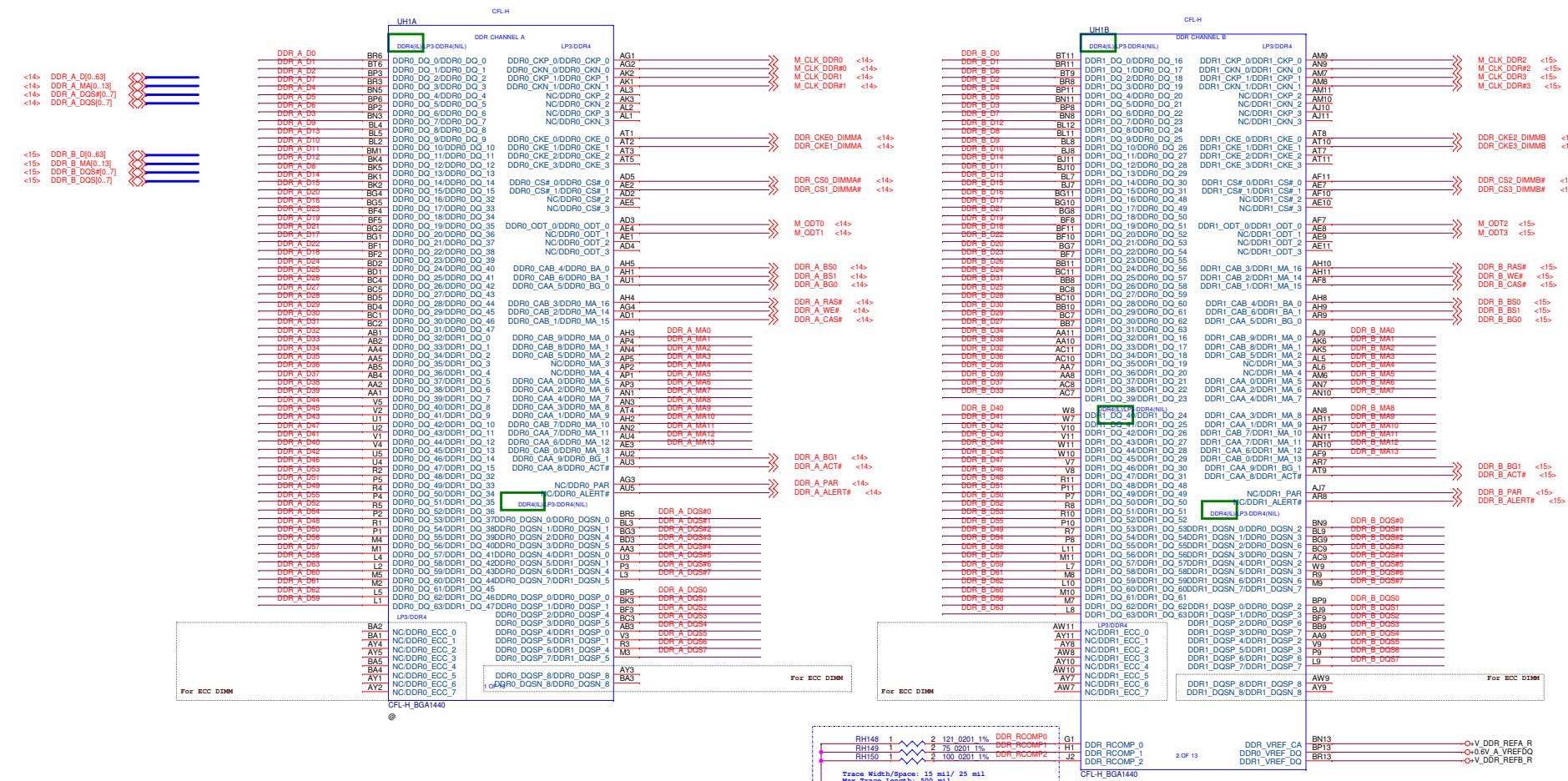
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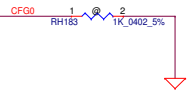
UHIIC



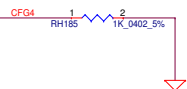


# CFG Straps for Processor

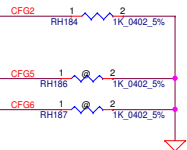
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall.  0 = Stall.



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port  * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion  0: PEG Wait for BIOS for training

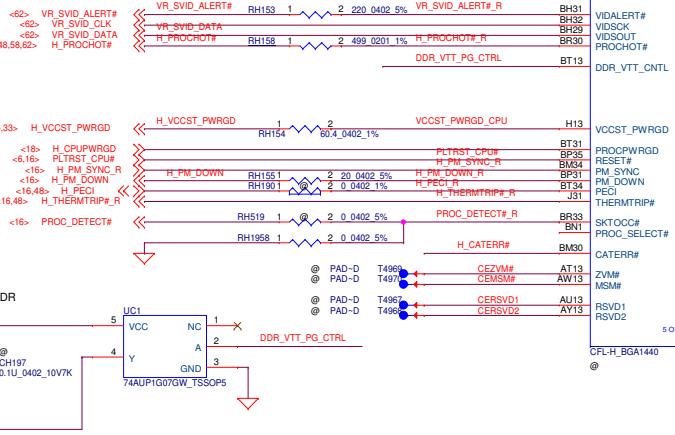
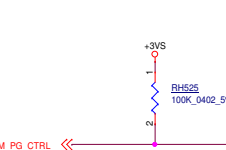
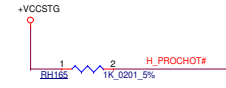
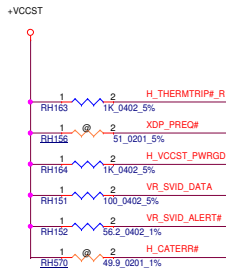


Table 2-13. PCI Express® Bifurcation and Lane Reversal Mapping

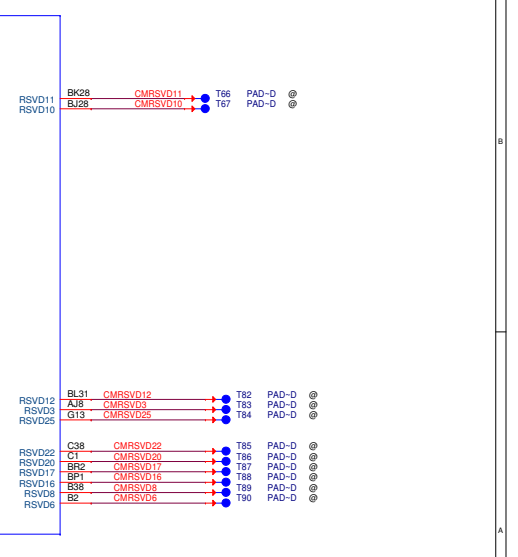
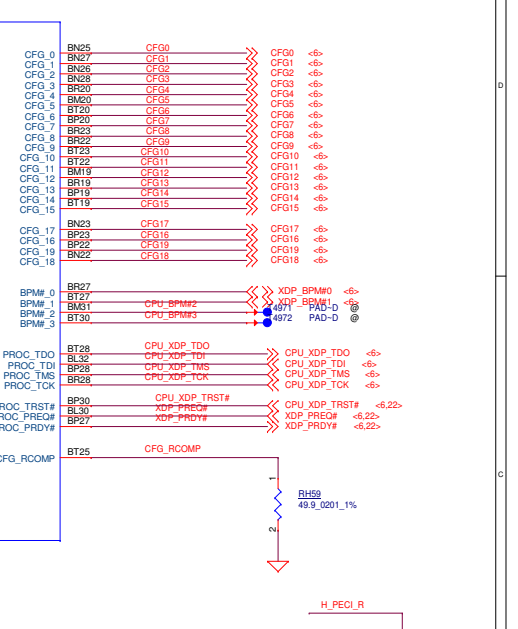
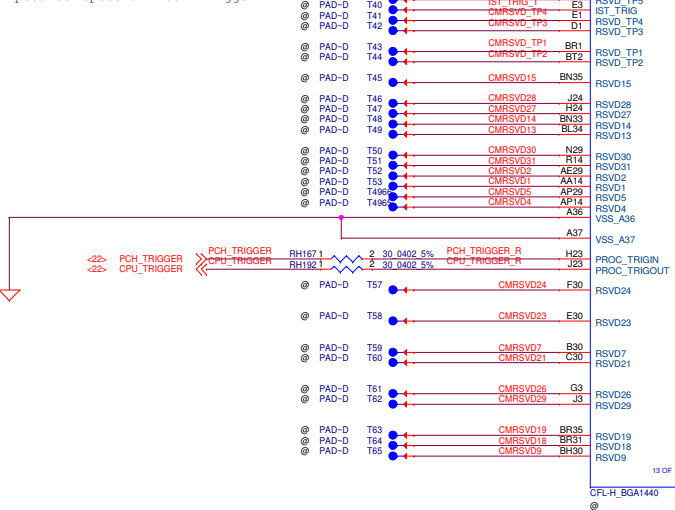
Bifurcation	Link Width			CFG Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10 <td>11</td> <td>12<td>13</td><td>14</td><td>15</td></td>	11	12 <td>13</td> <td>14</td> <td>15</td>	13	14	15
x16 reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8 reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7
x8+2x4 reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

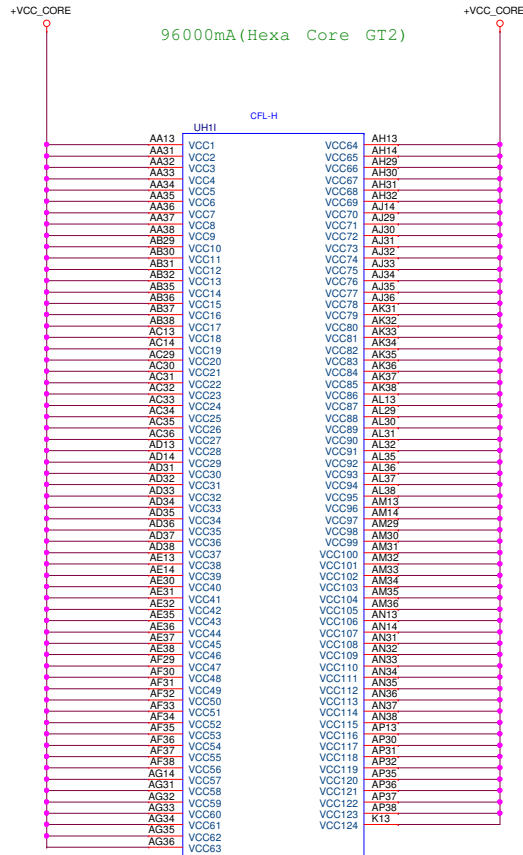
Notes:

- For CFG bus details, refer to Section 6.4.
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
  - Connect lane 0 of 1<sup>st</sup> device to lane 0.
  - Connect lane 0 of 2<sup>nd</sup> device to lane 5.
  - Connect lane 0 of 3<sup>rd</sup> device to lane 12.For example:
  - When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
  - When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lane device should use lanes 8:9.
  - When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
- for reversal lanes, for example:
  - When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
- For Basin Falls platform use 1x8+2x4 Bifurcation



Impedance Spectrum Tool Trigger





96000mA(Hexa Core GT2)

CFL-H

CFL-H\_BGA1440

9 OF 13 VCC\_SENSE  
VSS\_SENSE

+VCC\_CORE

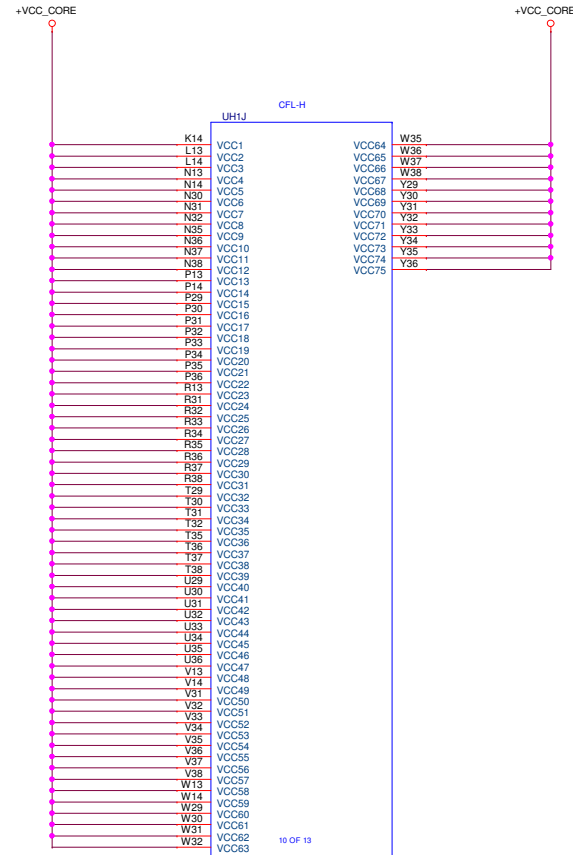
RH197  
100\_0402\_1%

RH198.1  
2 0.0402 1%

RH465.1  
2 0.0402 1%

RH466  
100\_0402\_1%

1. Vcc\_SENSE/ Vss\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU



CFL-H

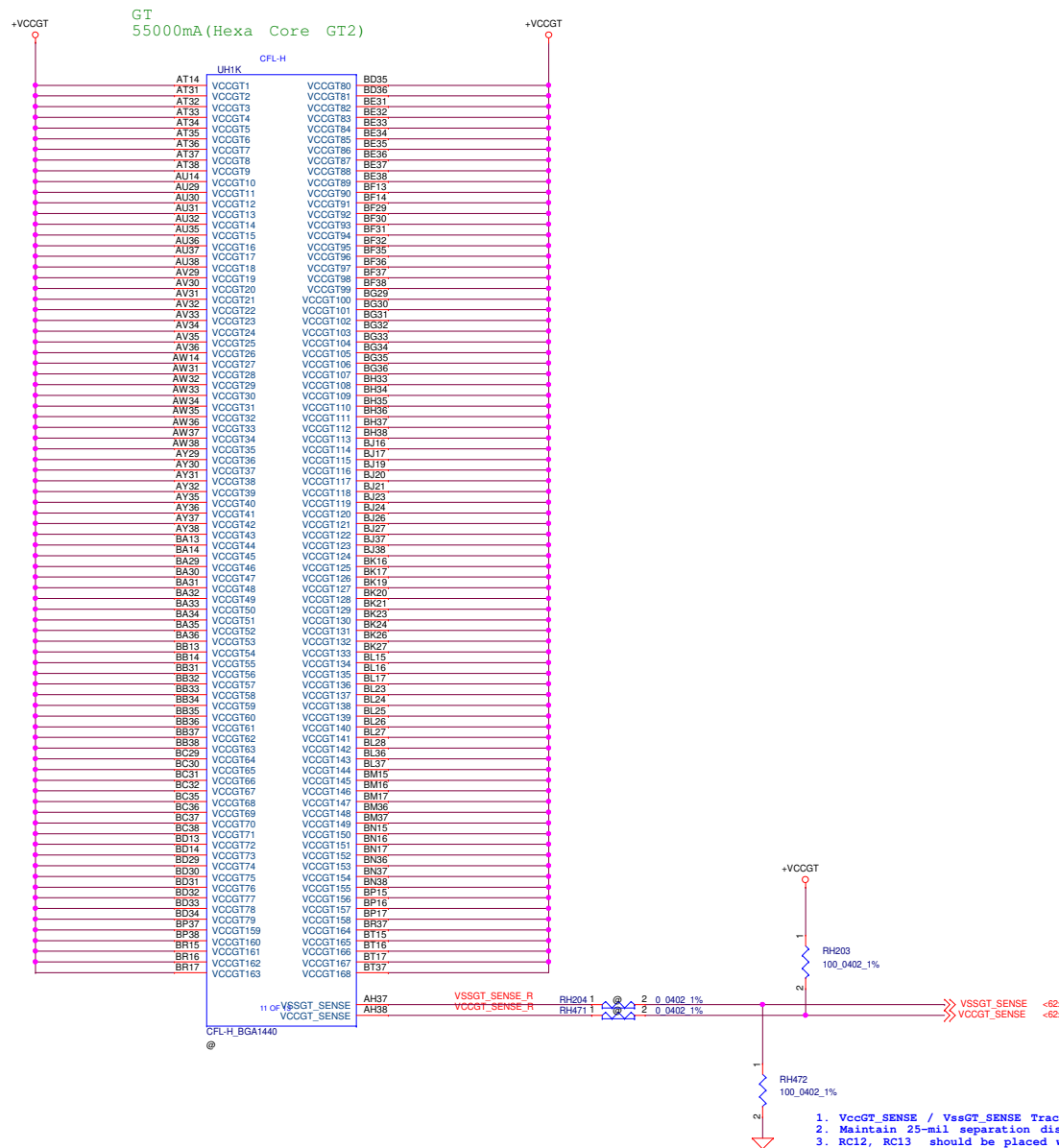
CFL-H\_BGA1440

10 OF 13

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								Size	Document	Number	Rev
								Custom			1.0/01
Date:		Wednesday, June 06, 2018				Sheet		10 of 76			





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Title		P12-CPU(6/7) PWR,VGT		
Size		Document Number		
Date		Wednesday, June 06, 2018		
Sheet		12 of 76		

CFL-H		
UH1F		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
A9	VSS_12	VSS_93
AA12	VSS_13	VSS_94
AA29	VSS_14	VSS_95
AA30	VSS_15	VSS_96
AB33	VSS_16	VSS_97
AB34	VSS_17	VSS_98
AB6	VSS_18	VSS_99
AC1	VSS_19	VSS_100
AC12	VSS_20	VSS_101
AC2	VSS_21	VSS_102
AC3	VSS_22	VSS_103
AC37	VSS_23	VSS_104
AC38	VSS_24	VSS_105
AC4	VSS_25	VSS_106
AC5	VSS_26	VSS_107
AC6	VSS_27	VSS_108
AD10	VSS_28	VSS_109
AD11	VSS_29	VSS_110
AD12	VSS_30	VSS_111
AD29	VSS_31	VSS_112
AD30	VSS_32	VSS_113
AD6	VSS_33	VSS_114
AD8	VSS_34	VSS_115
AD9	VSS_35	VSS_116
AE33	VSS_36	VSS_117
AE34	VSS_37	VSS_118
AE6	VSS_38	VSS_119
AF1	VSS_39	VSS_120
AF12	VSS_40	VSS_121
AF13	VSS_41	VSS_122
AF14	VSS_42	VSS_123
AF2	VSS_43	VSS_124
AF3	VSS_44	VSS_125
AF4	VSS_45	VSS_126
AG10	VSS_46	VSS_127
AG11	VSS_47	VSS_128
AG13	VSS_48	VSS_129
AG29	VSS_49	VSS_130
AG30	VSS_50	VSS_131
AG6	VSS_51	VSS_132
AG7	VSS_52	VSS_133
AG8	VSS_53	VSS_134
AH12	VSS_54	VSS_135
AH33	VSS_55	VSS_136
AH34	VSS_56	VSS_137
AH35	VSS_57	VSS_138
AH36	VSS_58	VSS_139
AH6	VSS_59	VSS_140
AJ1	VSS_60	VSS_141
AJ13	VSS_61	VSS_142
AJ2	VSS_62	VSS_143
AJ3	VSS_63	VSS_144
AJ37	VSS_64	VSS_145
AJ38	VSS_65	VSS_146
AJ4	VSS_66	VSS_147
AJ5	VSS_67	VSS_148
AJ6	VSS_68	VSS_149
W4	VSS_69	VSS_150
W5	VSS_70	VSS_151
Y10	VSS_71	VSS_152
Y11	VSS_72	VSS_153
Y13	VSS_73	VSS_154
Y14	VSS_74	VSS_155
Y37	VSS_75	VSS_156
Y38	VSS_76	VSS_157
Y7	VSS_77	VSS_158
Y8	VSS_78	VSS_159
Y9	VSS_79	VSS_160
AK29	VSS_80	VSS_161
AK30	VSS_81	VSS_162

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CFL-H		
UH1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B8	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA38	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB12	VSS_178	VSS_259
BB2	VSS_179	VSS_260
BB29	VSS_180	VSS_261
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BB30	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BB6	VSS_185	VSS_266
BC12	VSS_186	VSS_267
BC13	VSS_187	VSS_268
BC14	VSS_188	VSS_269
BC33	VSS_189	VSS_270
BC34	VSS_190	VSS_271
BC6	VSS_191	VSS_272
BD10	VSS_192	VSS_273
BD11	VSS_193	VSS_274
BD12	VSS_194	VSS_275
BD37	VSS_195	VSS_276
BD6	VSS_196	VSS_277
BD7	VSS_197	VSS_278
BD8	VSS_198	VSS_279
BD9	VSS_199	VSS_280
BE1	VSS_200	VSS_281
BE2	VSS_201	VSS_282
BE29	VSS_202	VSS_283
BE3	VSS_203	VSS_284
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BE4	VSS_205	VSS_286
BE5	VSS_206	VSS_287
BE6	VSS_207	VSS_288
BF12	VSS_208	VSS_289
BF33	VSS_209	VSS_290
BF34	VSS_210	VSS_291
BF6	VSS_211	VSS_292
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BG13	VSS_213	VSS_294
BG14	VSS_214	VSS_295
BG37	VSS_215	VSS_296
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BG6	VSS_217	VSS_298
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BH10	VSS_219	VSS_300
BH11	VSS_220	VSS_301
BH12	VSS_221	VSS_302
BH14	VSS_222	VSS_303
BH2	VSS_223	VSS_304
BH3	VSS_224	VSS_305
BH4	VSS_225	VSS_306
BH5	VSS_226	VSS_307
BH6	VSS_227	VSS_308
BH7	VSS_228	VSS_309
BH8	VSS_229	VSS_310
BH9	VSS_230	VSS_311
T2	VSS_231	VSS_312
T3	VSS_232	VSS_313
T33	VSS_233	VSS_314
T34	VSS_234	VSS_315
T4	VSS_235	VSS_316
T5	VSS_236	VSS_317
T7	VSS_237	VSS_318
T8	VSS_238	VSS_319
T9	VSS_239	VSS_320
U37	VSS_240	VSS_321
U38	VSS_241	VSS_322
UJ12	VSS_242 or	VSS_323
UJ14	VSS_243 or	VSS_324

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CFL-H		
UH1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP16	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP25	VSS_332	VSS_416
BP26	VSS_333	VSS_417
BP29	VSS_334	VSS_418
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BP34	VSS_336	VSS_420
BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
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BT32	VSS_355	VSS_439
BT5	VSS_356	VSS_440
C11	VSS_357	VSS_441
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C15	VSS_359	VSS_443
C17	VSS_360	VSS_444
C19	VSS_361	VSS_445
C21	VSS_362	VSS_446
C23	VSS_363	VSS_447
C25	VSS_364	VSS_448
C27	VSS_365	VSS_449
C29	VSS_366	VSS_450
C31	VSS_367	VSS_451
C37	VSS_368	VSS_452
C5	VSS_369	VSS_453
C8	VSS_370	VSS_454
C9	VSS_371	VSS_455
D10	VSS_372	VSS_456
D12	VSS_373	VSS_457
D14	VSS_374	VSS_458
D16	VSS_375	VSS_459
D18	VSS_376	VSS_460
D20	VSS_377	VSS_461
D22	VSS_378	VSS_462
D24	VSS_379	VSS_463
D26	VSS_380	VSS_464
D28	VSS_381	VSS_465
D3	VSS_382	VSS_466
D30	VSS_383	VSS_467
D33	VSS_384	VSS_468
D6	VSS_385	VSS_469
D9	VSS_386	VSS_470
E34	VSS_387	VSS_471
E35	VSS_388	VSS_472
E38	VSS_389	VSS_473
E4	VSS_390	VSS_474
E9	VSS_391	VSS_475
N3	VSS_392	VSS_476
N33	VSS_393	VSS_477
N34	VSS_394	VSS_478
N4	VSS_395	VSS_479
N5	VSS_396	
N6	VSS_397	VSS_A3
N7	VSS_398	VSS_A4
N8	VSS_399	VSS_B3
N9	VSS_400	VSS_B3
P12	VSS_401	VSS_B37
P37	VSS_402	VSS_BR38
M14	VSS_403	VSS_BT3
M6	VSS_404	VSS_BT35
N1	VSS_405	VSS_BT36
F11	VSS_406	VSS_BT4
F13	VSS_407 or VSS_C2	VSS_D38

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		2027/06/21		Rev	
Size		Document		Number	
Custom				1.0(A00)	
Date:		Wednesday, June 06, 2018		Sheet 13 of 76	

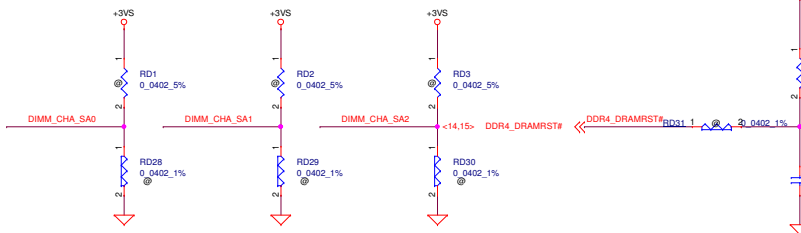
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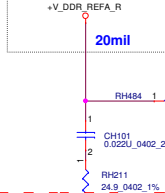
P13-CPU(7/7) VSS

The circuit diagram shows a 4-bit DAC implemented with an op-amp buffer and a resistor ladder. The input is a 2.5V MEM signal. The circuit consists of four op-amp buffers (CD9, CD10, CD3, CD4) and four resistors (10k, 10k, 10k, 10k). The output of the first buffer (CD9) is connected to the input of the second buffer (CD10), and so on, forming a chain. The output of the final buffer (CD4) is the DAC output.

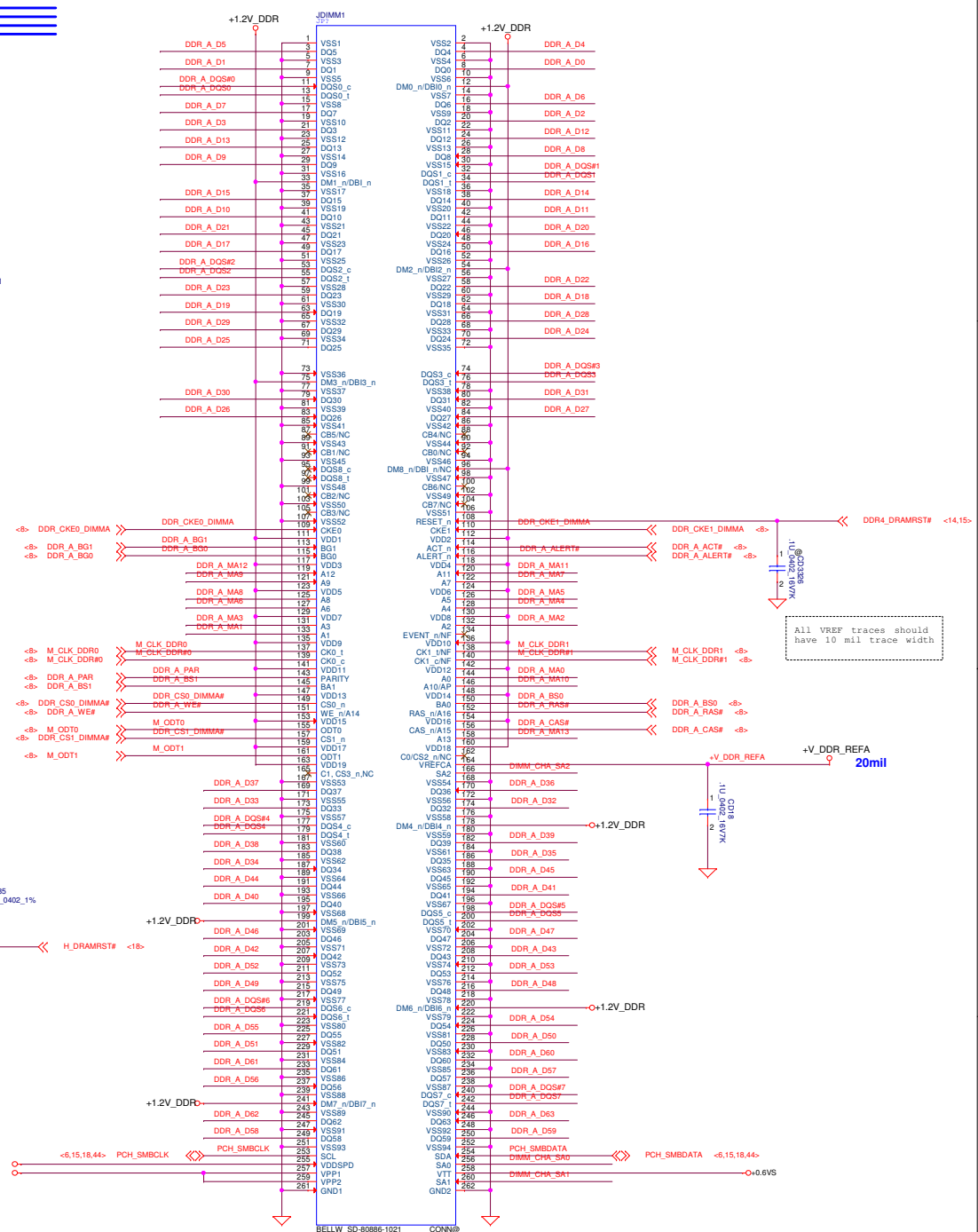
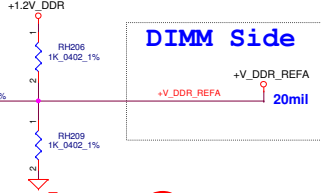
The schematic shows two DDR memory modules connected to a system bus. The top module is labeled '+1.2V\_DDR' and contains eight chips: U0\_06D1E3WK, U1\_06D1E3WK, U2\_06D1E3WK, U3\_06D1E3WK, U4\_06D1E3WK, U5\_06D1E3WK, U6\_06D1E3WK, and U7\_06D1E3WK. Each chip has pins 1 and 2 connected to the bus. The bottom module is labeled '+1.2V\_DDR' and contains four chips: C0\_09D1F7WM, C1\_09D1F7WM, C2\_09D1F7WM, and C3\_09D1F7WM. Each chip has pins 1 and 2 connected to the bus. A ground symbol is shown at the bottom right.



CPU Side



## DIMM Side



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			Sheet	14 of 76

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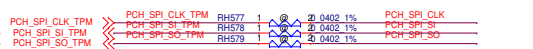
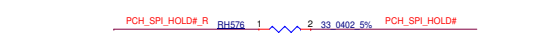
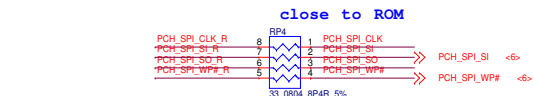
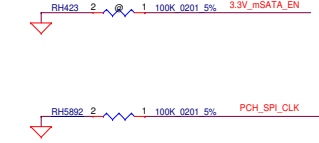
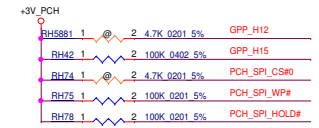
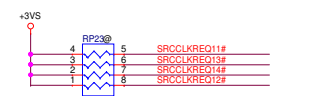
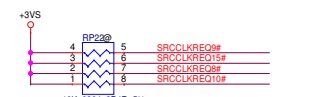
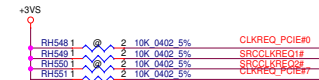
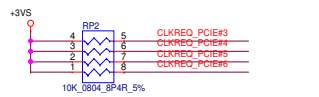
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			Date:	Wednesday, June 06, 2018	Sheet	15 of 76

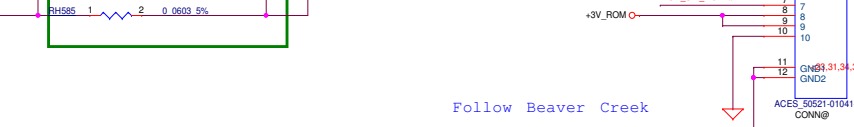
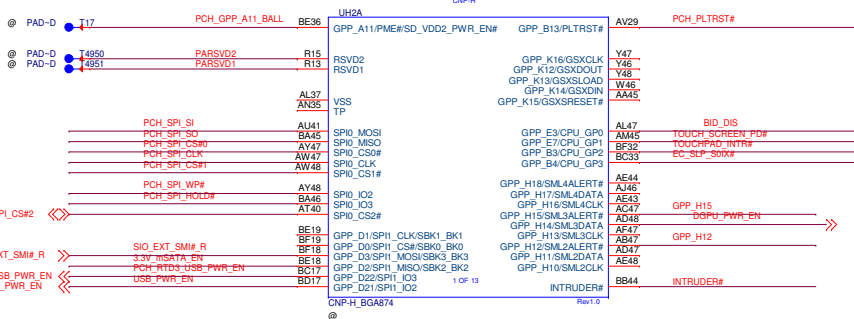
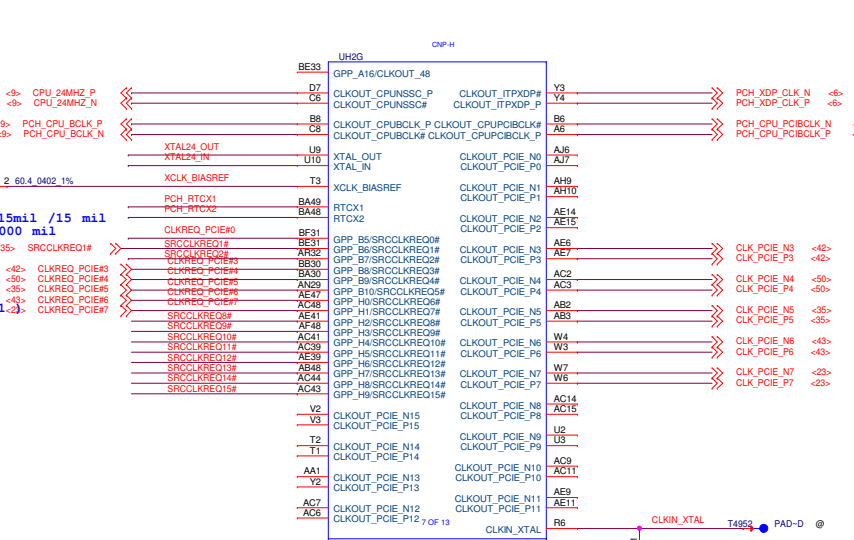
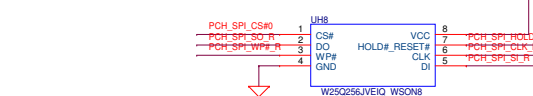




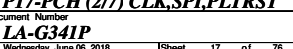
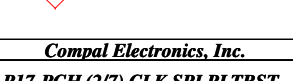
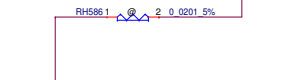
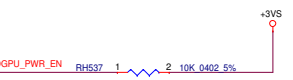
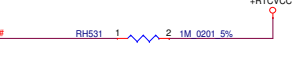
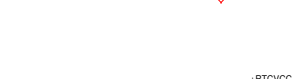
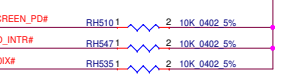
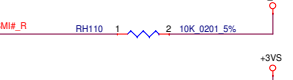
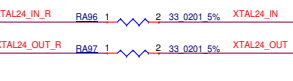
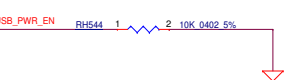
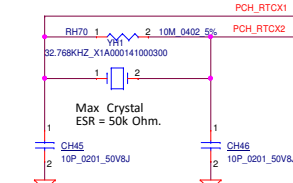




## SPI ROM FOR ME ( 32MByte )

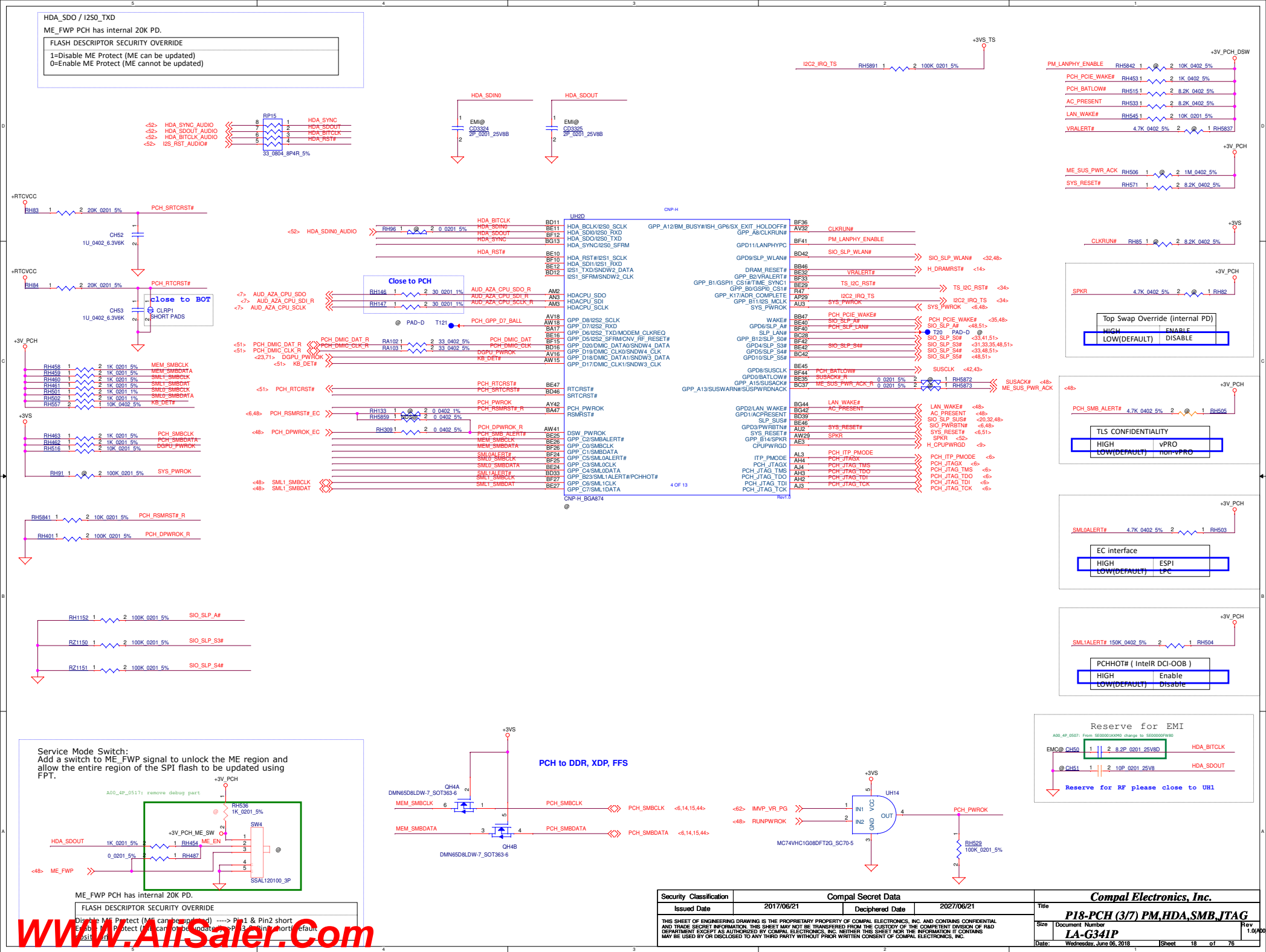


## RTC CRYSTAL

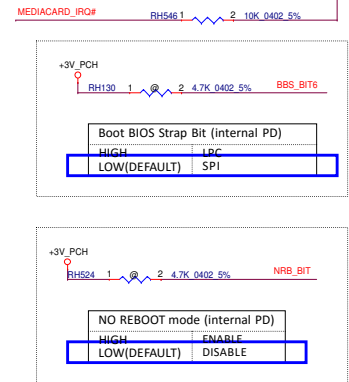


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Size	Document Number	Rev	1.0(100)
LA-G341P			
Date:	Wednesday, June 06, 2018	Sheet	17 of 76

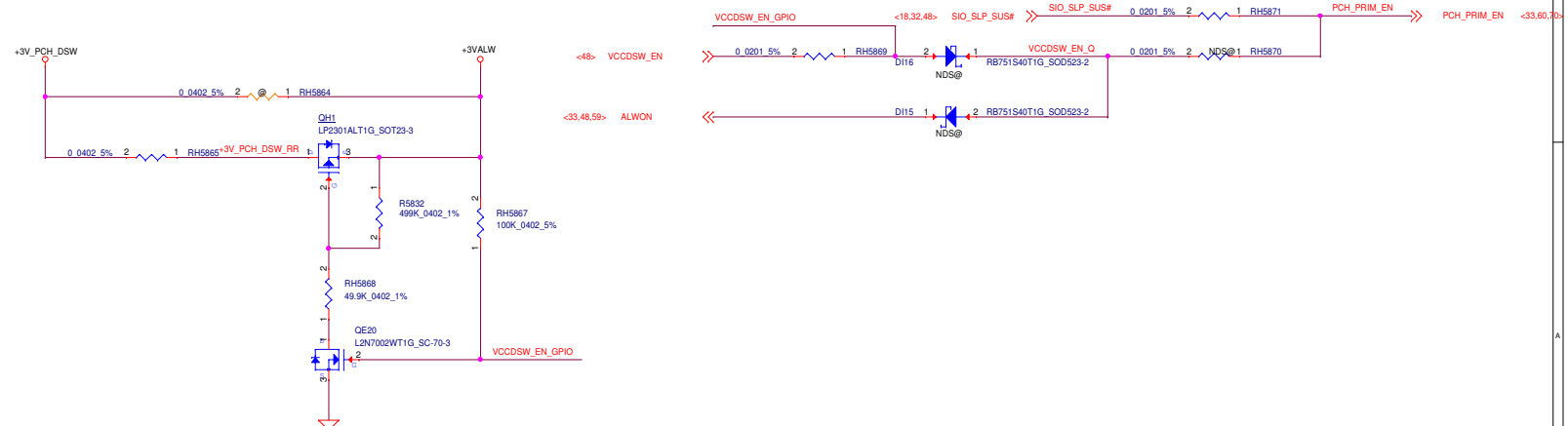
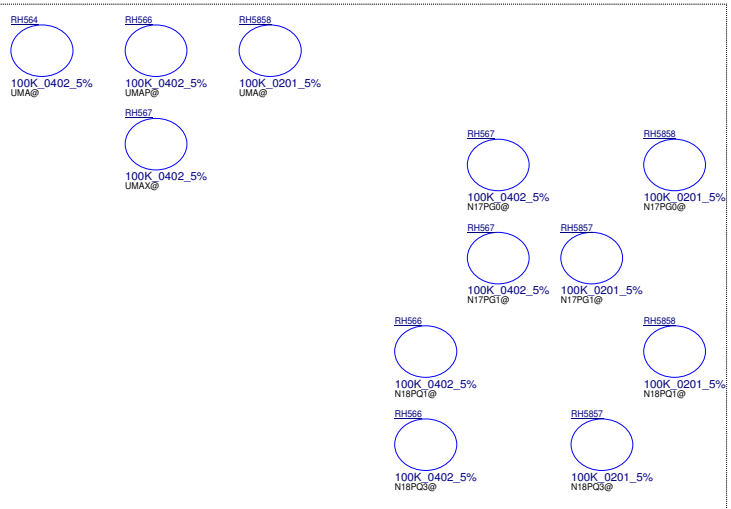




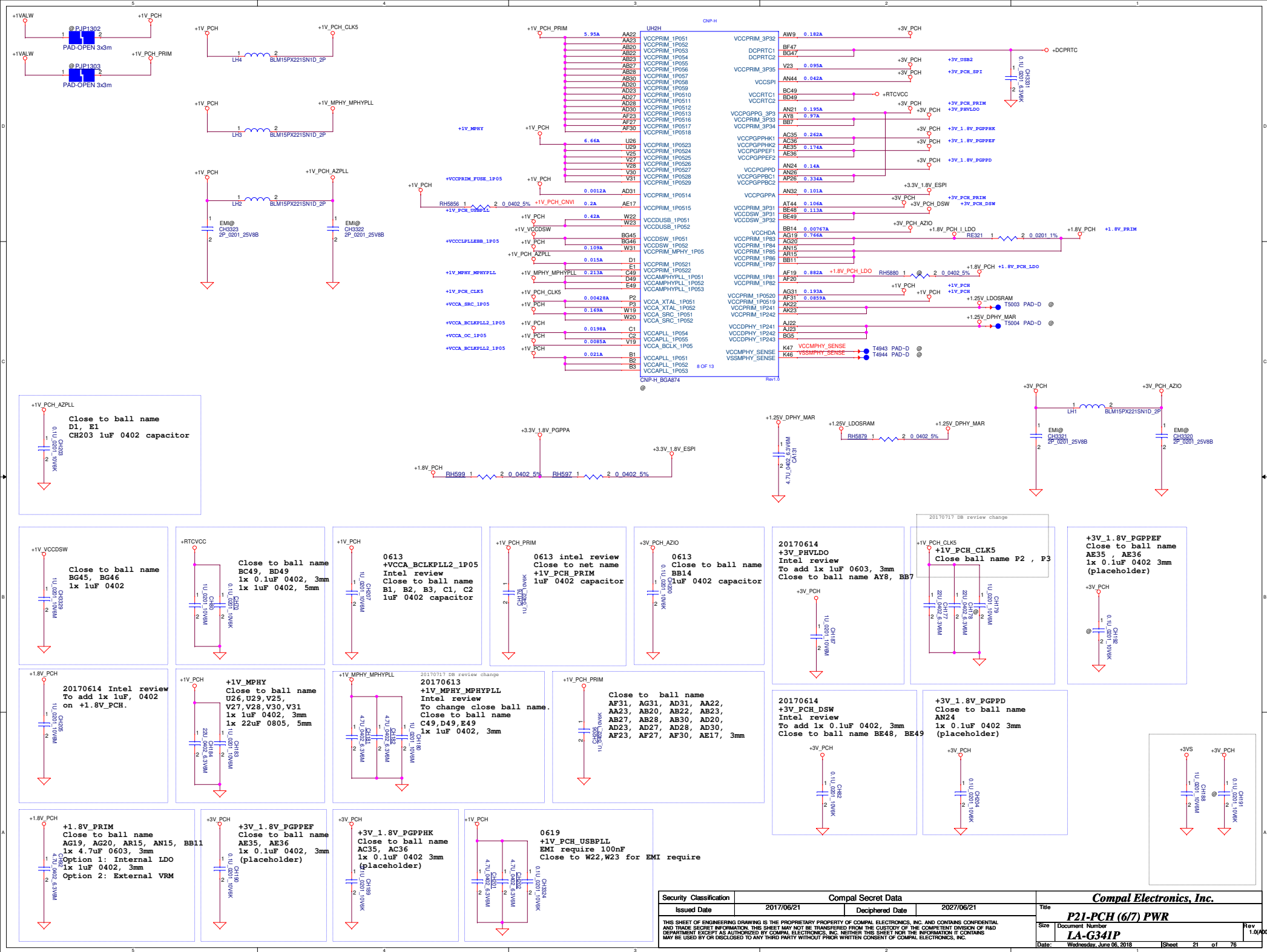


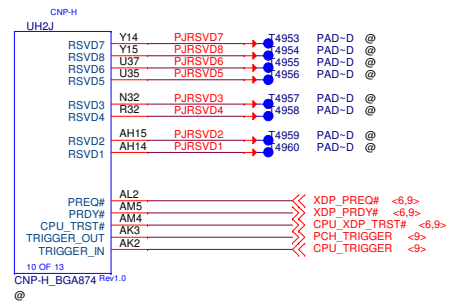
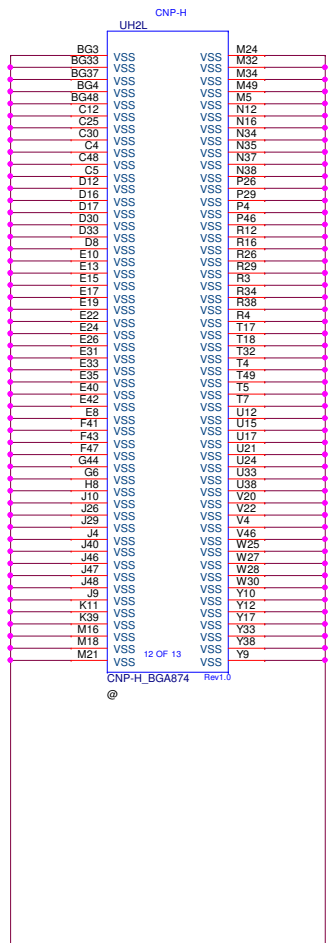
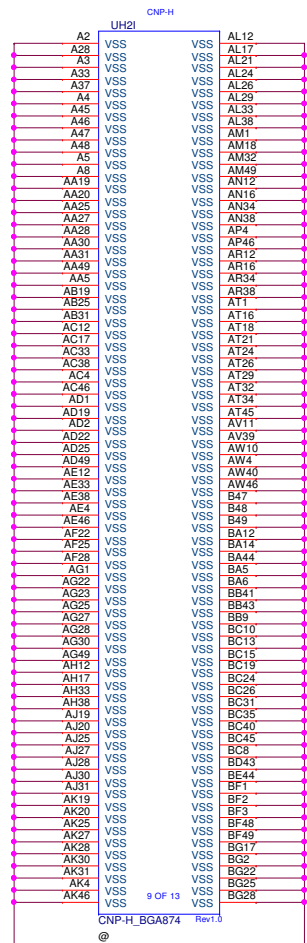
Three circuit diagrams are shown, each representing a different component connected to the +3V\_PCH pin. Each diagram includes a pull-up resistor (RH564, RH566, or RH5857) connected to +3V\_PCH and a signal line (BID\_DIS, BID\_BC, or BID\_GPU) connected to ground. The signal lines are labeled with their respective component values and tolerances.

- Diagram 1 (Left):** Shows a pull-up resistor RH564 (100K\_0402\_5%) connected to +3V\_PCH. The signal line is BID\_DIS, which is connected to ground. The signal line is labeled with its component value and tolerance: BID\_DIS <17.48>.
- Diagram 2 (Middle):** Shows a pull-up resistor RH566 (100K\_0402\_5%) connected to +3V\_PCH. The signal line is BID\_BC, which is connected to ground. The signal line is labeled with its component value and tolerance: BID\_BC <17.48>.
- Diagram 3 (Right):** Shows a pull-up resistor RH5857 (100K\_0201\_5%) connected to +3V\_PCH. The signal line is BID\_GPU, which is connected to ground. The signal line is labeled with its component value and tolerance: BID\_GPU <17.48>.

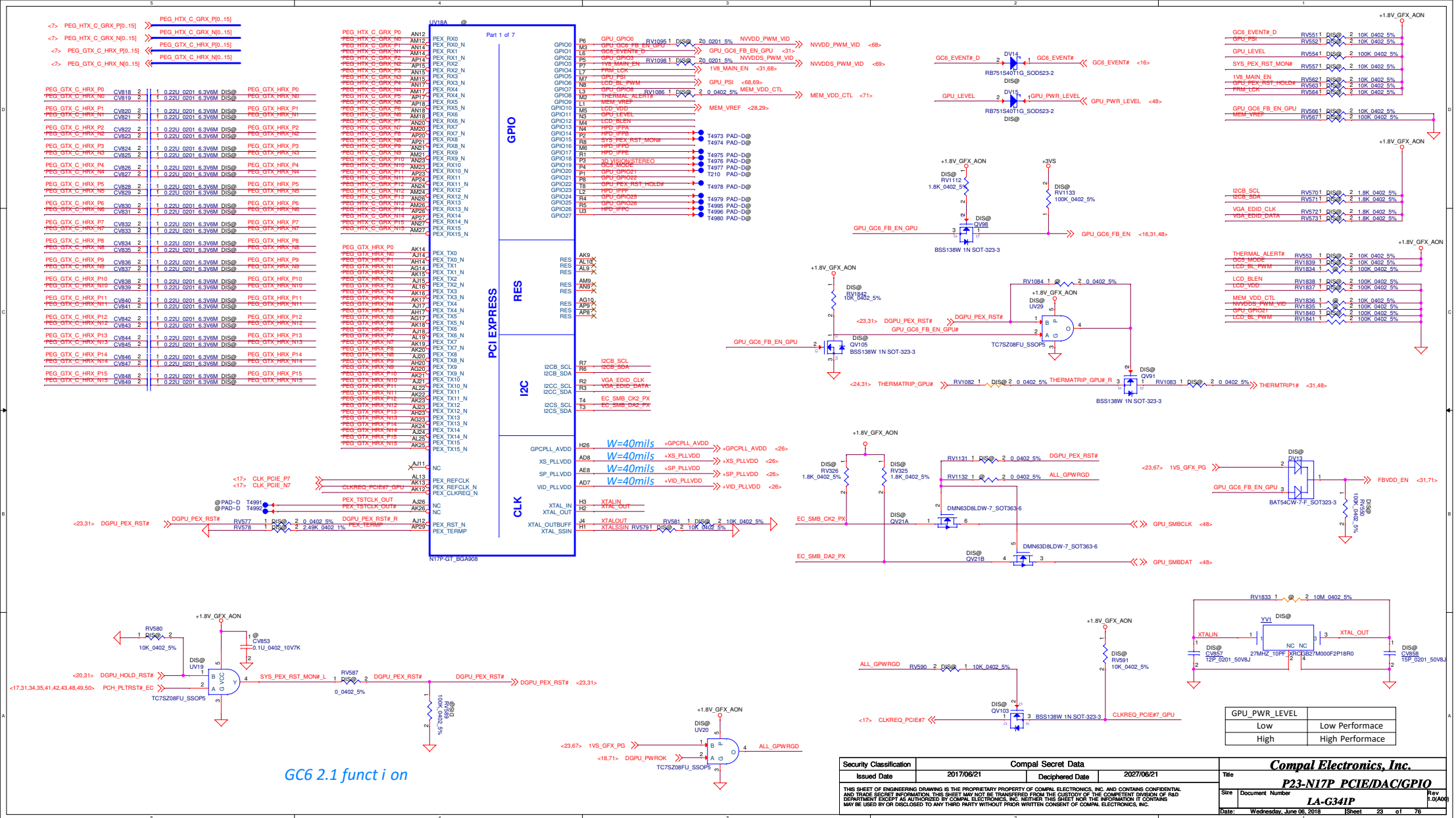


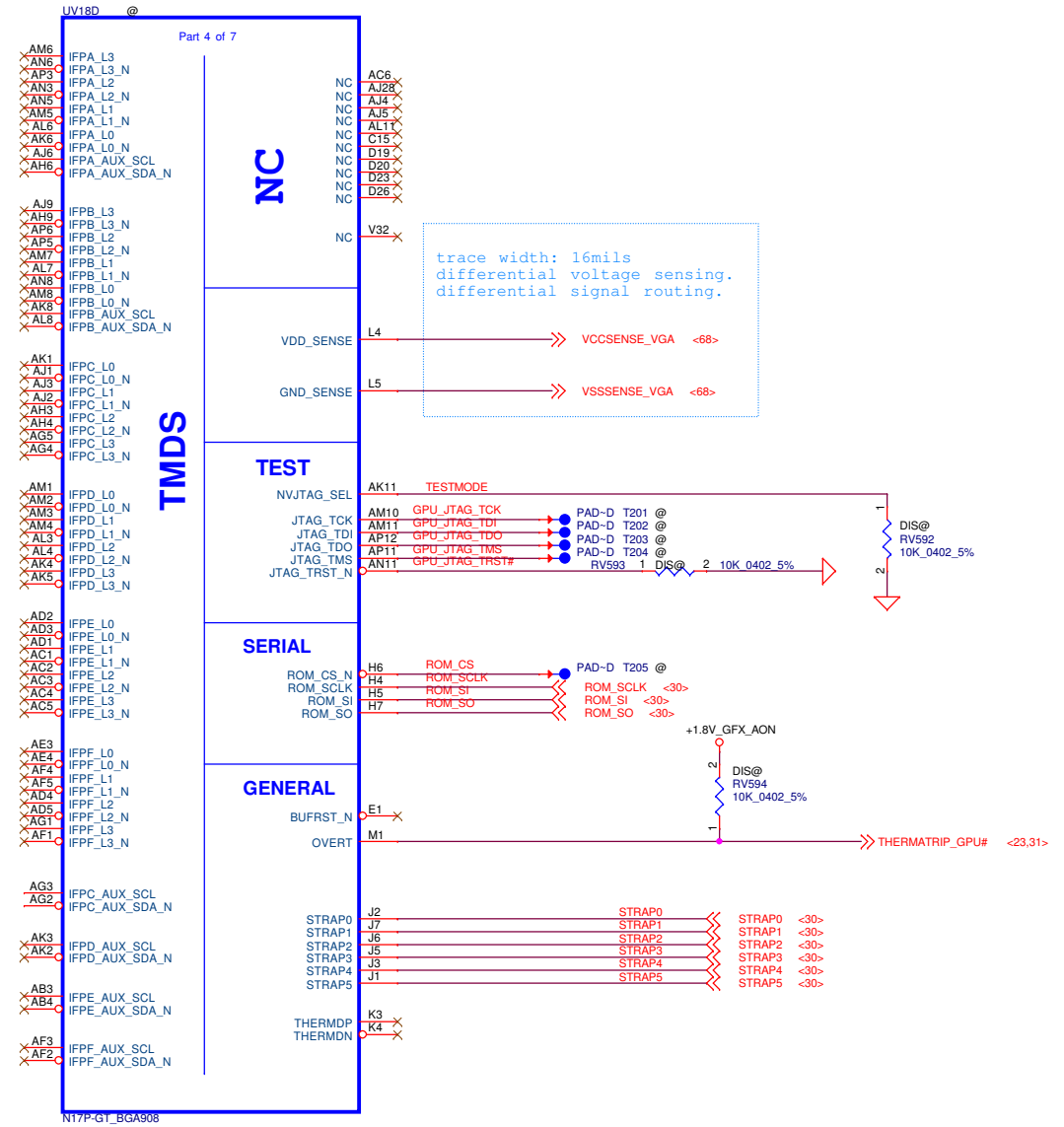
SYSTEM ID 3 (VR)









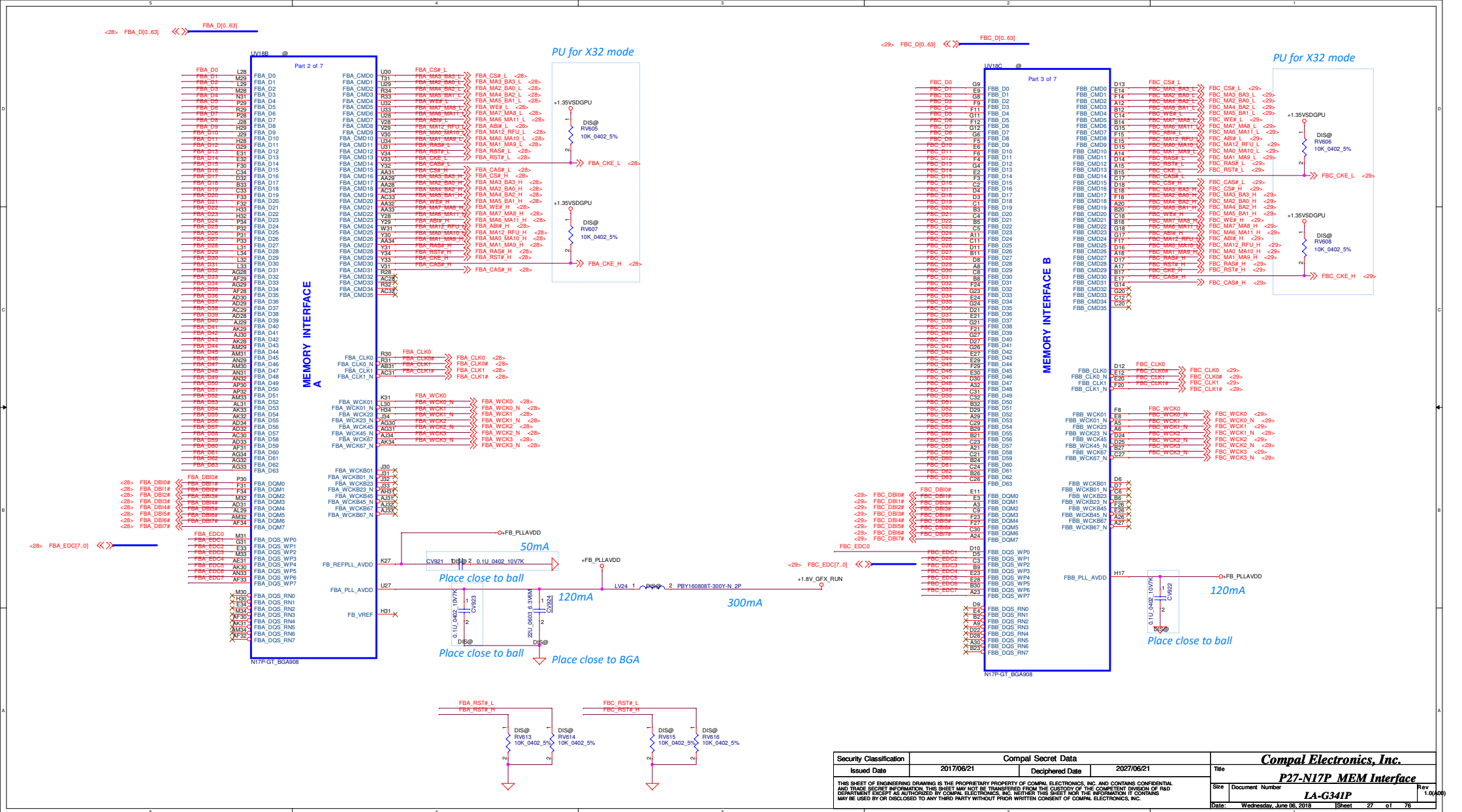


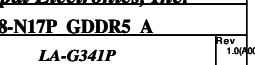
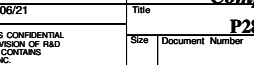
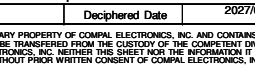
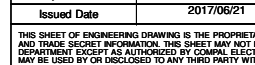
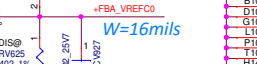
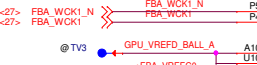
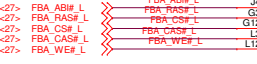
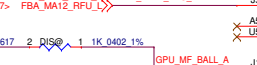
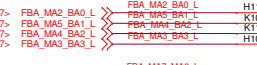
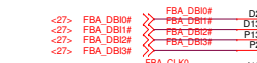
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				LA-G341P		
				Date:	Wednesday, June 06, 2018	Sheet 24 of 76







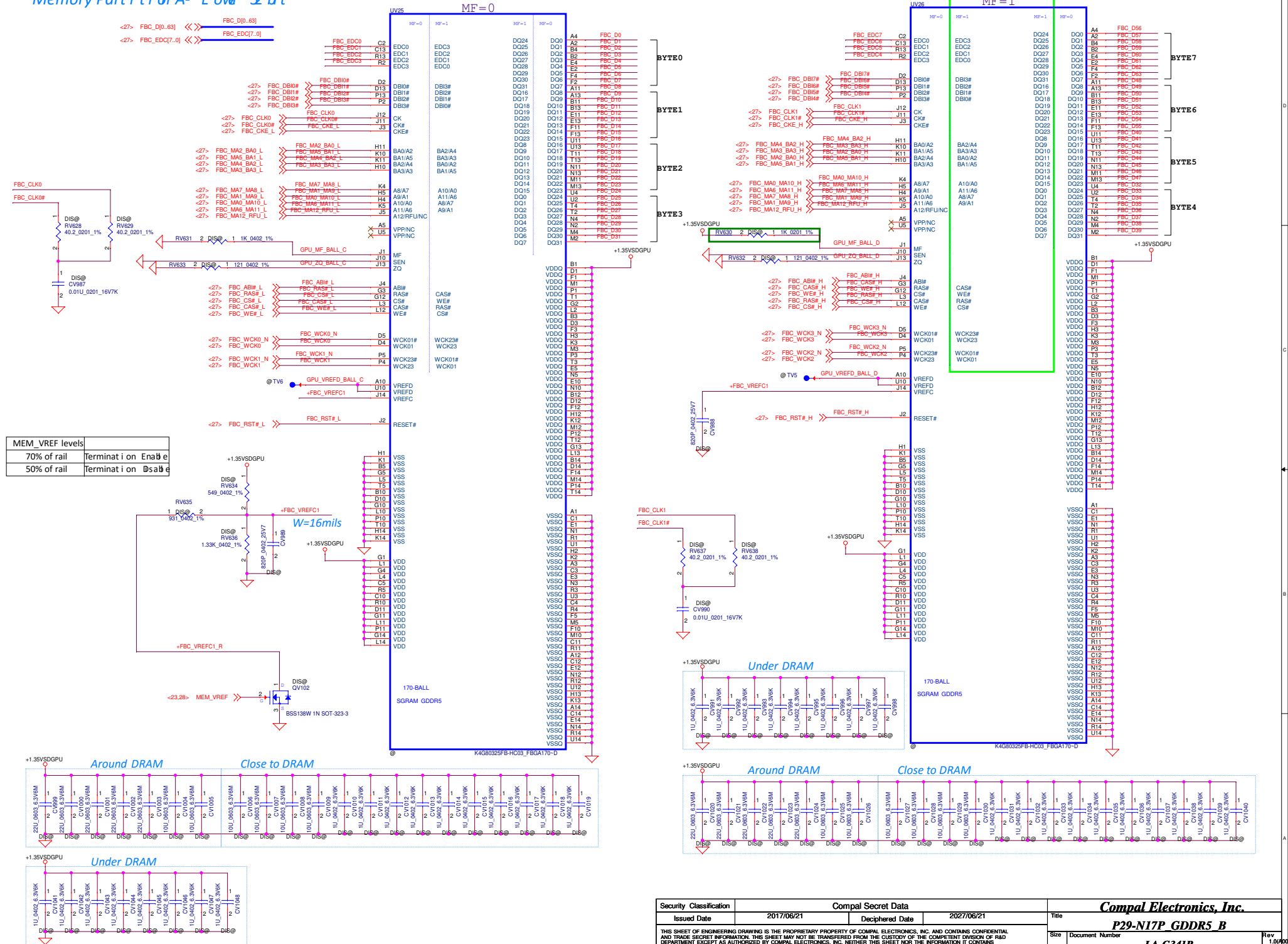


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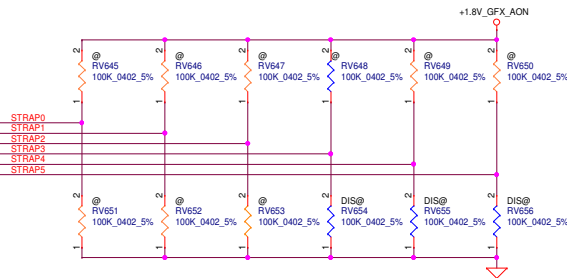
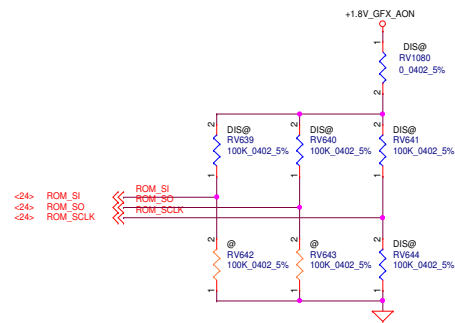
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<b>Title</b>			
<b>P28-N17P GDDR5 A</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
	<b>LA-G341P</b>		<b>1.0(400)</b>
<b>Date:</b>	<b>Wednesday, June 06, 2018</b>	<b>Sheet 28 of 76</b>	

Memory Partition A- Lower 32 bit







SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB\_ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins <sup>Note 1</sup>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins <sup>see Note</sup>			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
			Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Hynix	H5GC8H24WJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24WJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND.			
STRAP2	Do not stuff.			
STRAP3				
STRAP4				

Berlinetta MLK			
Straps	(N17P-Q1)	(N17P-G0)	
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0), DEVID_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0), VGA_DEVICE(0)
STRAP5	Unused	"L"	

Table 4. N17P-Q1 GDDR5 Recommended Memories

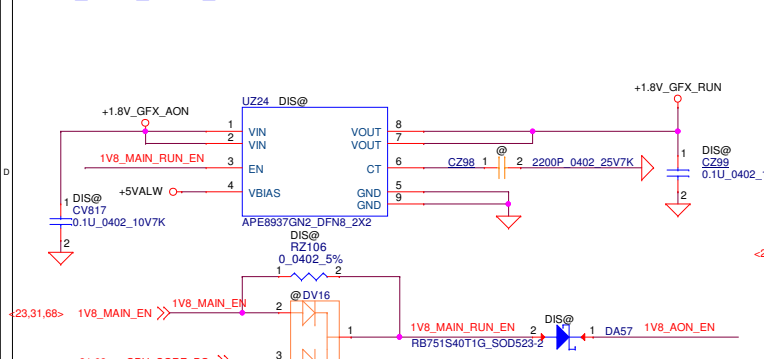
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:

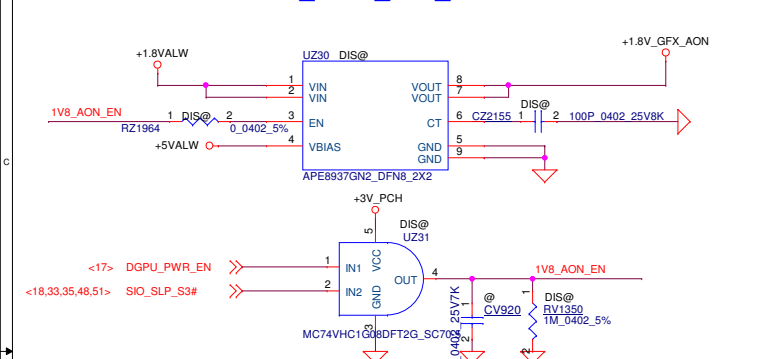
1. For N17P-Q1, the maximum allowable memory case temperature is 85 °C.

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Size	Document Number	LA-G341P	Rev	1.0/000
Date:	Wednesday, June 06, 2018	ISheet	30	of 76

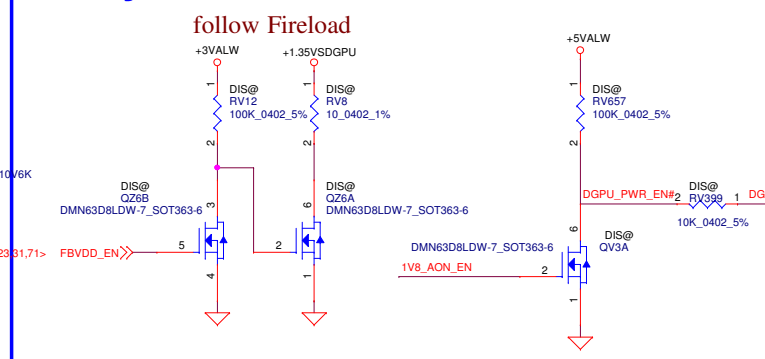
# +1.8V\_3.3V\_GFX\_RUN



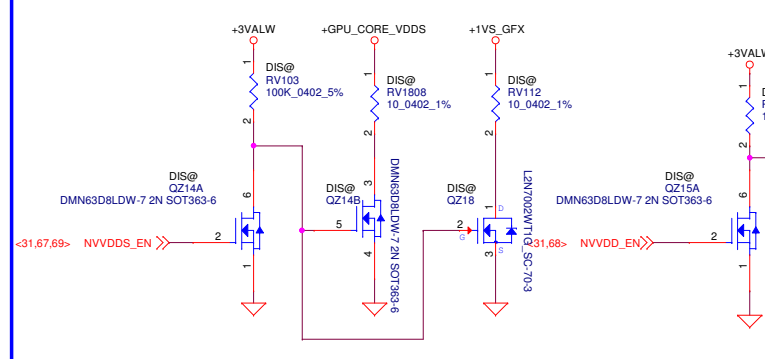
# +1.8VALW to +1.8V\_3.3V\_GFX\_AON



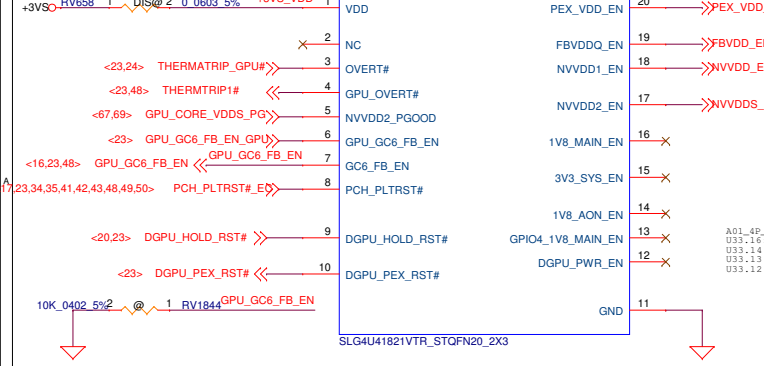
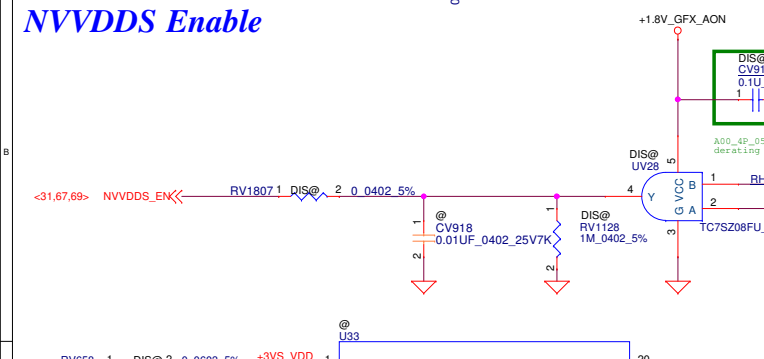
# Discharge



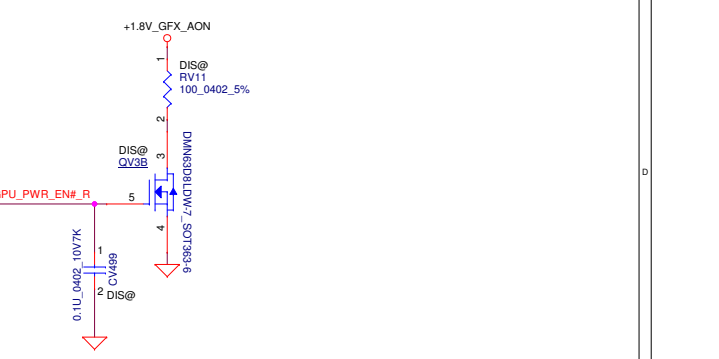
# follow Fireload



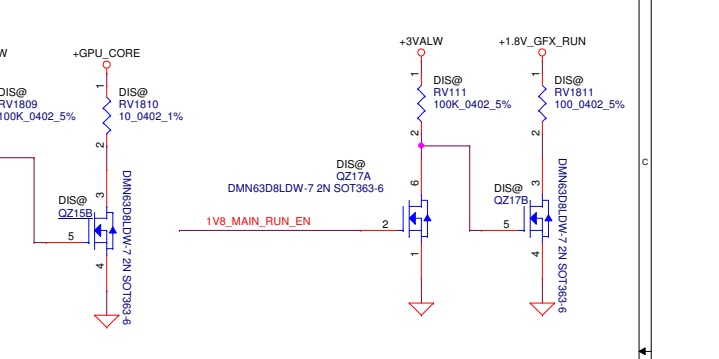
# NVVDDS Enable



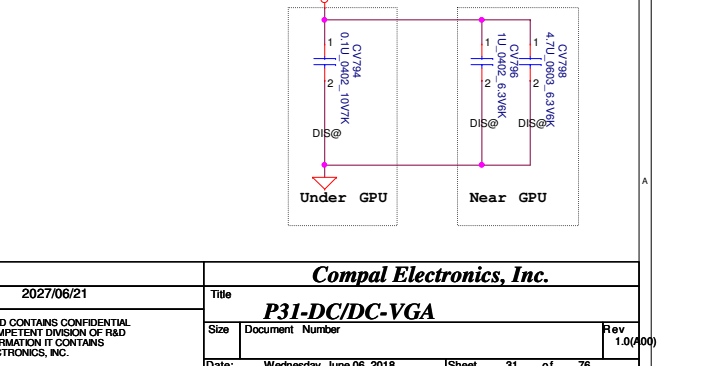
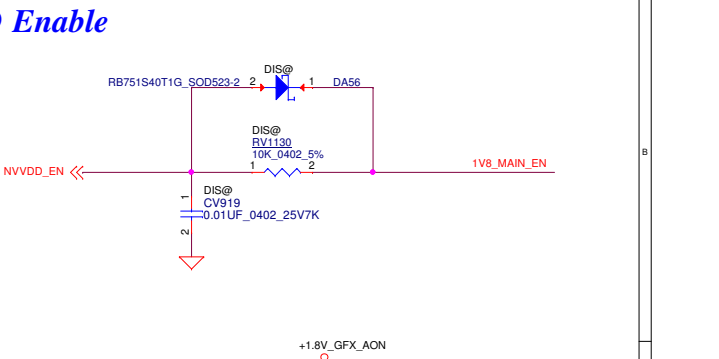
# Discharge



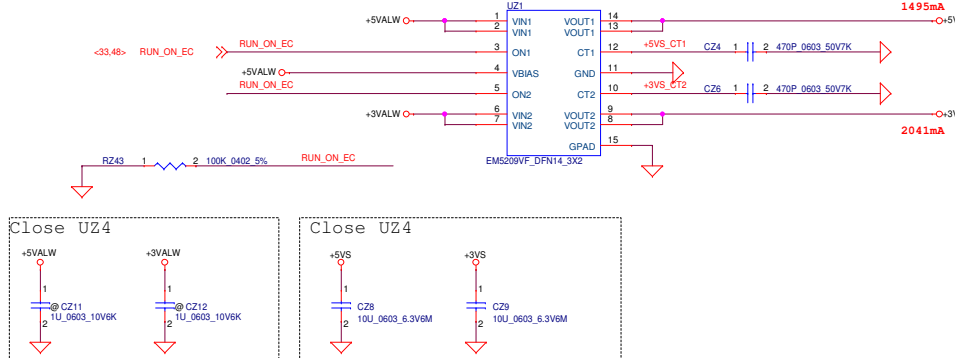
# follow Fireload



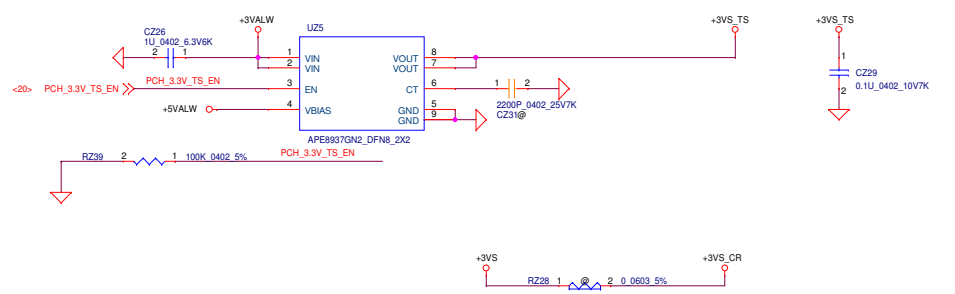
# NVVDD Enable



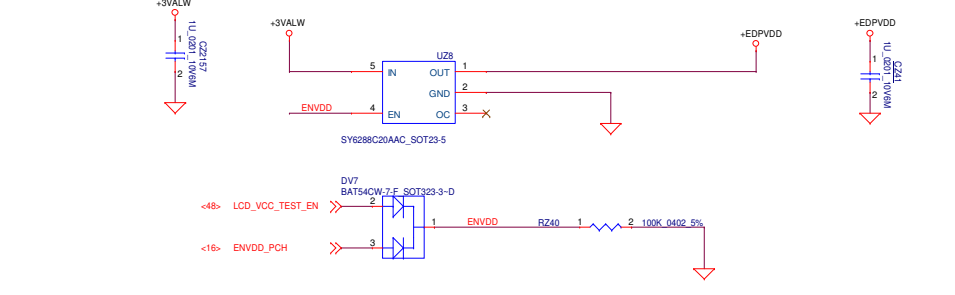
**+5VALW to +5VS  
+3VALW to +3VS**



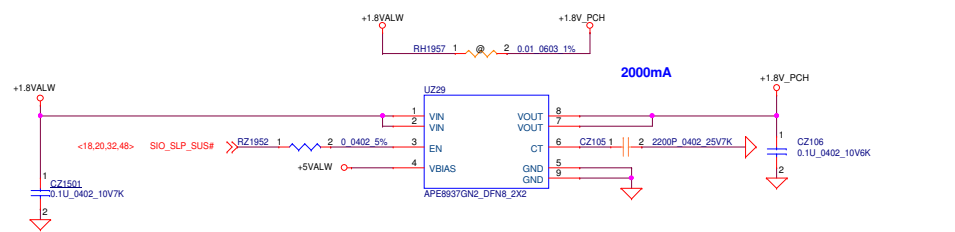
**Touch Screen Load Switch & Card Reader**



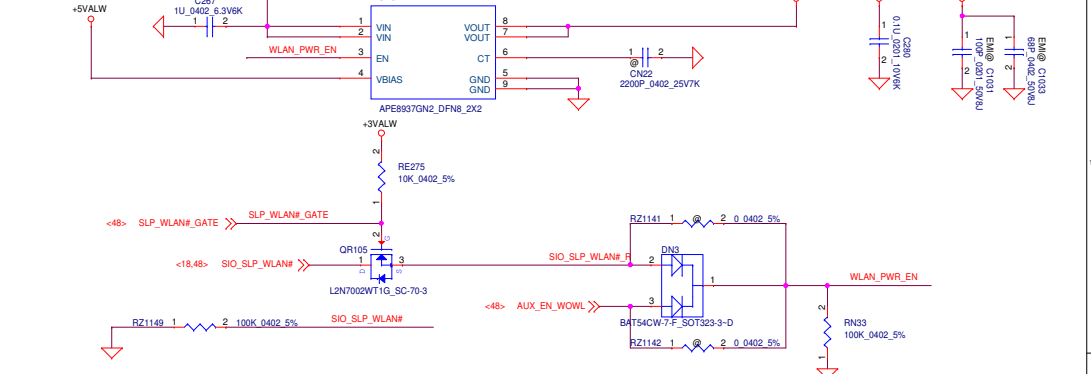
**eDP & Camera Load Switch**



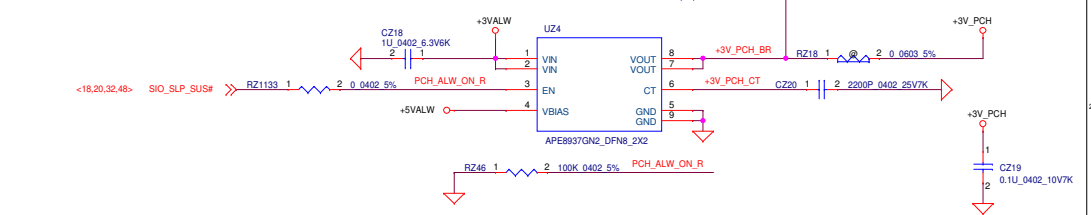
**+1.8VALW to +1.8V\_PCH**



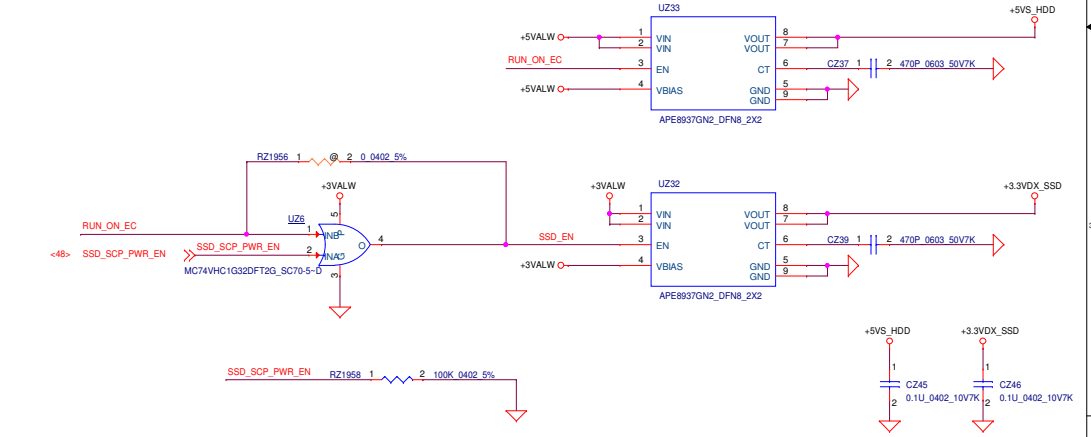
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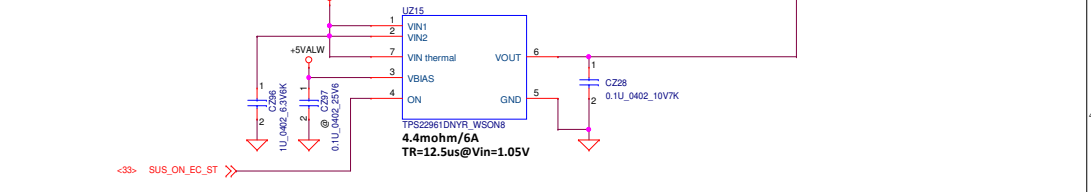
**+3VALW to +3V\_PCH**



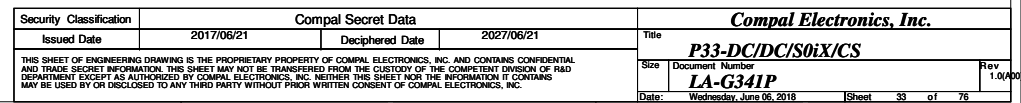
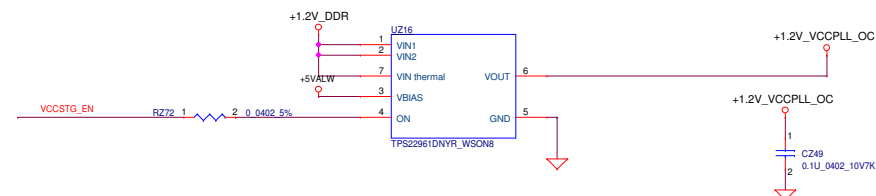
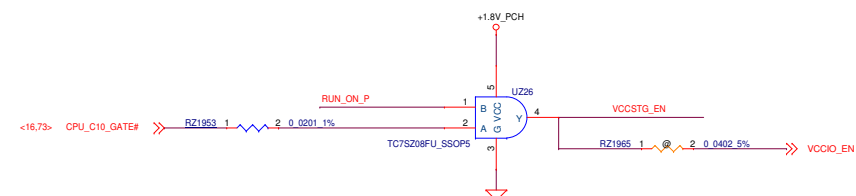
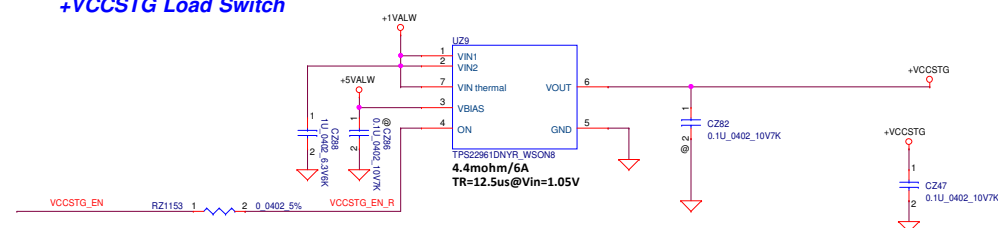
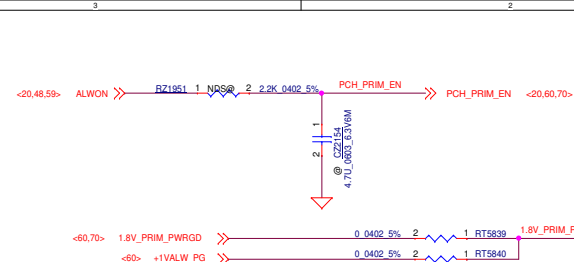
**HDD, SSD Load Switch**



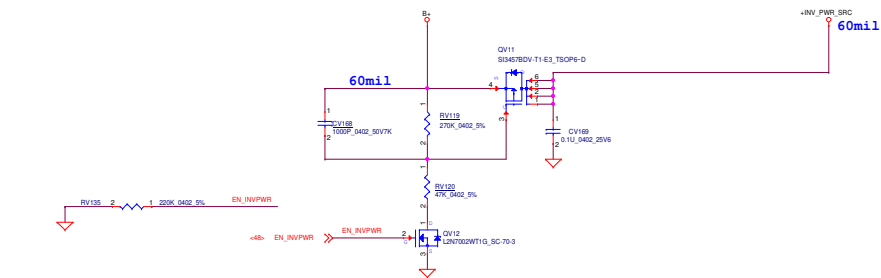
**+VCCST Load Switch**



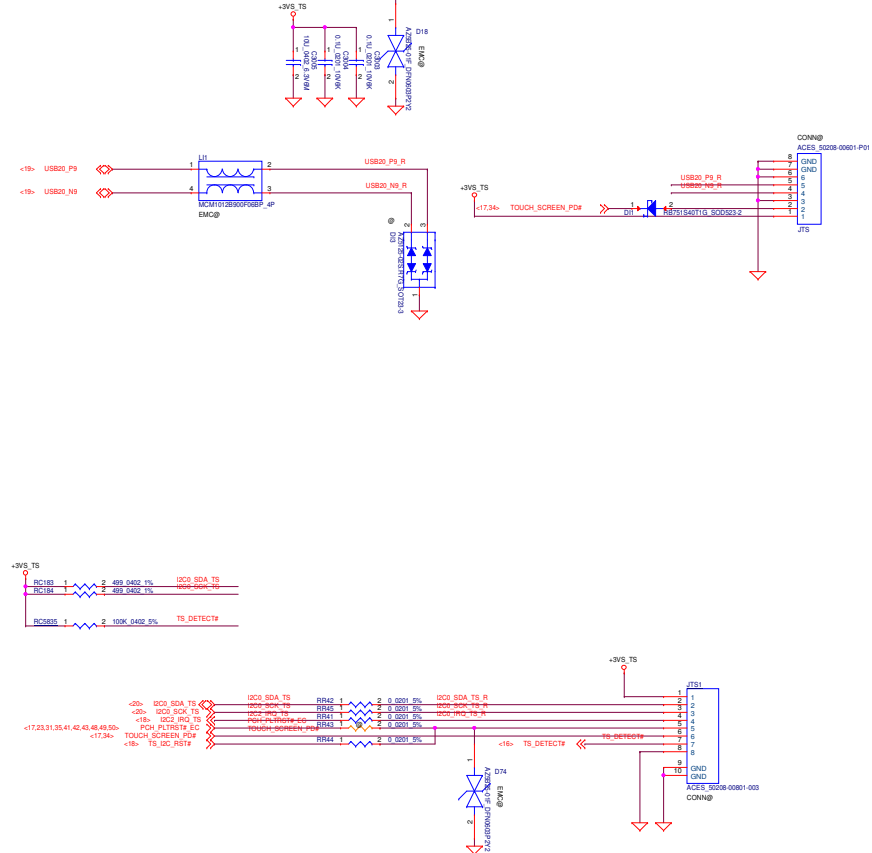




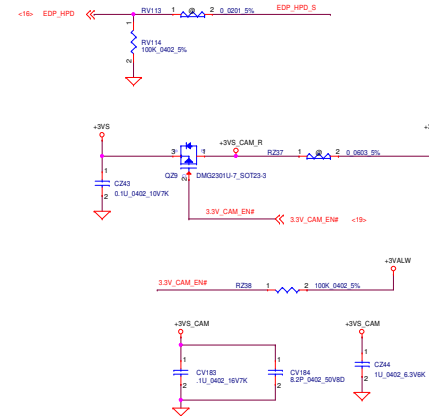
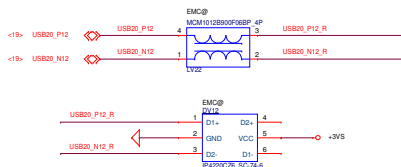
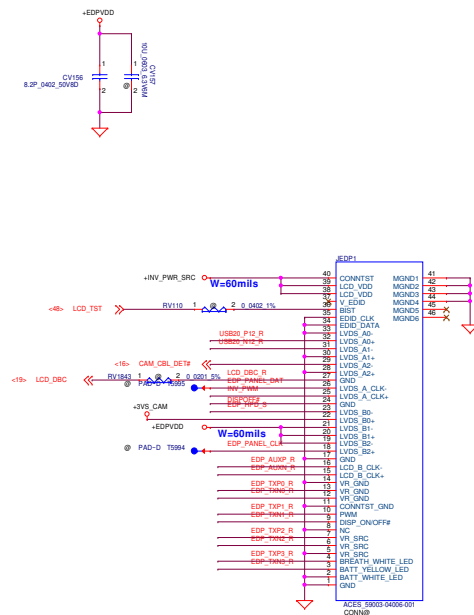
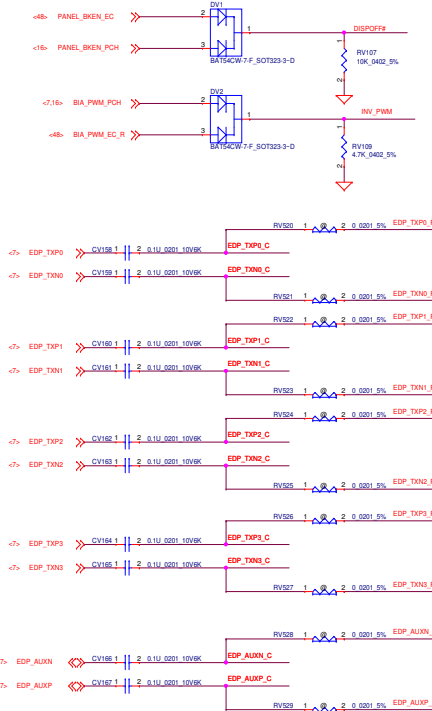
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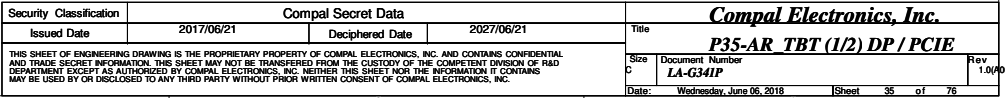


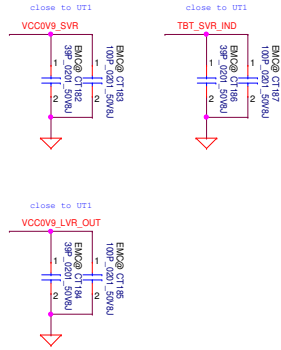
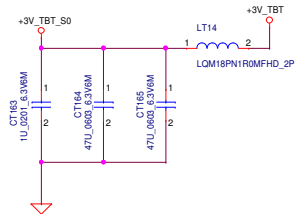
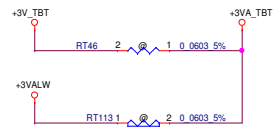
## Touch Screen Conn.



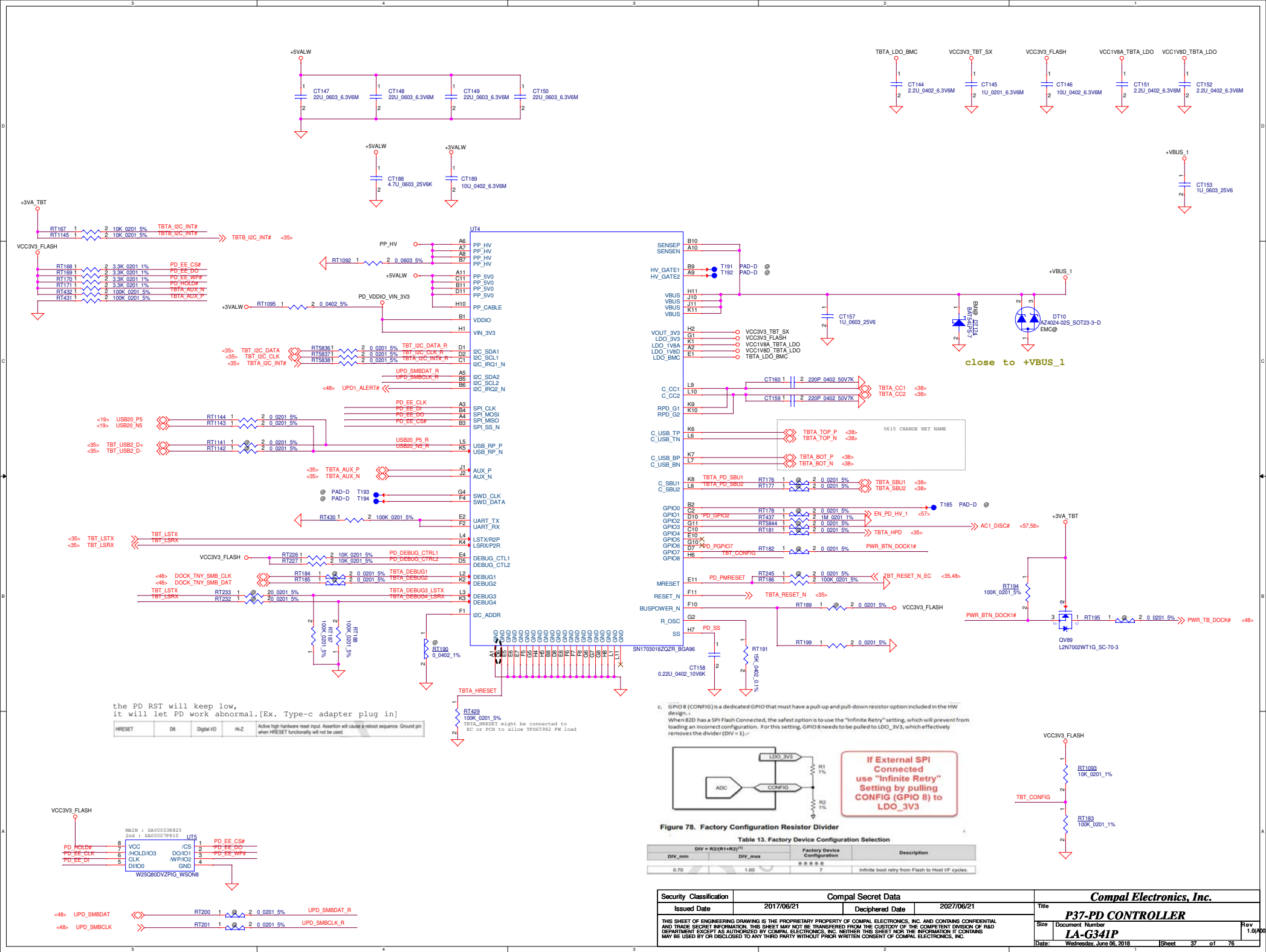
## eDP & CCD(RGB) Conn.

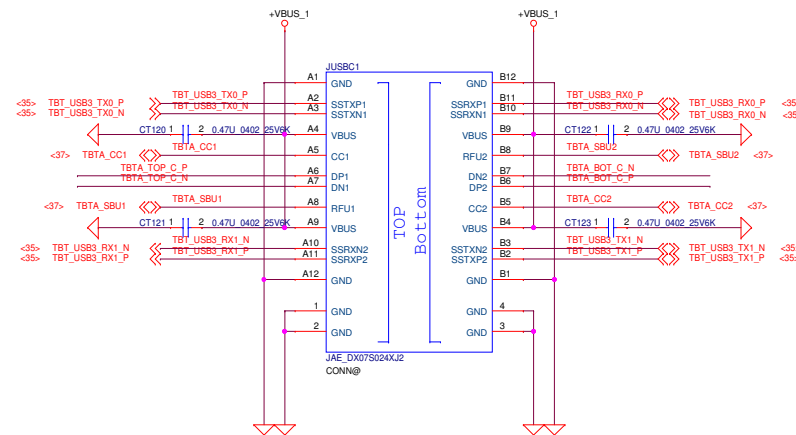
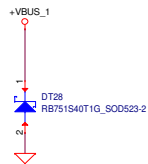
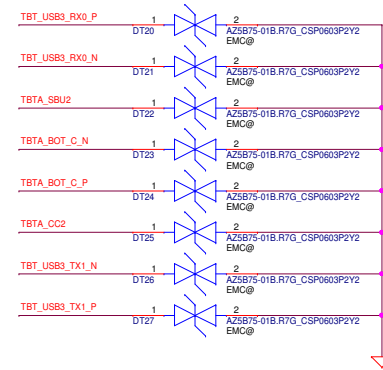
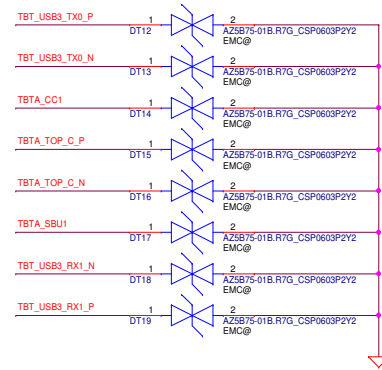
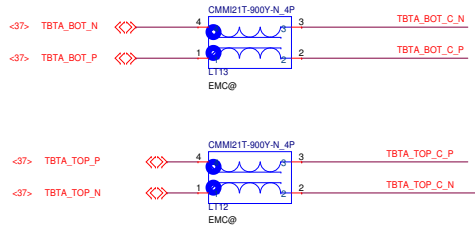




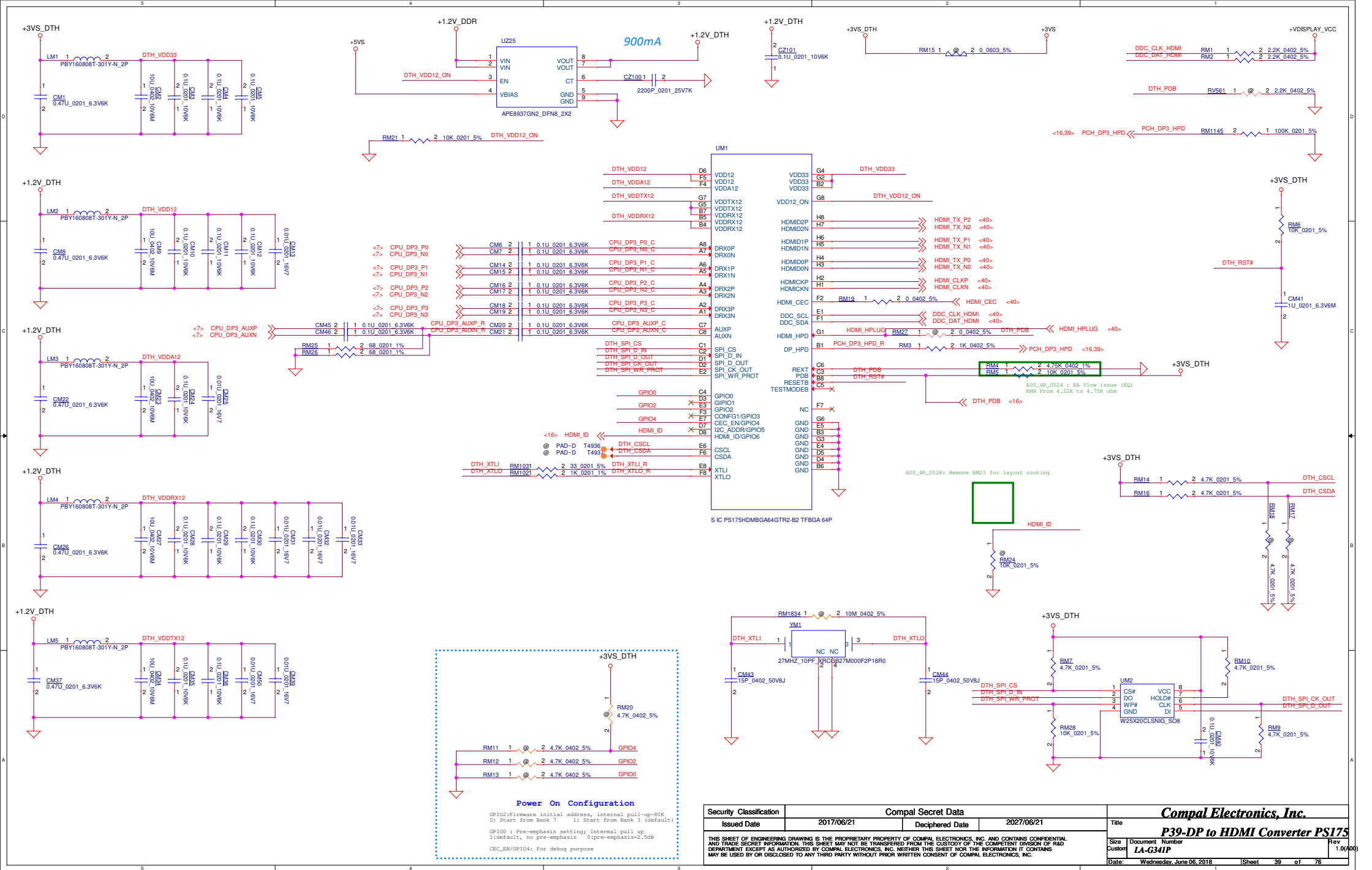


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Size	Document Number	Rev	1.0(00)	
C	LA-G341P			
Date:	Wednesday, June 06, 2018	Sheet	38	of 76



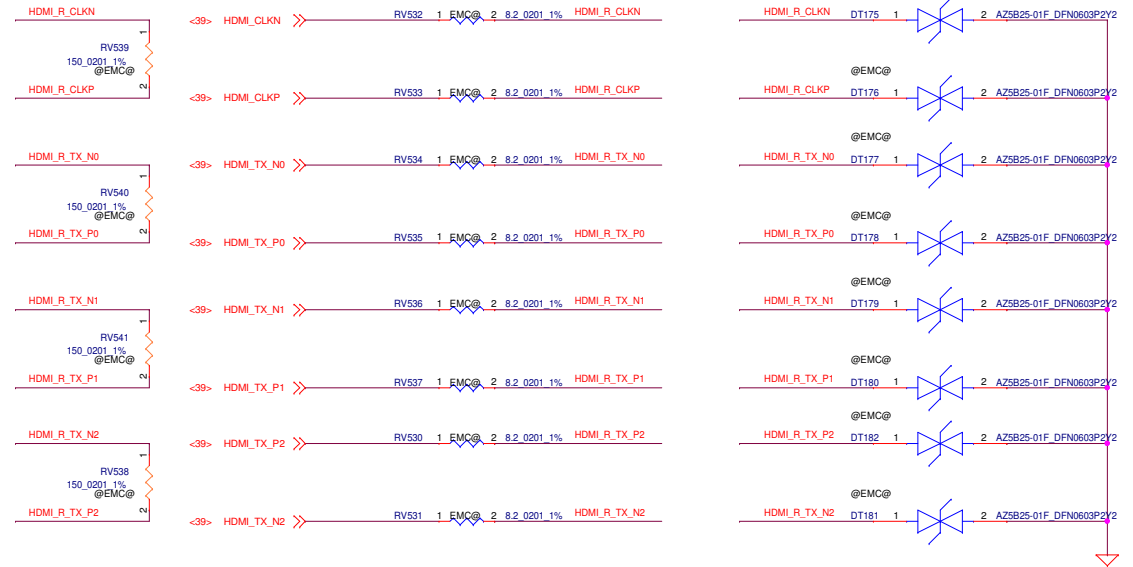
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		Date		Wednesday, June 06, 2018	
		Sheet		39 of 76	



HDMI change to CPU to PS185 to CONN

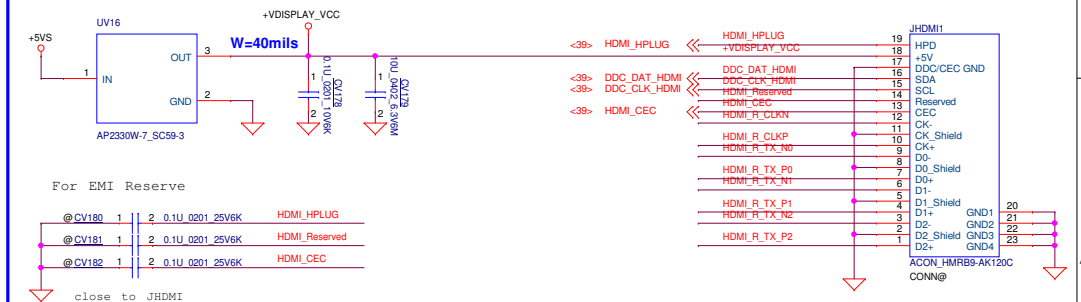
Place between ESD and CM-Choke

Place close to JHDMI1



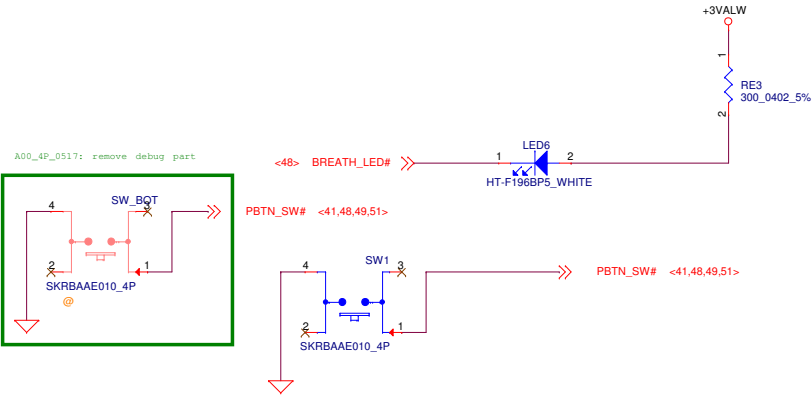
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HDMI conn

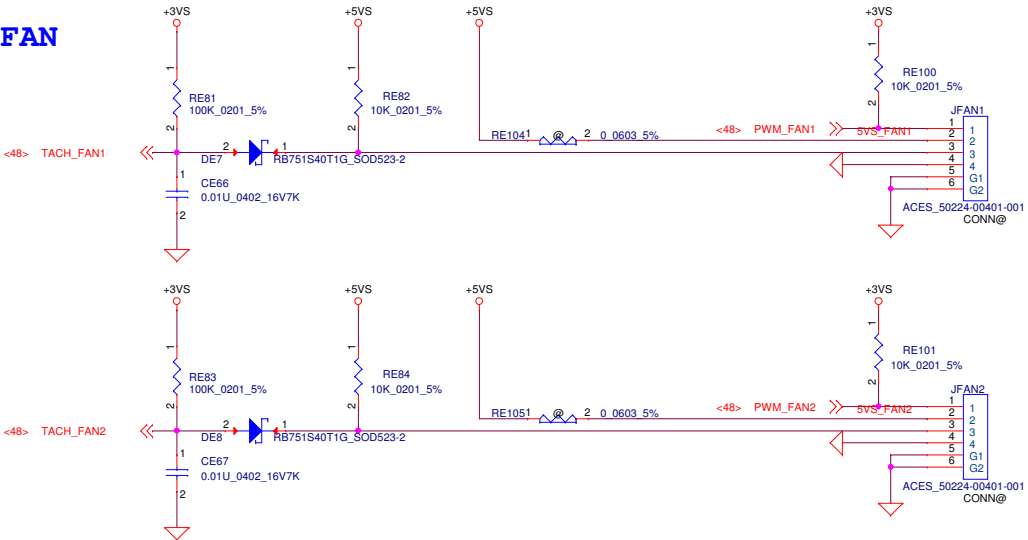


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Sheet		40	of	
Date		1	76	

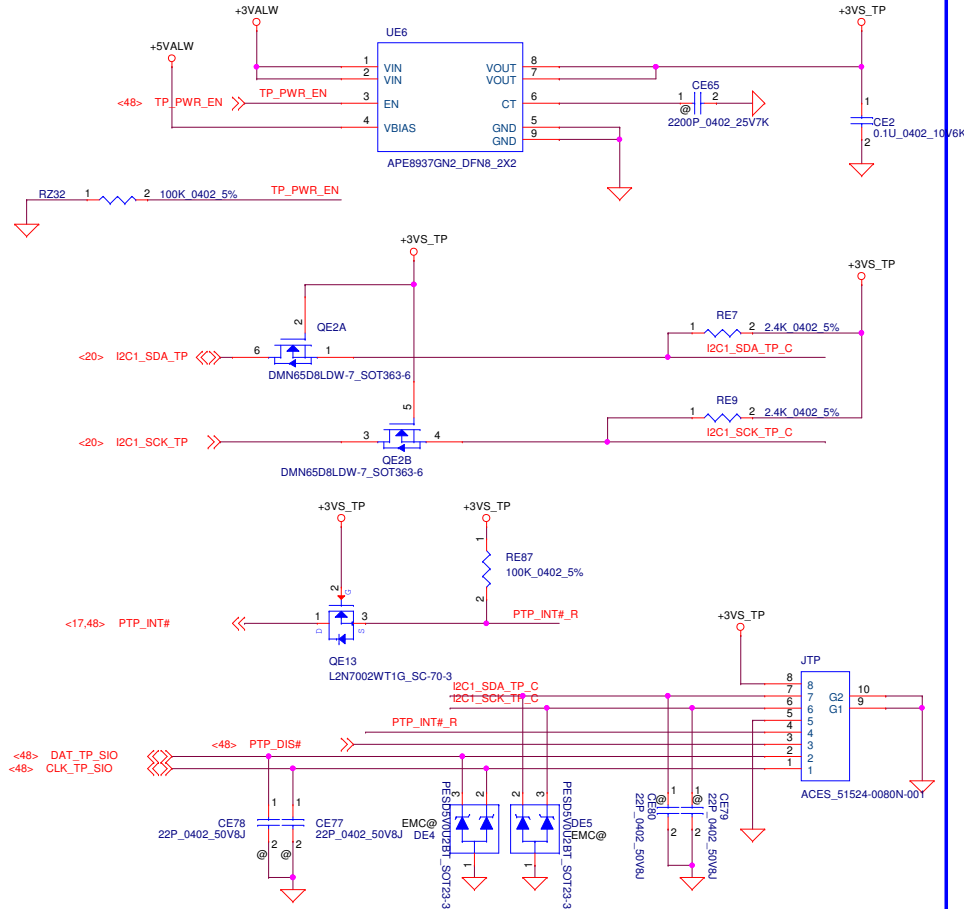
Power Button and LED



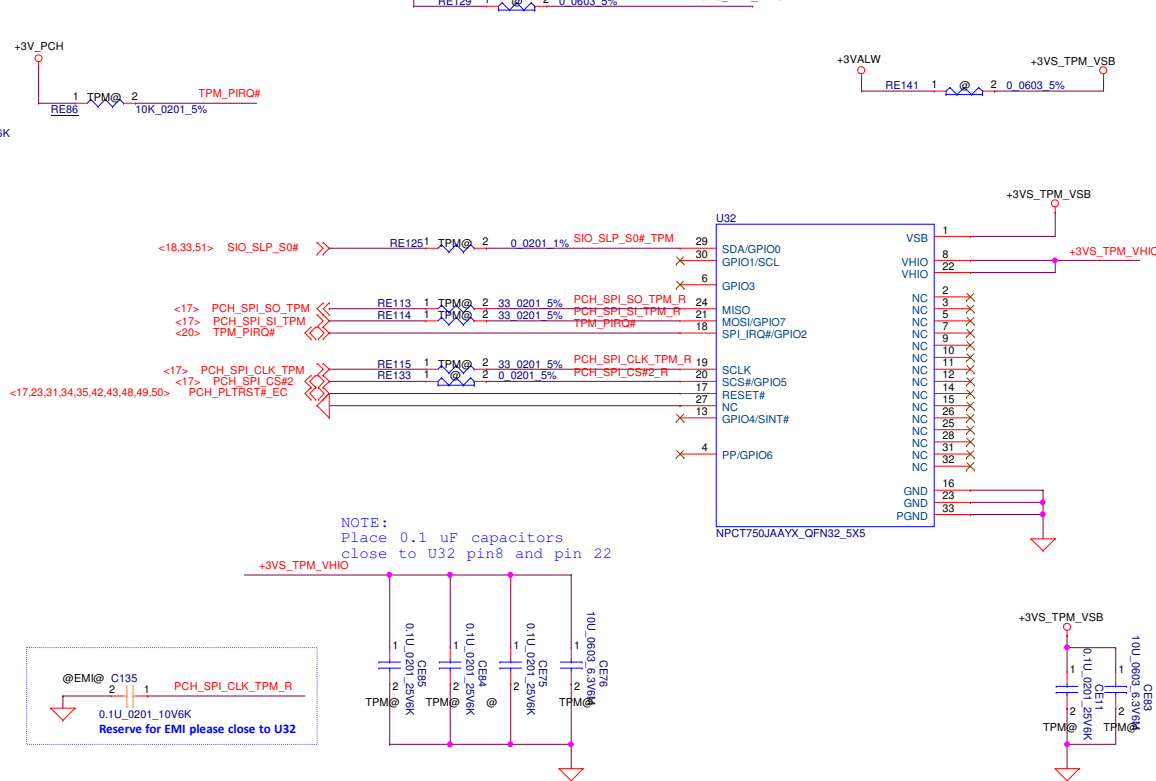
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Touch pad

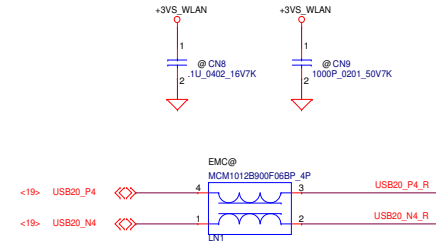
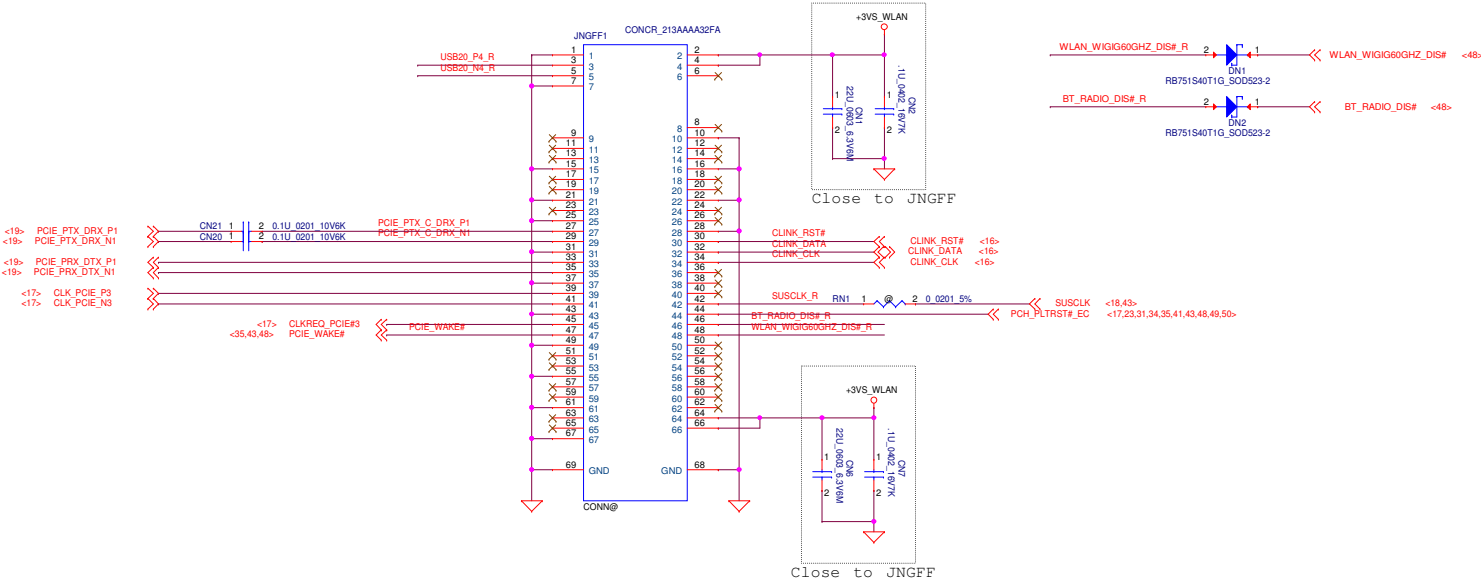


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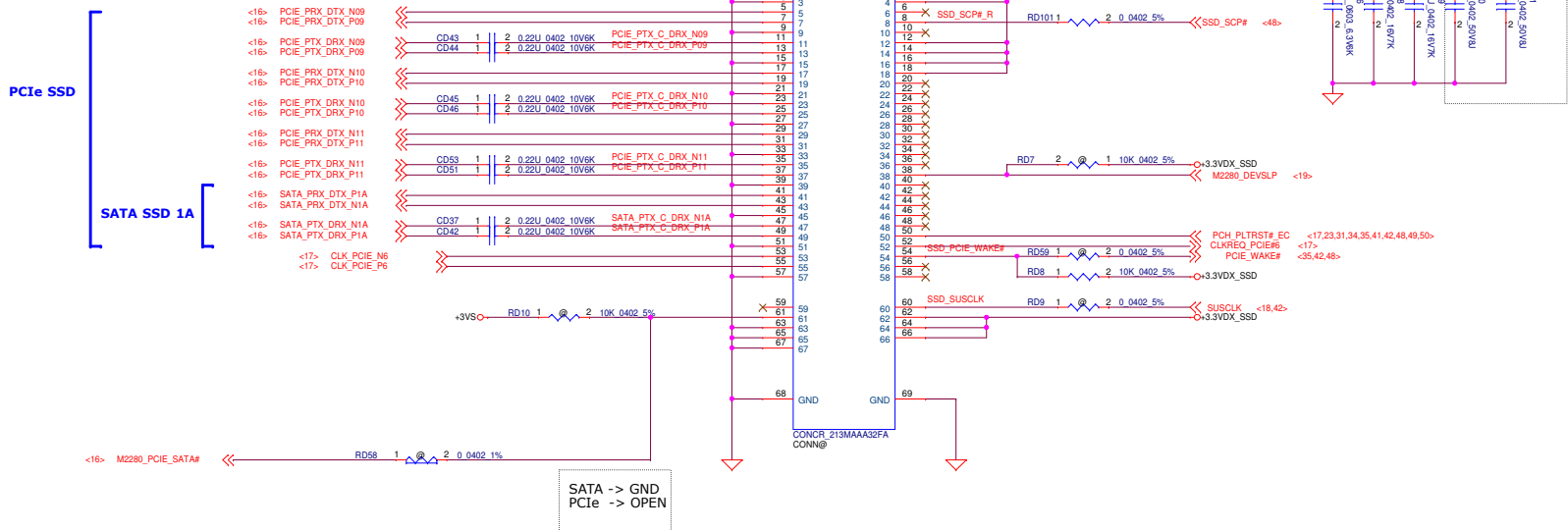
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Size	Document	Number	Rev	1.0(400)	
Custom	LA-G31P				
Date:	Wednesday, June 06, 2018	Sheet	41 of 76		

M.2 Slot-A Key-A (WLAN + BT)



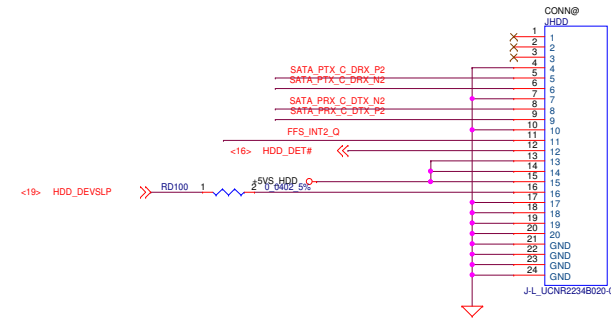
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				C	LA-G341P
				Date:	Wednesday, June 06, 2018
				Sheet	42 of 76
				Rev	1.0(00)

**M.2 Slot-C Key-M (SSD)**

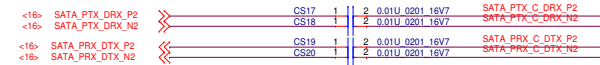
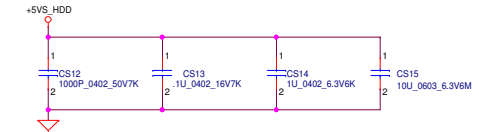


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					LA-6341P
Date:				Wednesday, June 06, 2018	Sheet 43 of 76

## HDD CONN

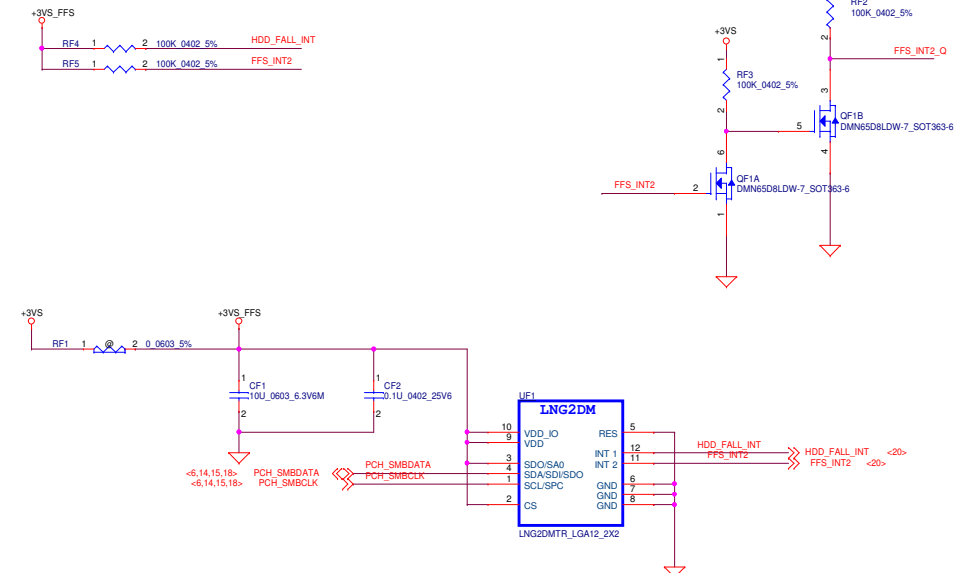


Place near HDD CONN (JHDD1)



## BYPASS Circuit

## Free Fall Sensor

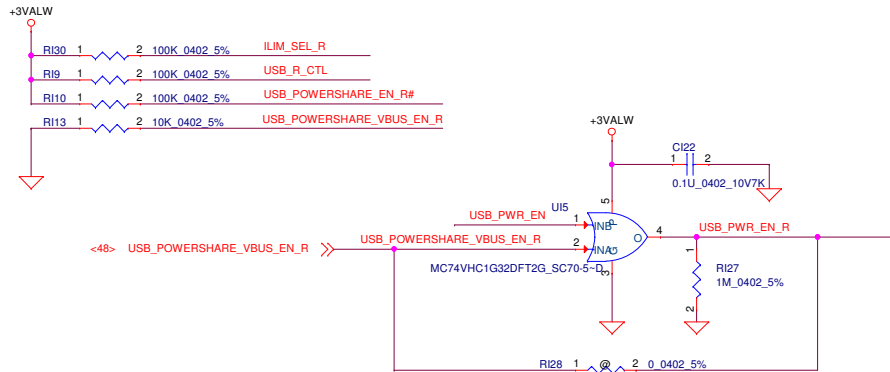


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				LA-G341P
				Rev
				1.0/000
				Date: Wednesday, June 06, 2018
				Sheet 44 of 76

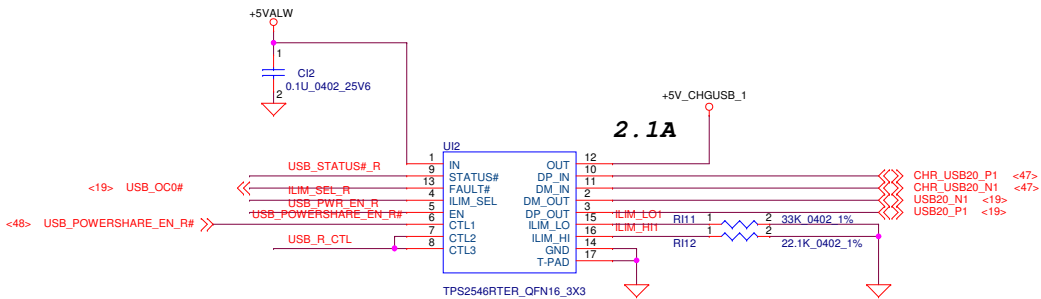
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

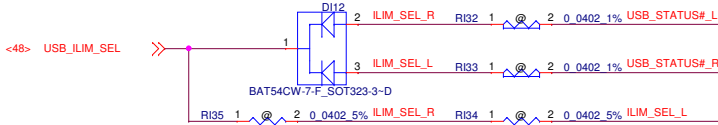
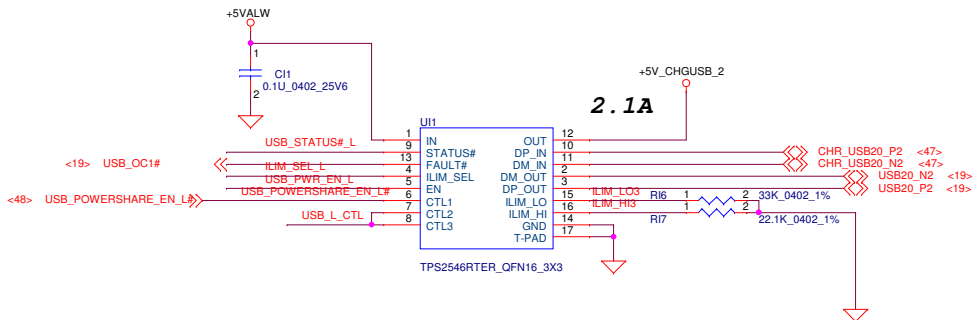
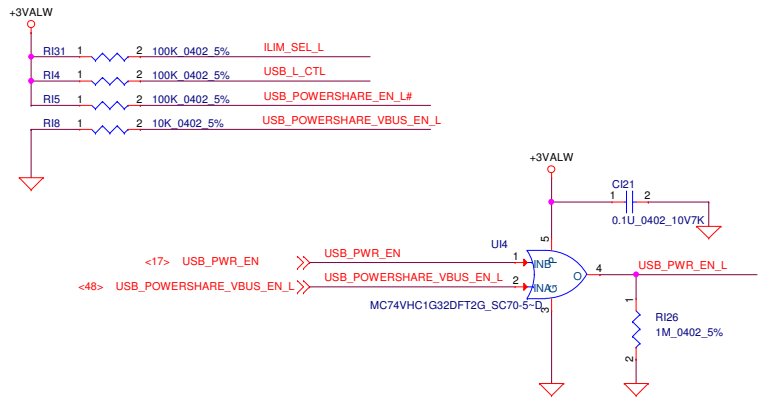
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

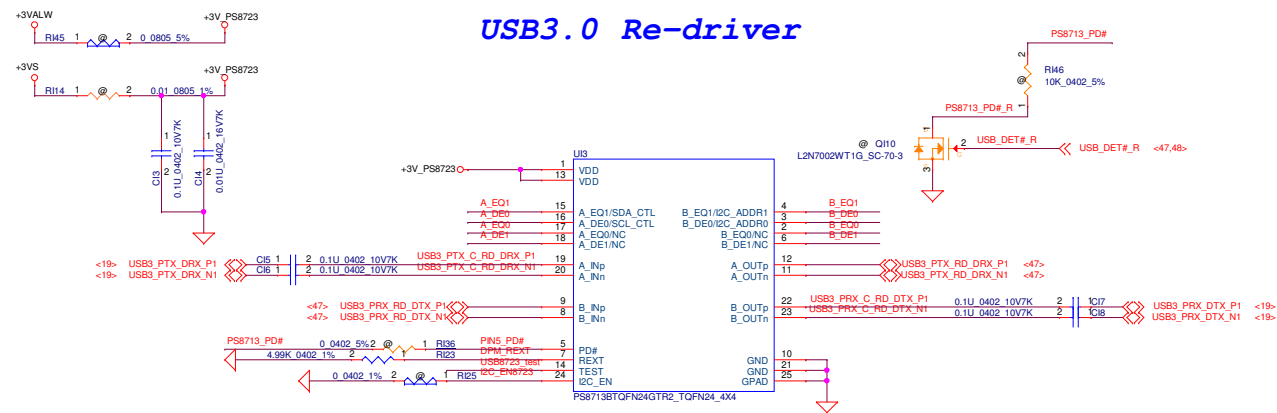
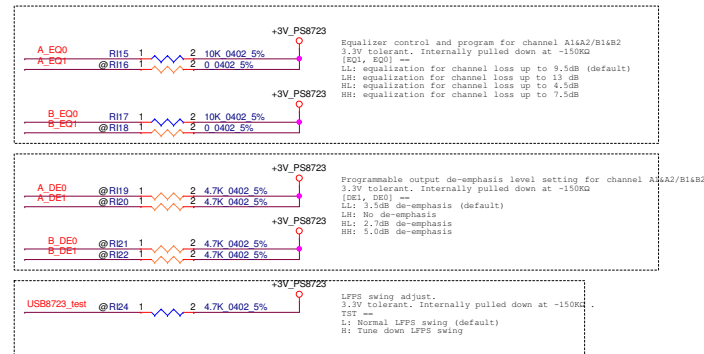


USB3.1 / USB2.0 Port1 (Right Side)



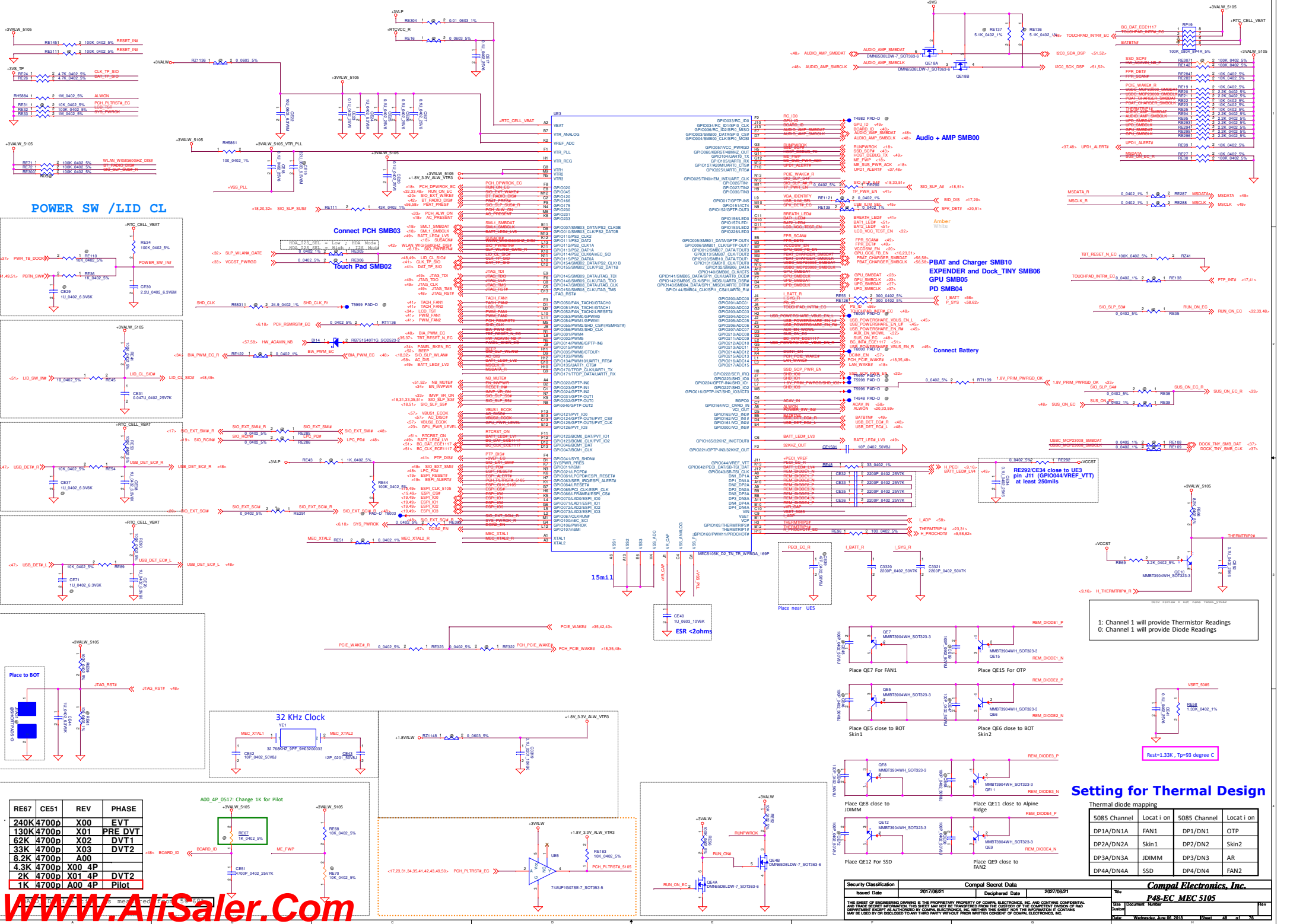
USB3.1 / USB2.0 Port2 (Left Side)











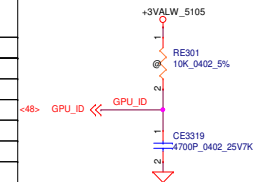
RE67	CE51	REV	PHASE
240K 4700p	X00	EVT	PRE DVT
130K 4700p	X01	DVT1	DVT1
62K 4700p	X02	DVT2	DVT2
33K 4700p	X03	DVT2	DVT2
4.3K 4700p	X00 4P	DVT2	DVT2
4.3K 4700p	X01 4P	DVT2	DVT2
1K 4700p	A00 4P	Pilot	Pilot

WWW.AliSaler.Com

1: Channel 1 will provide Thermistor Readings  
0: Channel 1 will provide Diode Readings

### Setting for Thermal Design

5085 Channel	Locat i on	5085 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDIMM	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2



The schematic diagram illustrates a battery gauge LED circuit. It consists of five LEDs (LED1 to LED5) connected to a +5VALW supply. Each LED is driven by a current source (RL1 to RL5) connected to a battery level input (BATT\_LED#\_LV1 to BATT\_LED#\_LV5). The current sources are implemented using 2N7002KDW\_SOT363-6 MOSFETs and 820 Ohm resistors. The MOSFETs are controlled by EC GPIO pins (Q4 to Q5) set to OD output. The LEDs are labeled LED1 to LED5, with part numbers 27-21-T3D-CPIQ2B16Y-3C\_WHITE. The circuit is powered by +3VALW and +5VALW supplies.

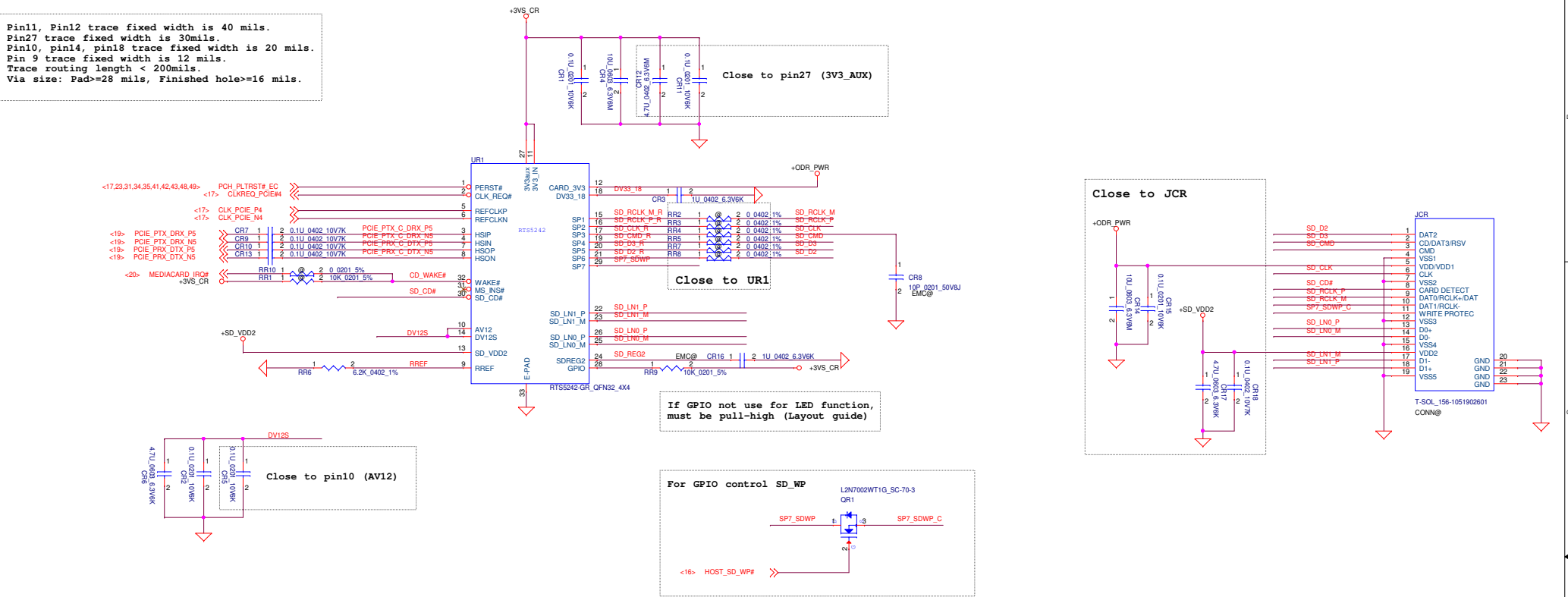
[illegible]

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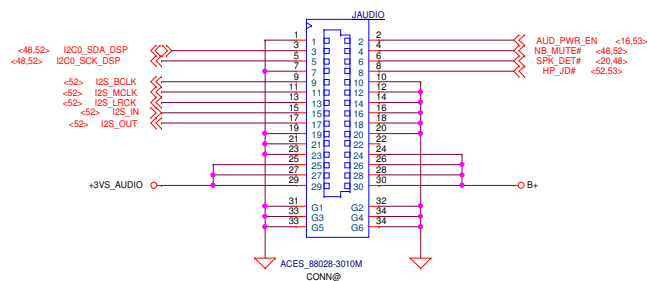
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Card Reader

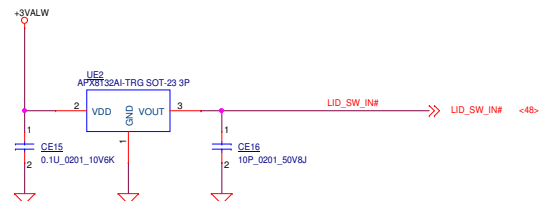
Pin11, Pin12 trace fixed width is 40 mils.  
Pin27 trace fixed width is 30mils.  
Pin10, pin14, pin18 trace fixed width is 20 mils.  
Pin 9 trace fixed width is 12 mils.  
Trace routing length < 200mils.  
Via size: Pad=>28 mils, Finished hole=>16 mils.



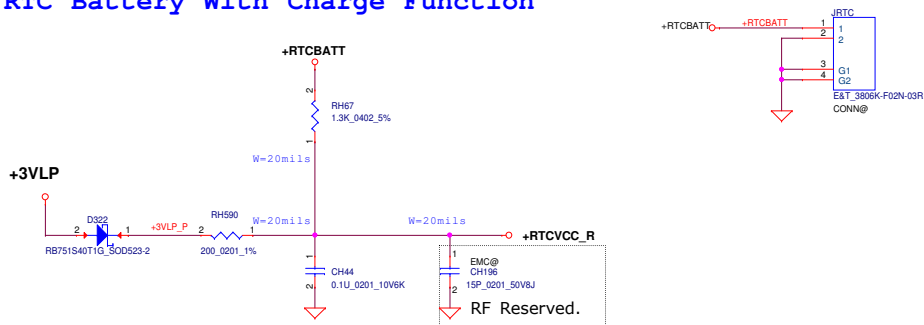
## AUDIO Board Conn.



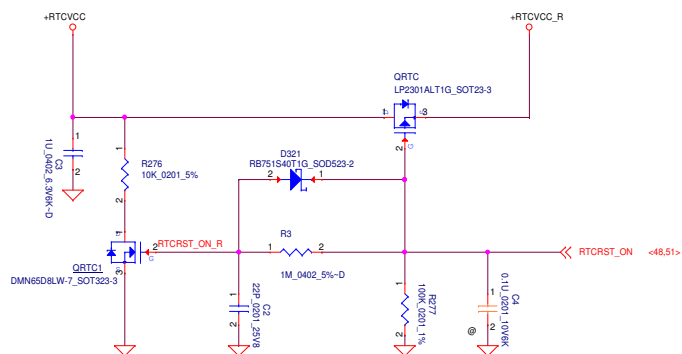
## Lid Switch



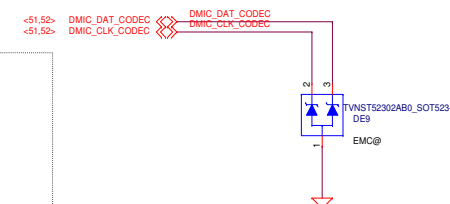
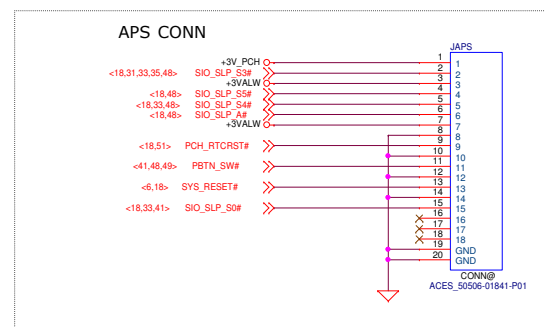
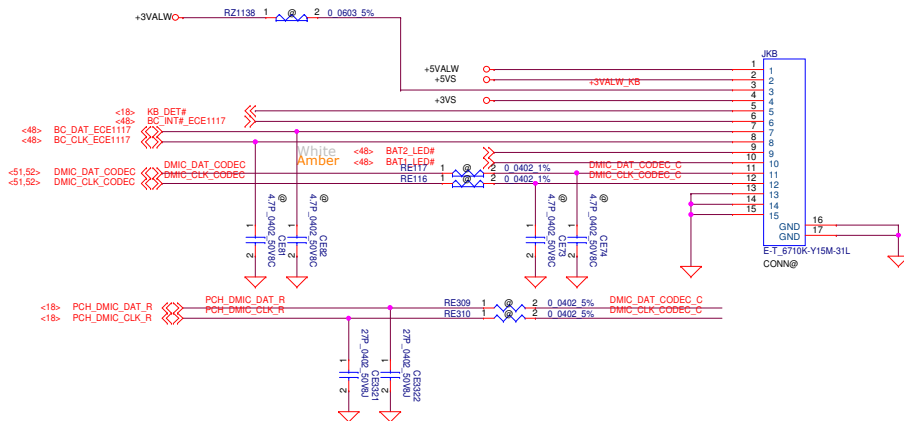
## RTC Battery With Charge Function



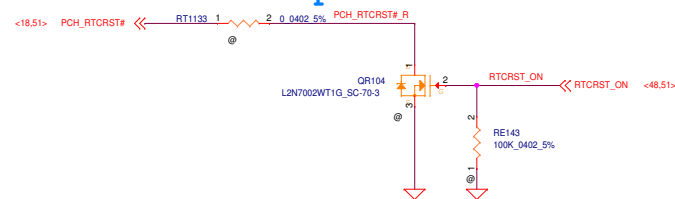
Default: OD\_EC drives GPIOs to LOW to turn off power to VCCRTC.



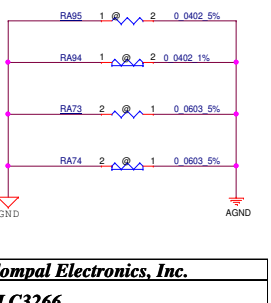
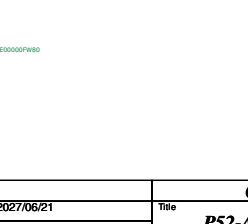
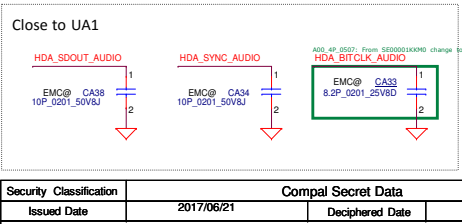
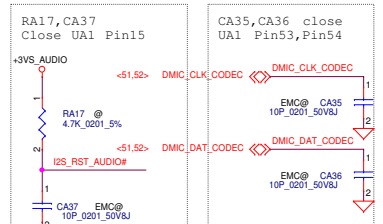
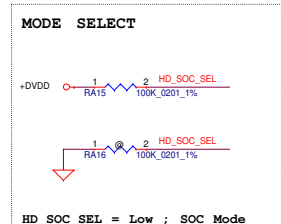
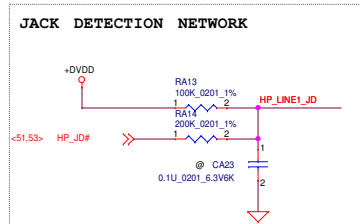
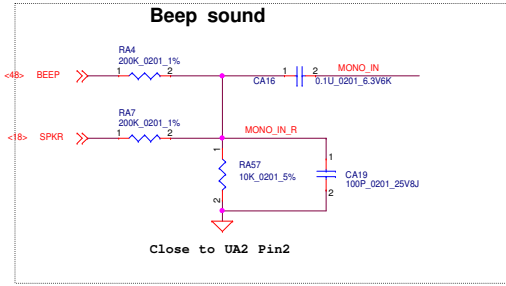
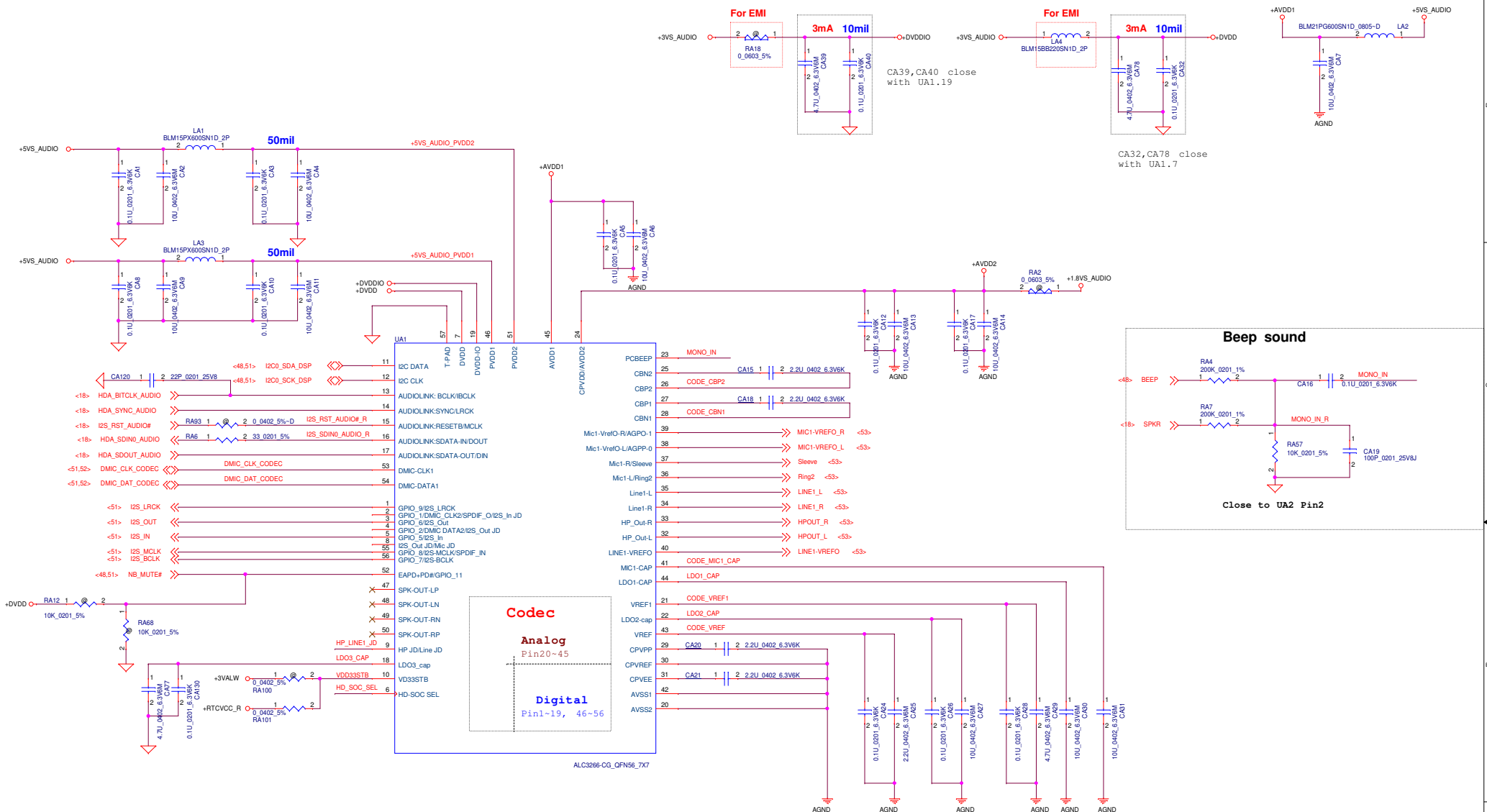
## Keyboard Controller board + DMIC



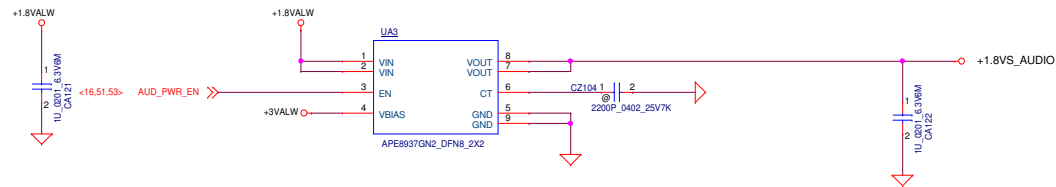
follow Intel Keep old RTC



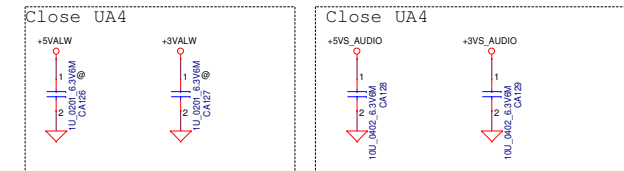
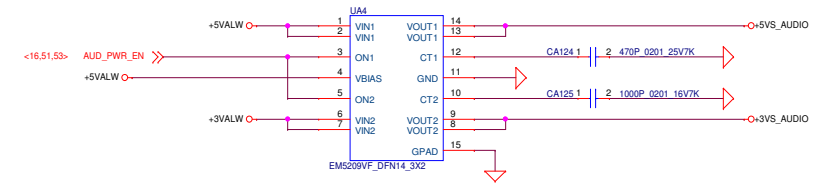
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					LA-G341P	1.0/A00
Date: Wednesday, June 06, 2018				Sheet	51	of 76



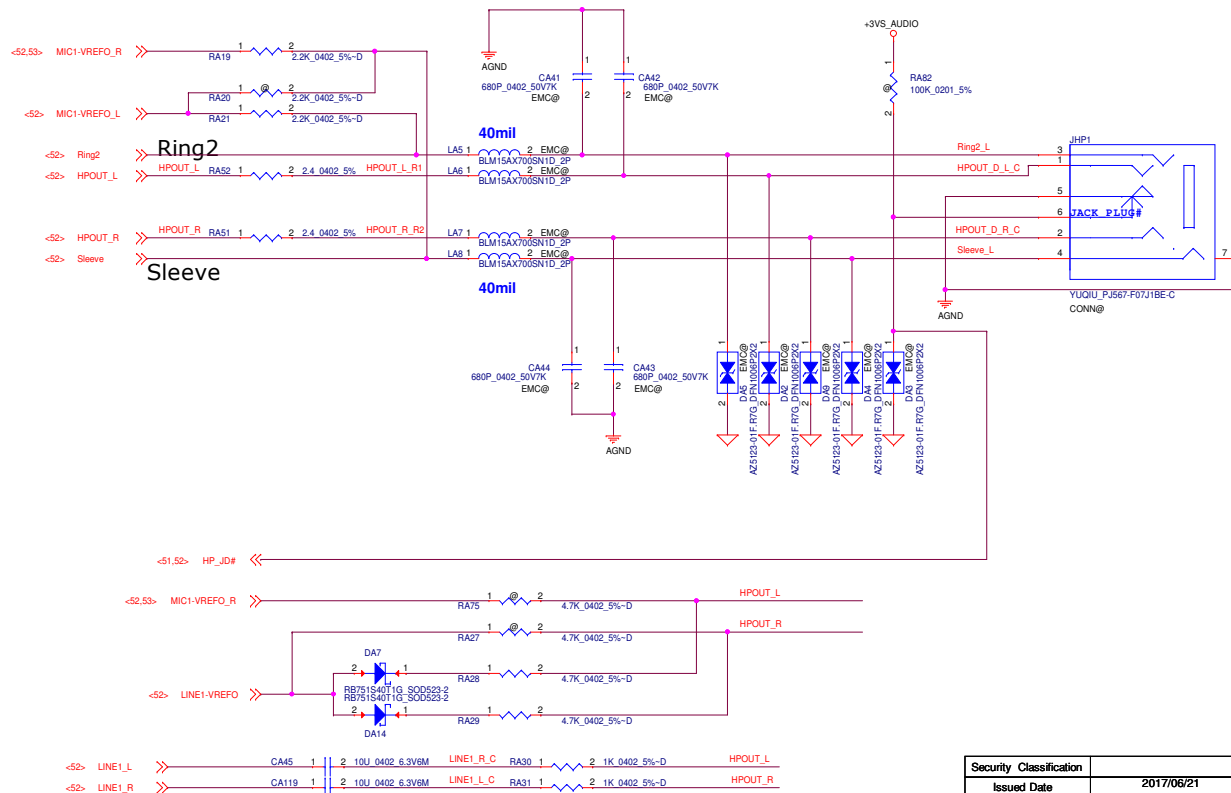
**+1.8VALW To +1.8VS\_AUDIO**



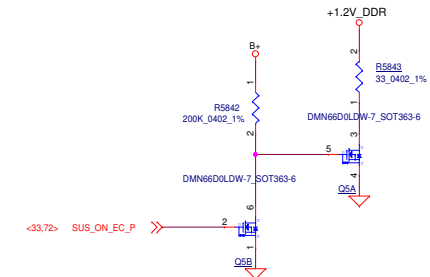
**+5VALW and +3VALW To +5VS\_AUDIO and +3VS\_AUDIO**



### ***Universal Audio Jack***



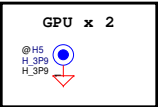
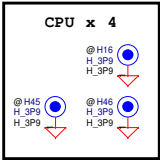
1.2V DDR dischager



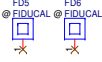
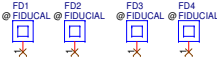
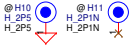
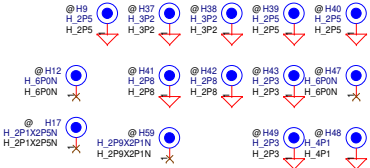
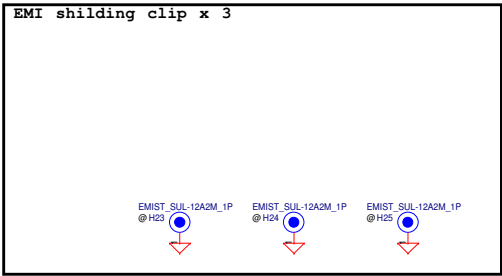
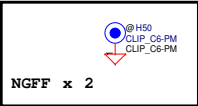
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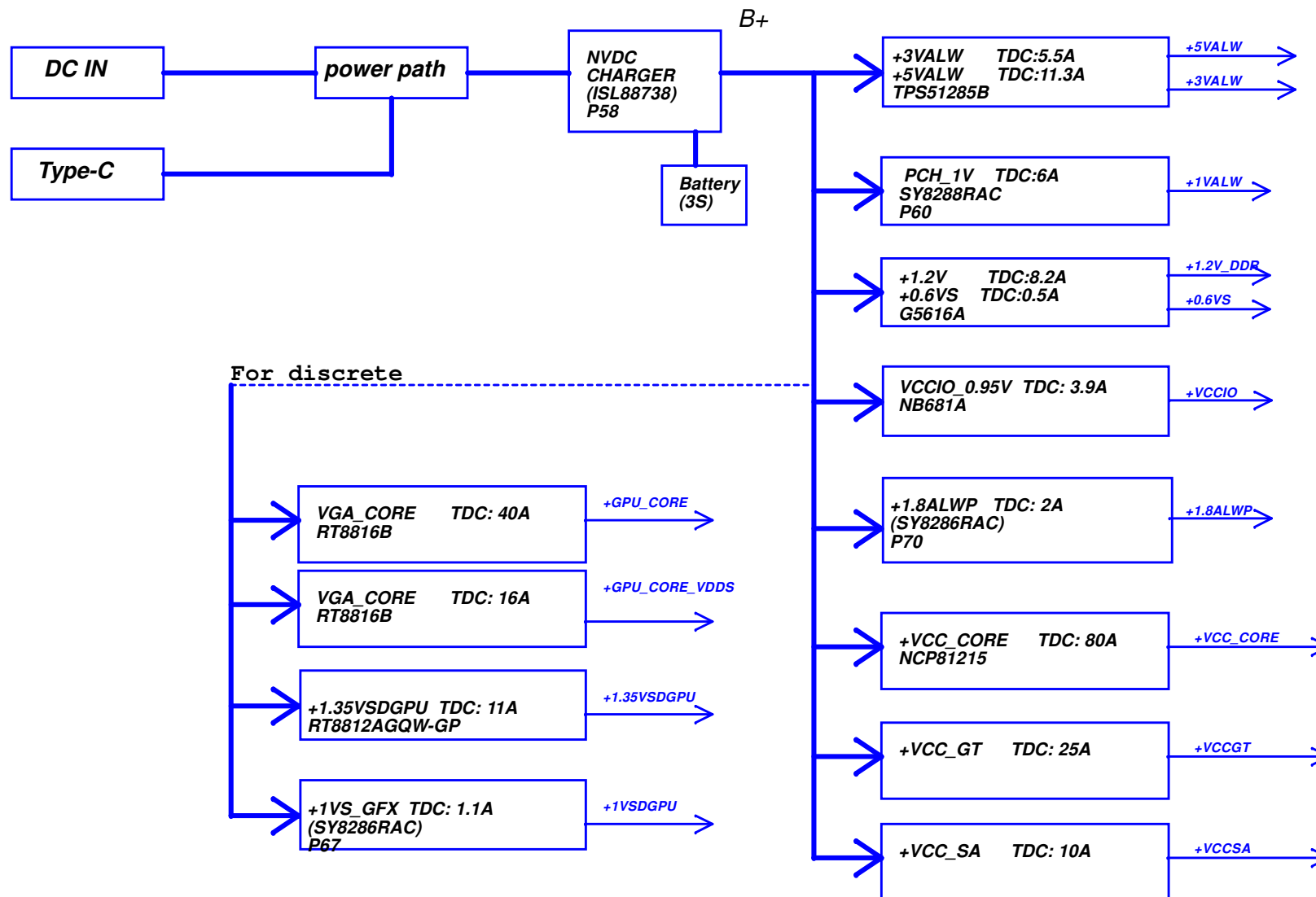


Screw Hole



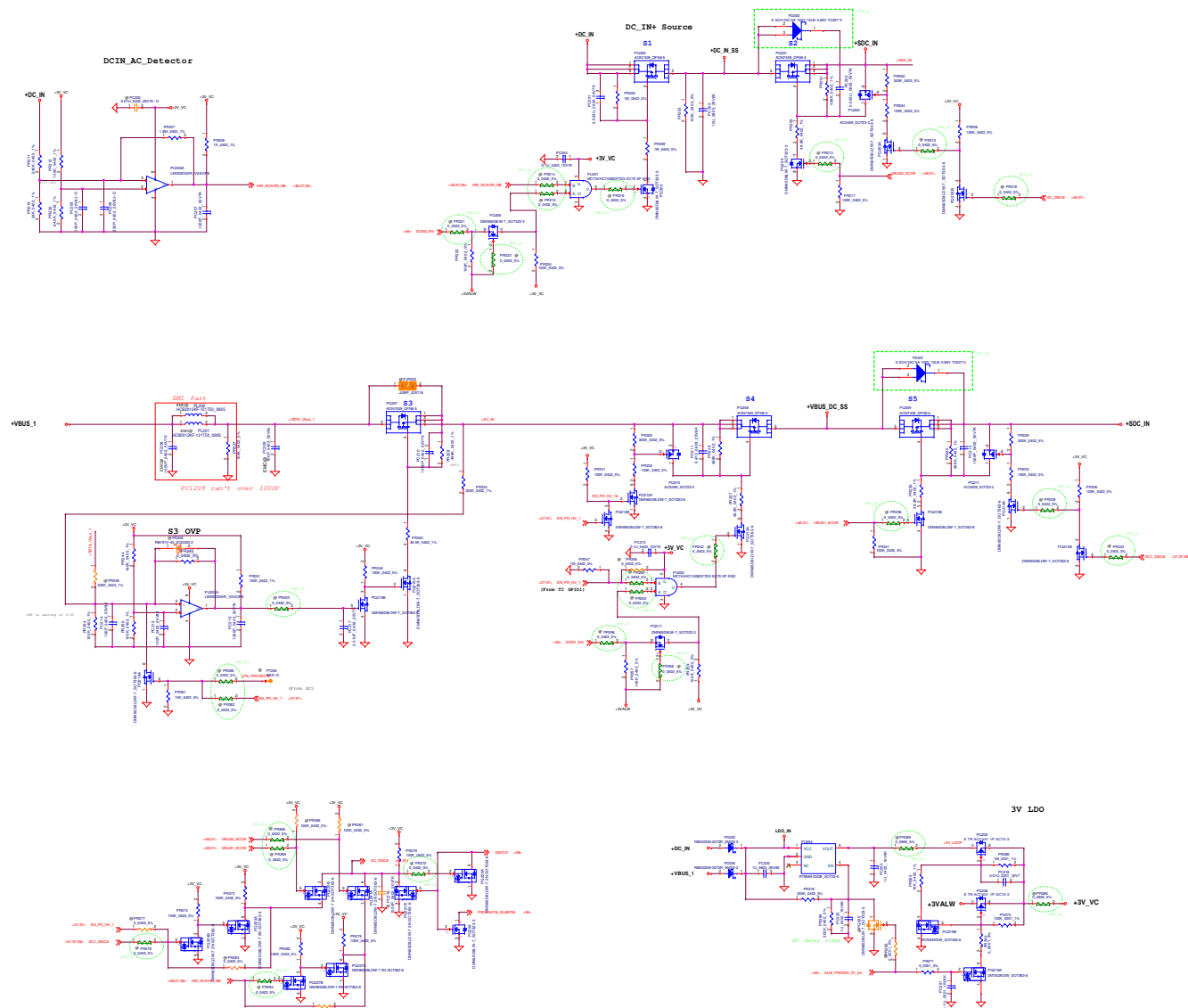
X03\_1222: for peel off issue,  
change footprint to CLIP\_C6-PM



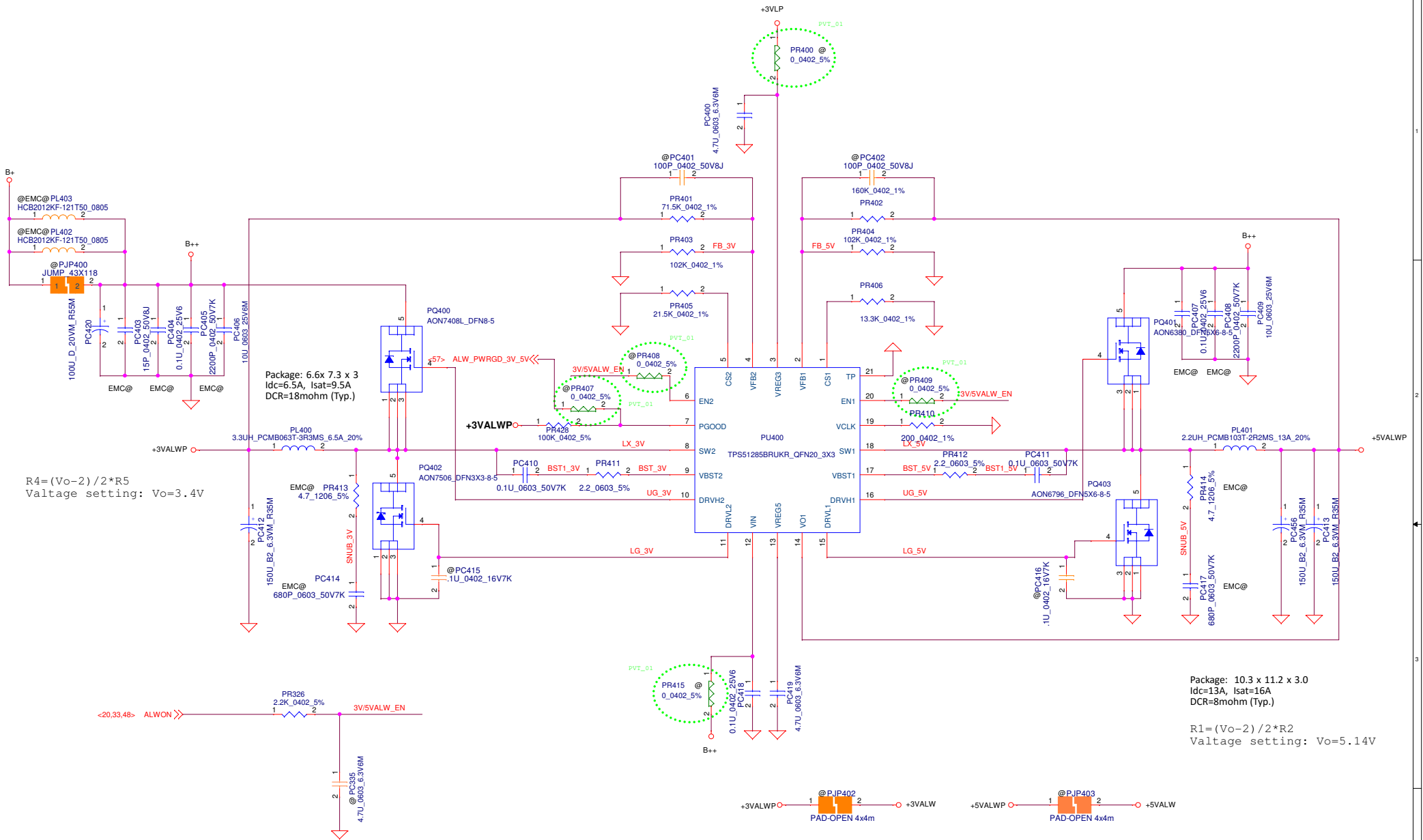


@ : Nopop Component  
 @DIS@ : Nopop Component  
 DIS@: POP for discrete GPU SKU









3.3VALWP  
TDC 5.5A  
Peak Current 7.7A  
OCP current 9.35A

5VALWP  
TDC 11.3A  
Peak Current 12.6A  
OCP current 19.2A

3V/5V controller(35.1), Support component(35.2)

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Title	P59-PWR 3.3VALWP/5VALWP		
Size	Document Number	Rev	
	LA-F541P	0.1(00)	
Date:	Wednesday, June 06, 2018	Sheet	59 of 74







Place close to Choke in VCCSA first phase circuit


Place close to Choke in VCORE first phase circuit

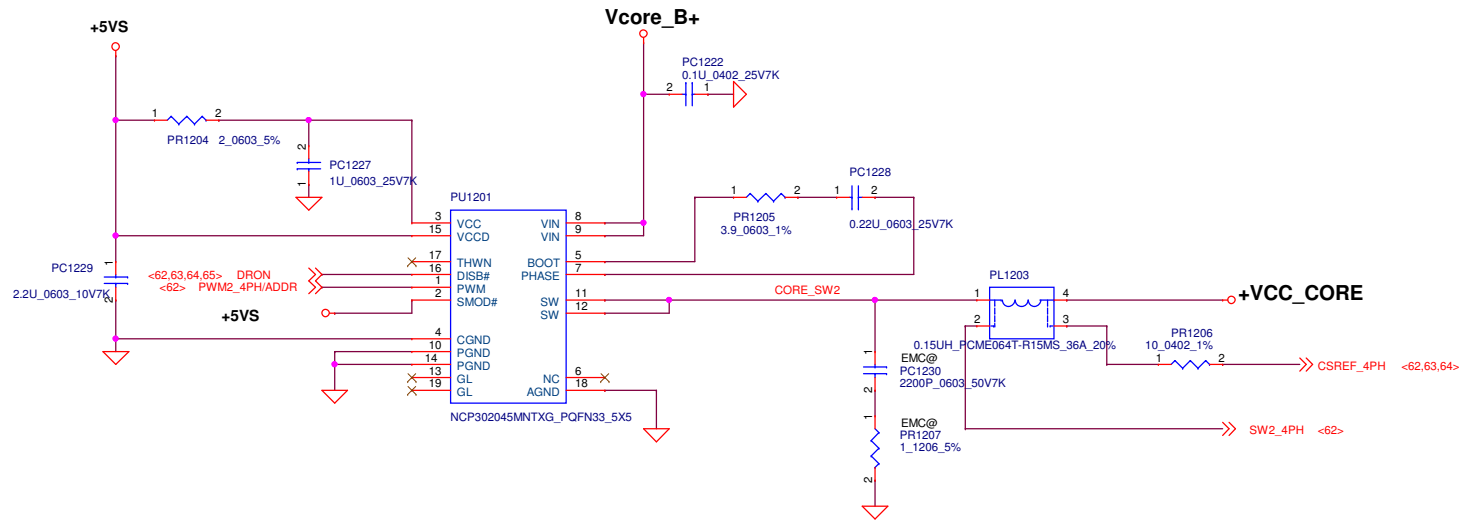
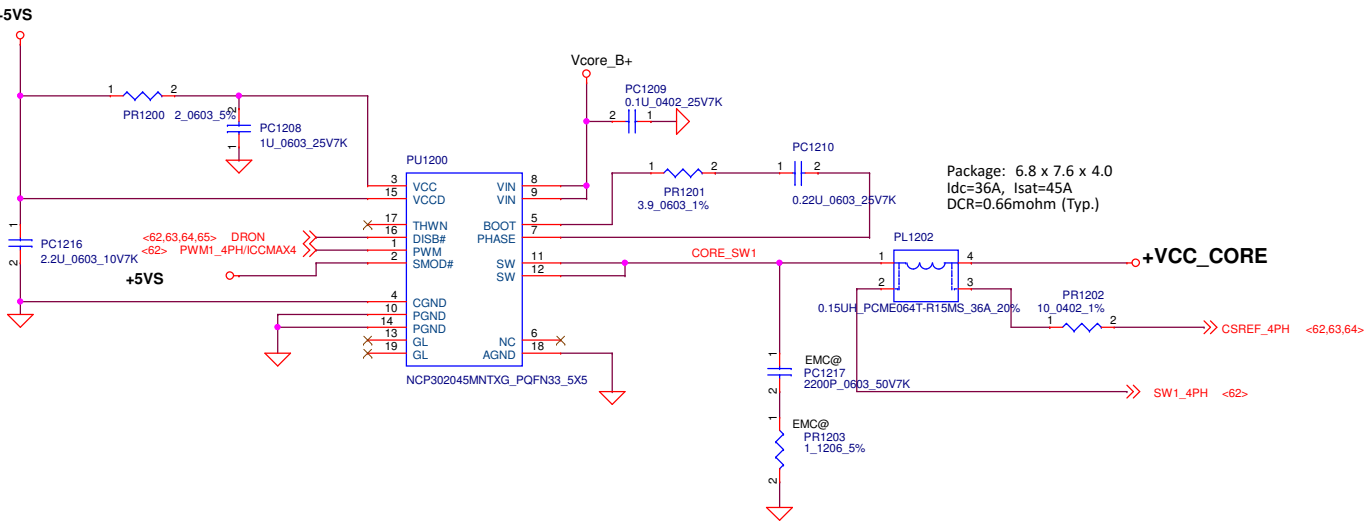
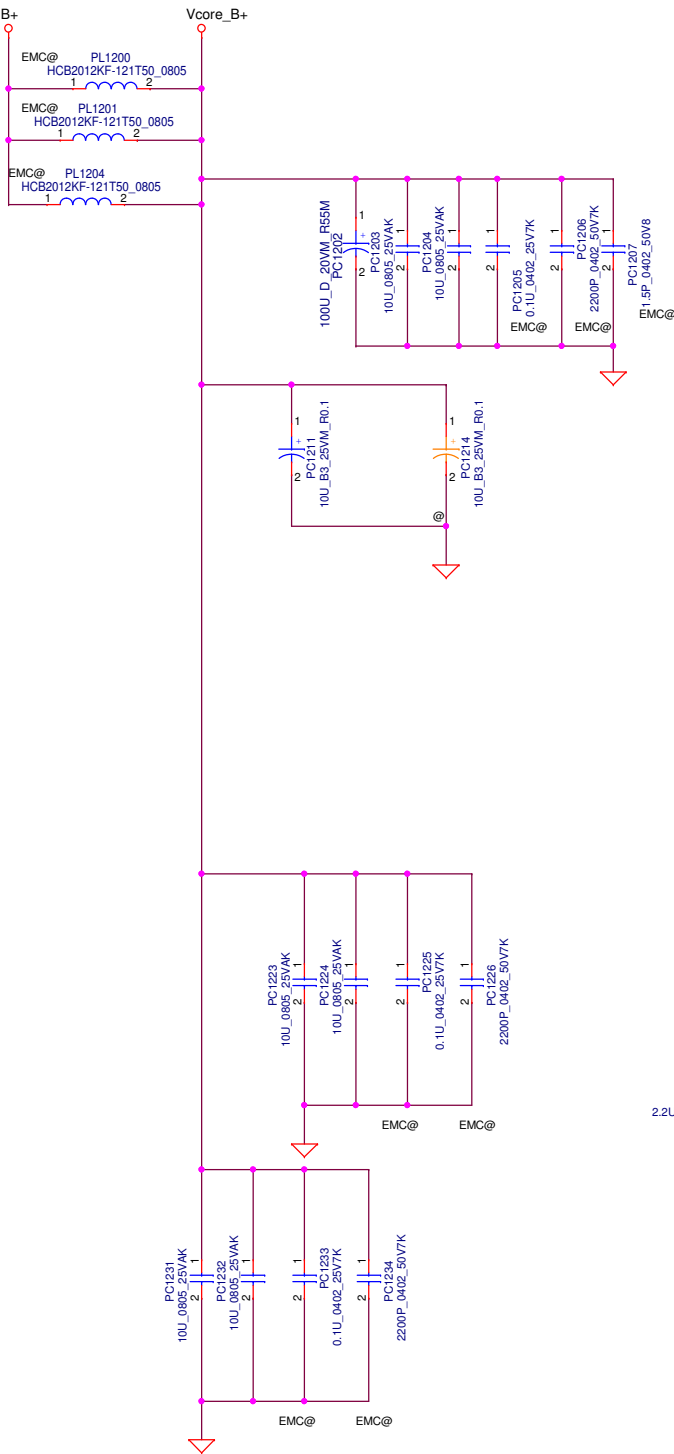
Place close to Choke in VCGT first phase circuit

RAIL NAME	Enable	V <sub>IN</sub>	V <sub>OUT</sub>	I <sub>CCMax</sub>	I <sub>PL2</sub>
V <sub>CC</sub> (MVP8)	VR_EN	VDC	SVID	128.0 A	80.0 A
V <sub>CGT</sub> (MVP8)	VR_EN	VDC	SVID	32.0 A	25.0 A
V <sub>CSA</sub> (MVP8)	VR_EN	VDC	SVID	11.1 A	10.0 A

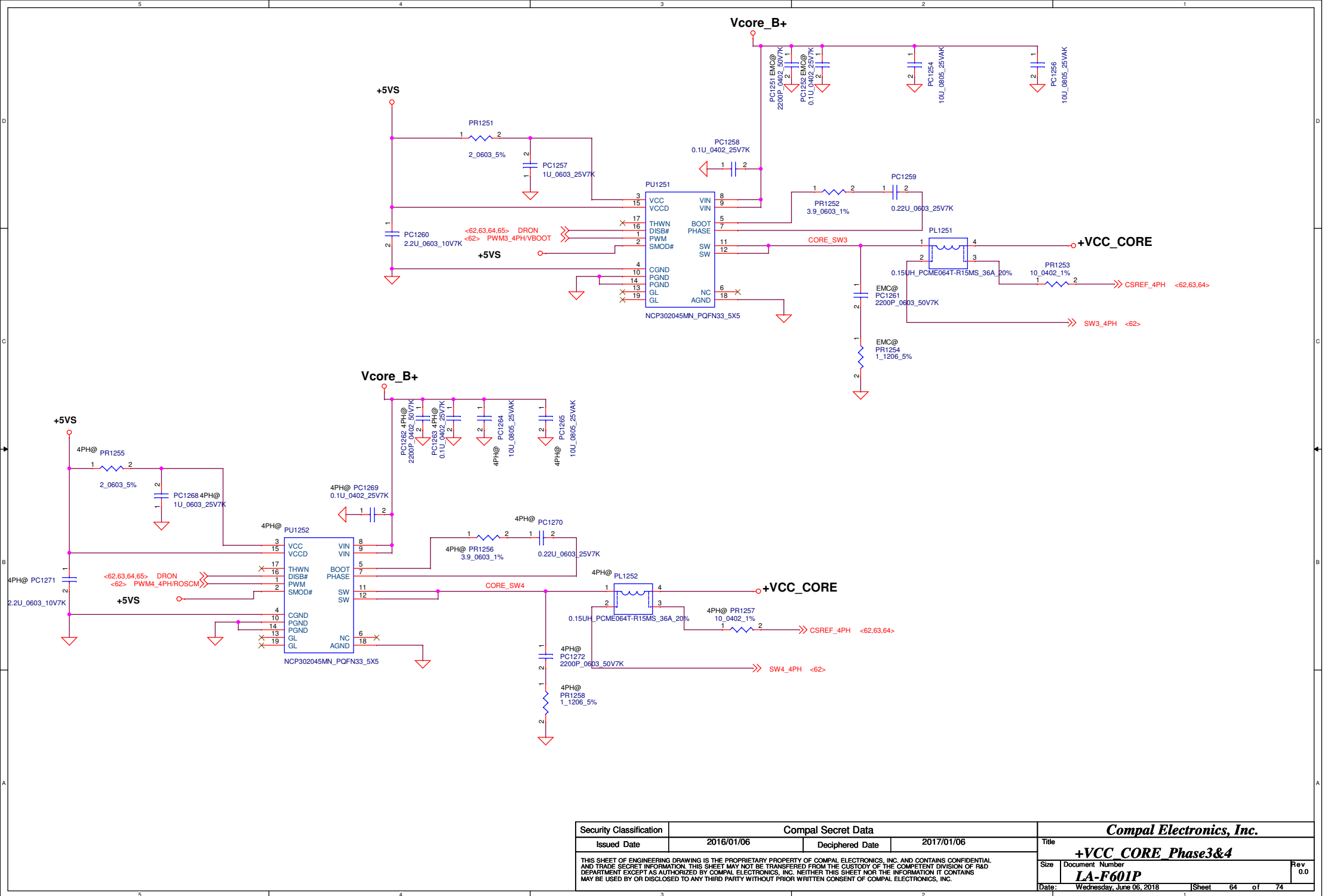
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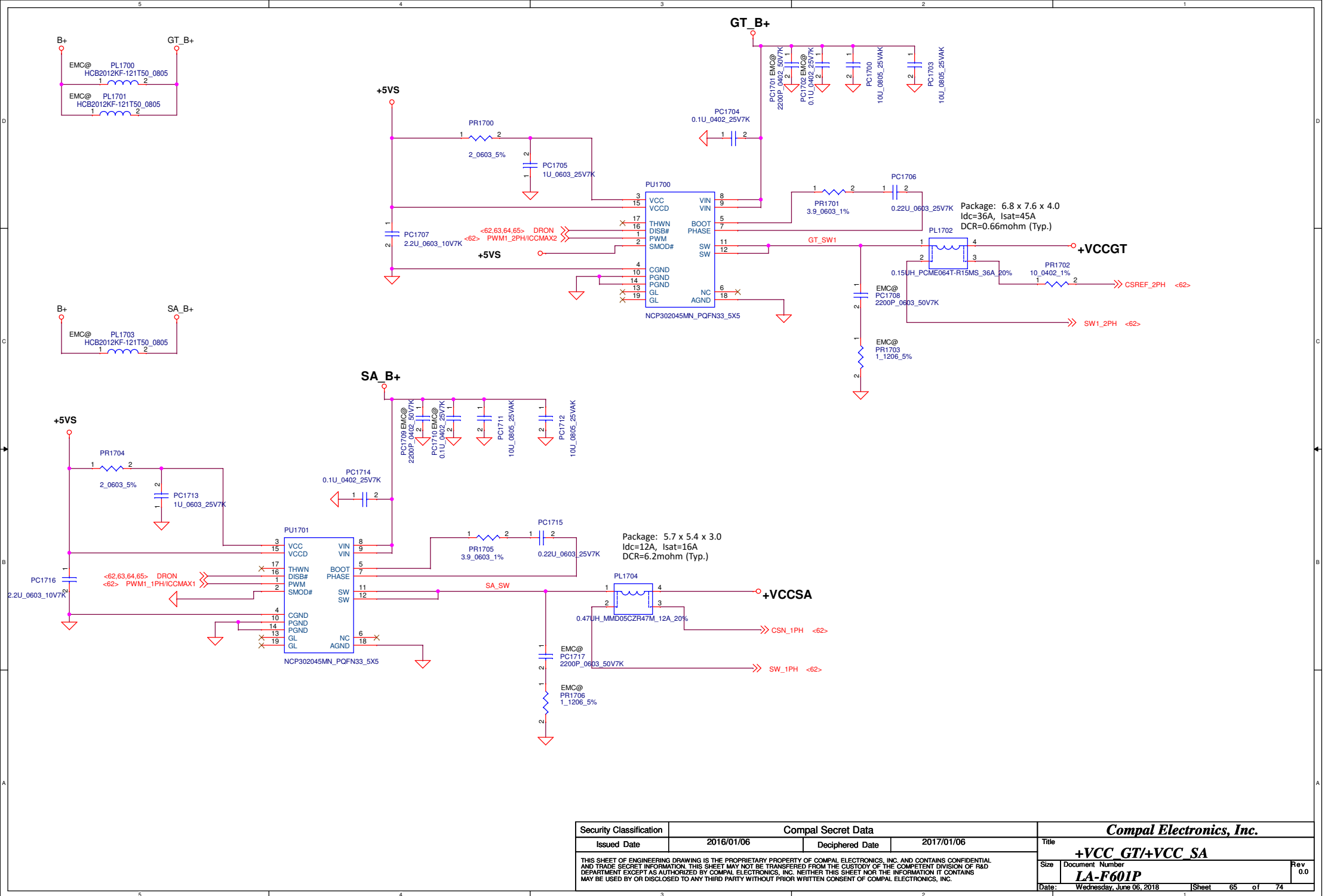
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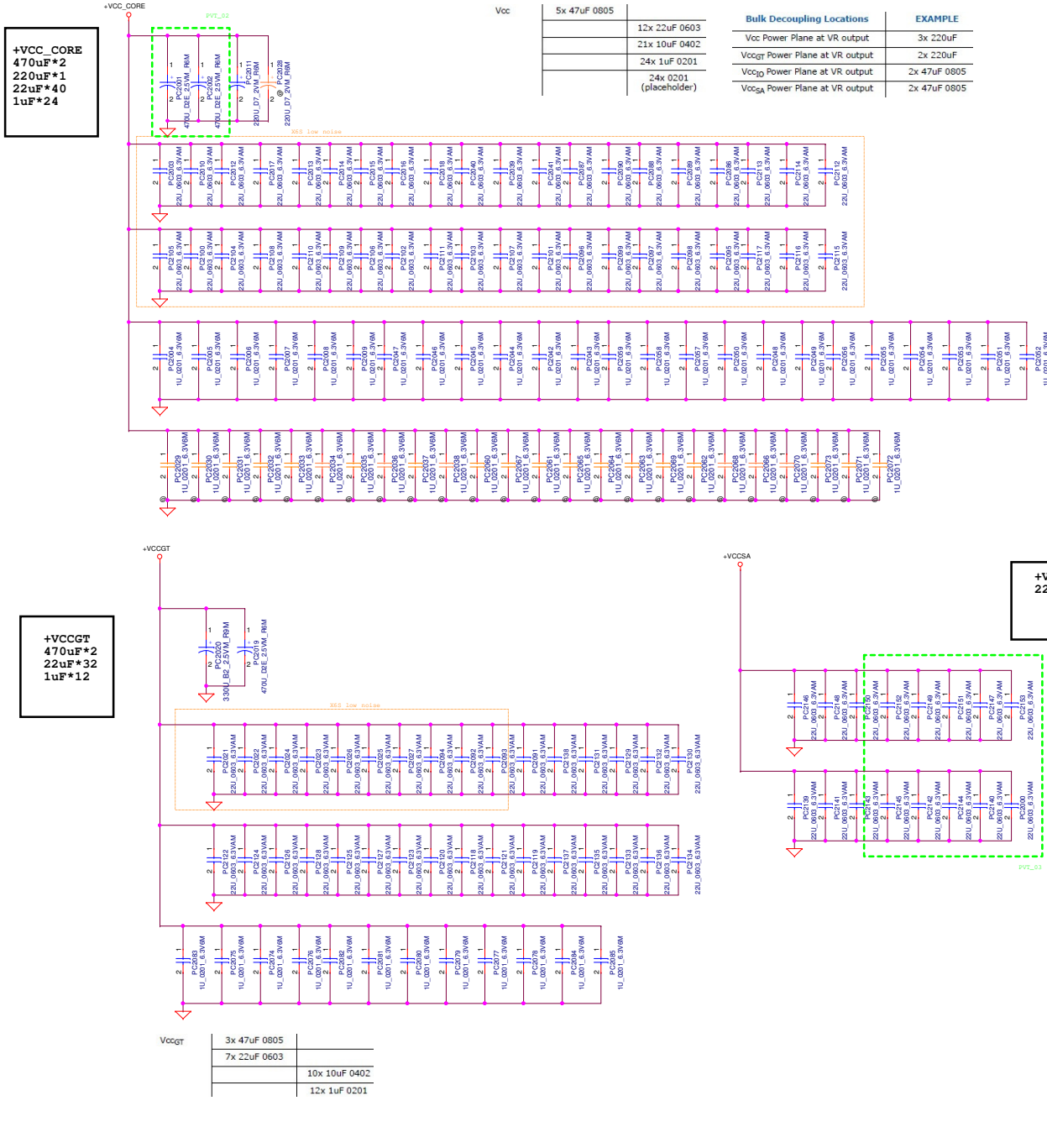
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		NCP81215	
Size	Document Number	LA-F601P	
Date	Wednesday, June 06, 2018	Sheet	82 of 74



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Size	Document Number	Rev		0.0	
LA-F601P		Date		Wednesday, June 06, 2018	
Sheet		63		of 74	







VCCSA	2x 47uF 0805	
	2x 22uF 0805	
	7x 10uF 0402	

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				Date	Wednesday, June 06, 2018
				Sheet	98 of 74

+1.0VSP/1.05VSP
TDC 1.1A
Peak Current 1.1A
OCP current 6A(fix)



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Issued Date		2017/06/21		Deciphered Date	
				2027/06/21	
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				P67-PWR +1.05VSDGPU(SY8286RAC)	
				Size	Document Number
					Rev
				0.1(100)	
				LA-F541P	
Date:				Wednesday, June 06, 2018	
Sheet				67 of 74	

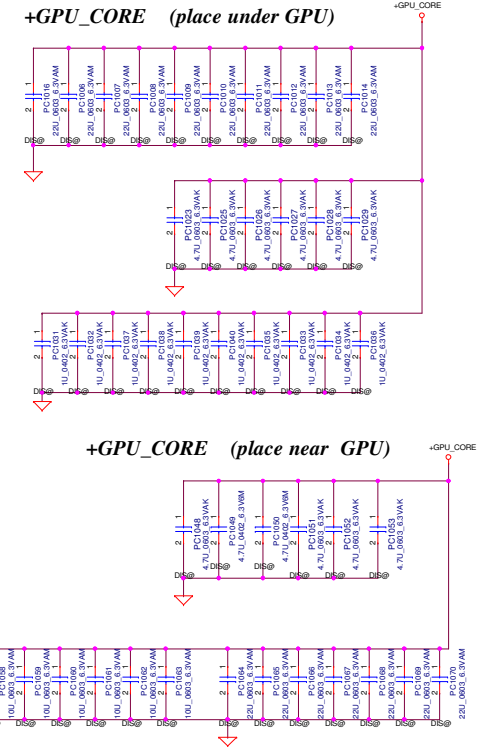
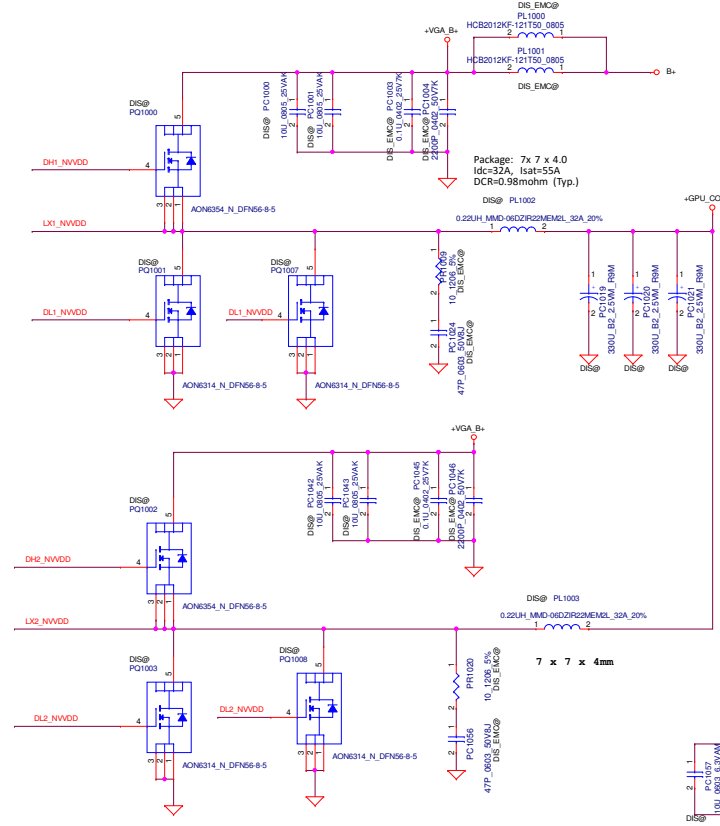
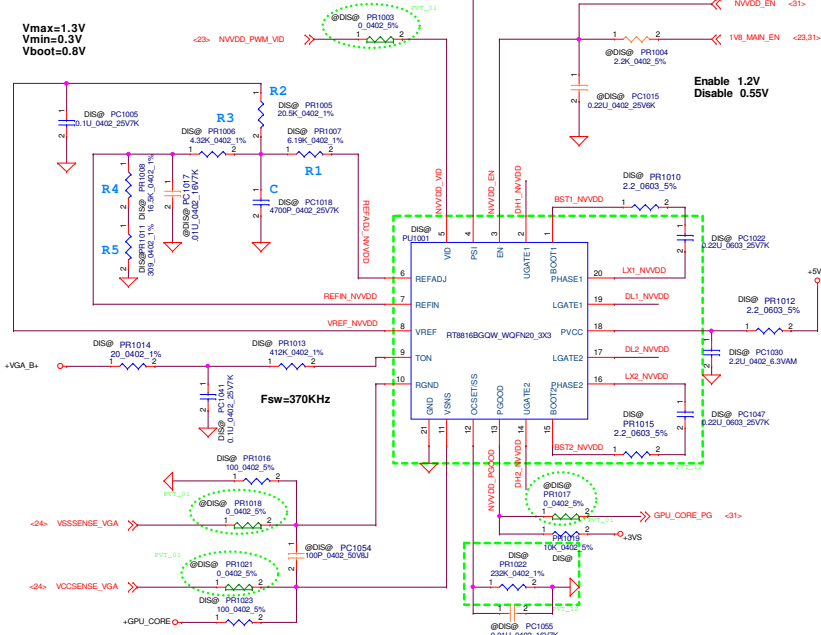


for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

GPU\_CORE (0.95V)  
TDC 41A  
Peak Current 94A  
OCP current 100A  
DCR 0.98mohm +/- 5%

MIN MAX  
H/S Rds(on) : 4mohm , 5.2mohm  
L/S Rds(on) : 2.8mohm , 3.5mohm



Under:  
4.7U\_0603\_6.3VAK \*16  
1U\_0402\_6.3VAK \*10

Near:  
10U\_0805\_6.3V6M\*7  
22U\_0805\_6.3V6M \*7  
4.7U\_0805\_6.3V6K \*6  
330u\*3

VGA\_CORE controller(43.1), Support component(43.2)  
VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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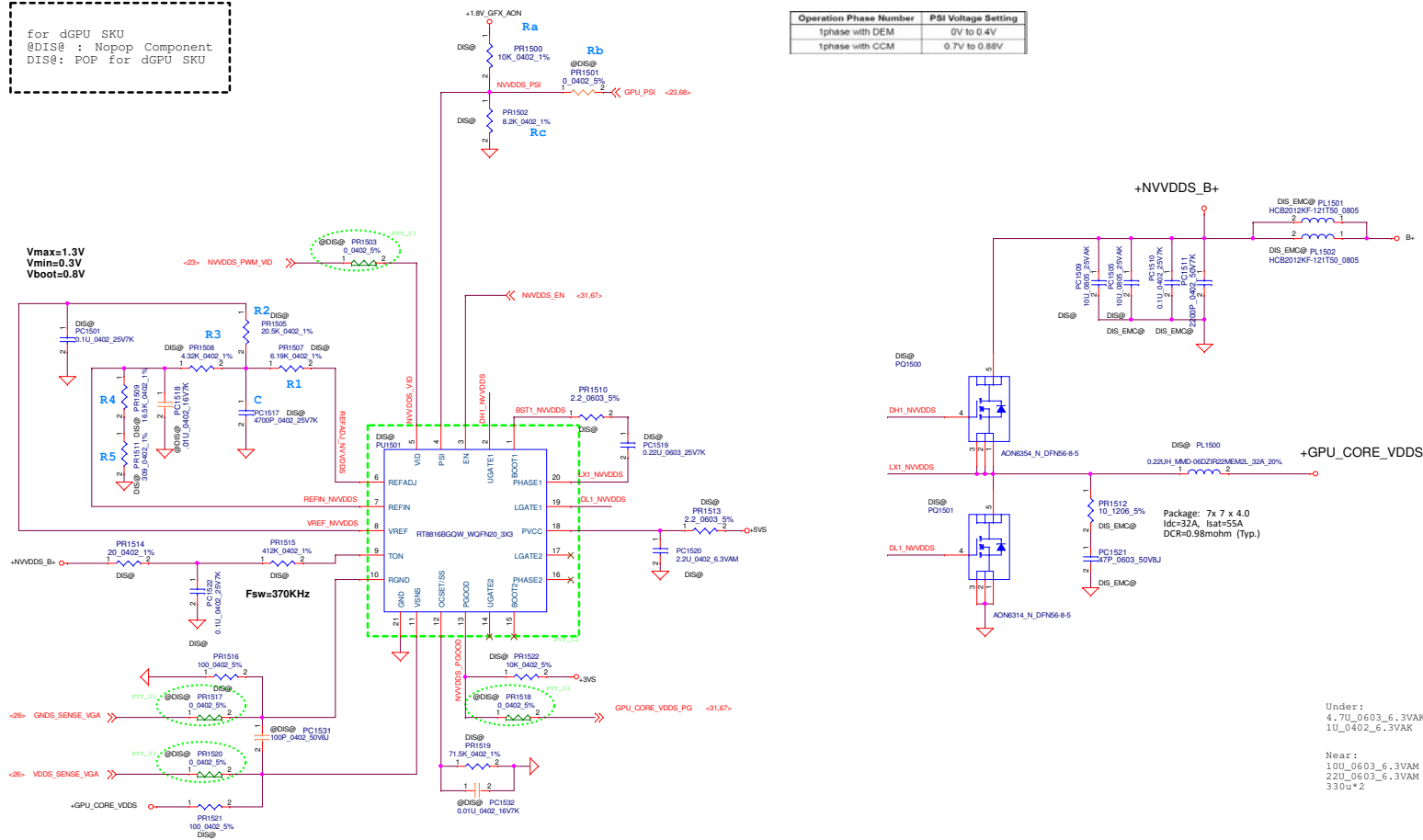
		Compal Electronics, Inc.	
		P68-PWR+GPU CORE	
Size	Document Number	LA-F541P	Rev 01000
Date	Wednesday, June 06, 2018	Sheet 08	of 74

for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU

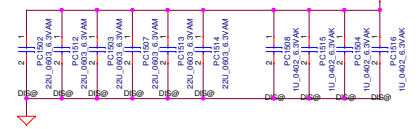
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

+GPU\_CORE\_VDDS  
TDC I2A  
Peak Current 16A  
OCP current 21A  
DCR 0.98mohm +/- 5%

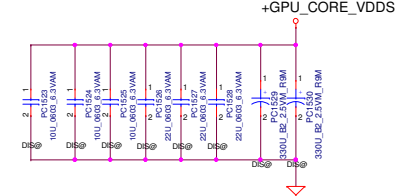
H/S Rds (on) : 3.7mohm , 4.5mohm  
L/S Rds (on) : 1.5mohm , 1.9mohm



NVVDDS (place under GPU)



NVVDDS (place near GPU)



Under:  
4.7U\_0603\_6.3VAK \*6  
1U\_0402\_6.3VAK \*4  
Near:  
100\_0603\_6.3VAK \*3  
22U\_0603\_6.3VAK \*3  
330u\*2

VGA\_CORE controller(43.1), Support component(43.2)  
VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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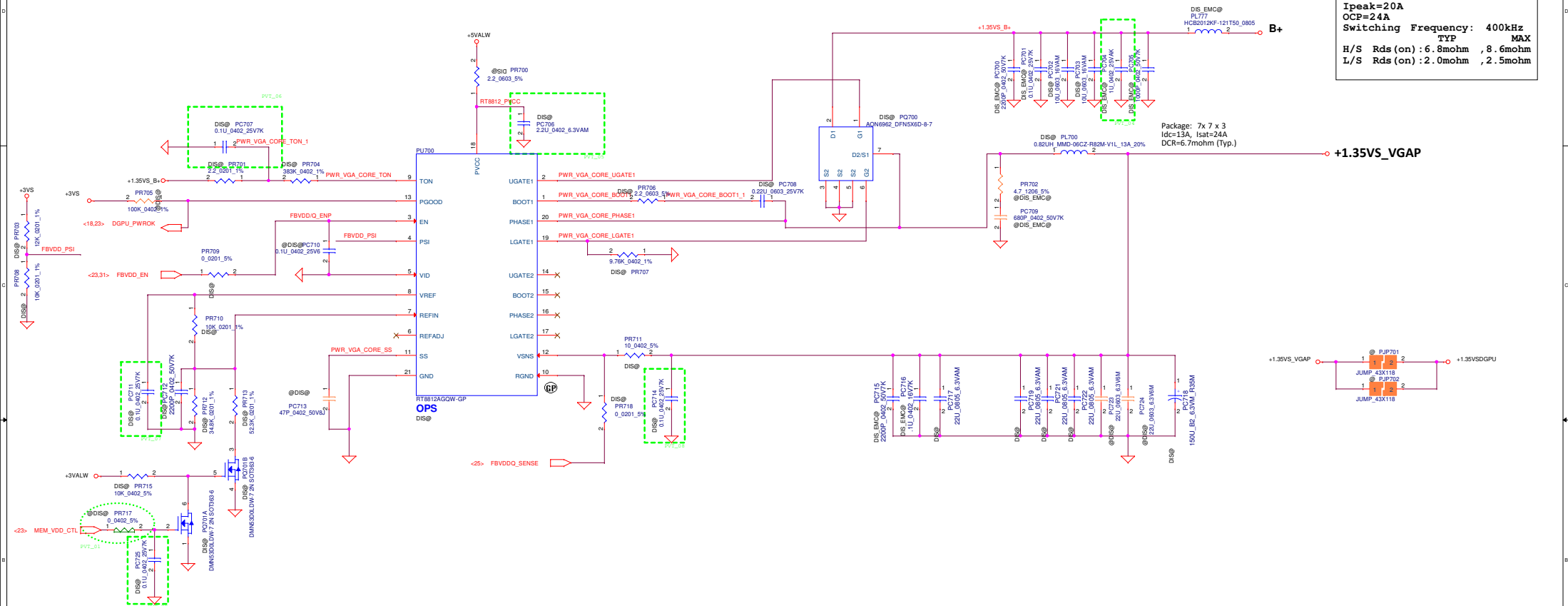
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Compal Electronics, Inc.			
P69-PWR+GPU CORE VDDS			
LA-F541P			
Size	Document Number	Rev	01000
Date	Wednesday, June 06, 2018	Sheet	89 of 74

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for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
```



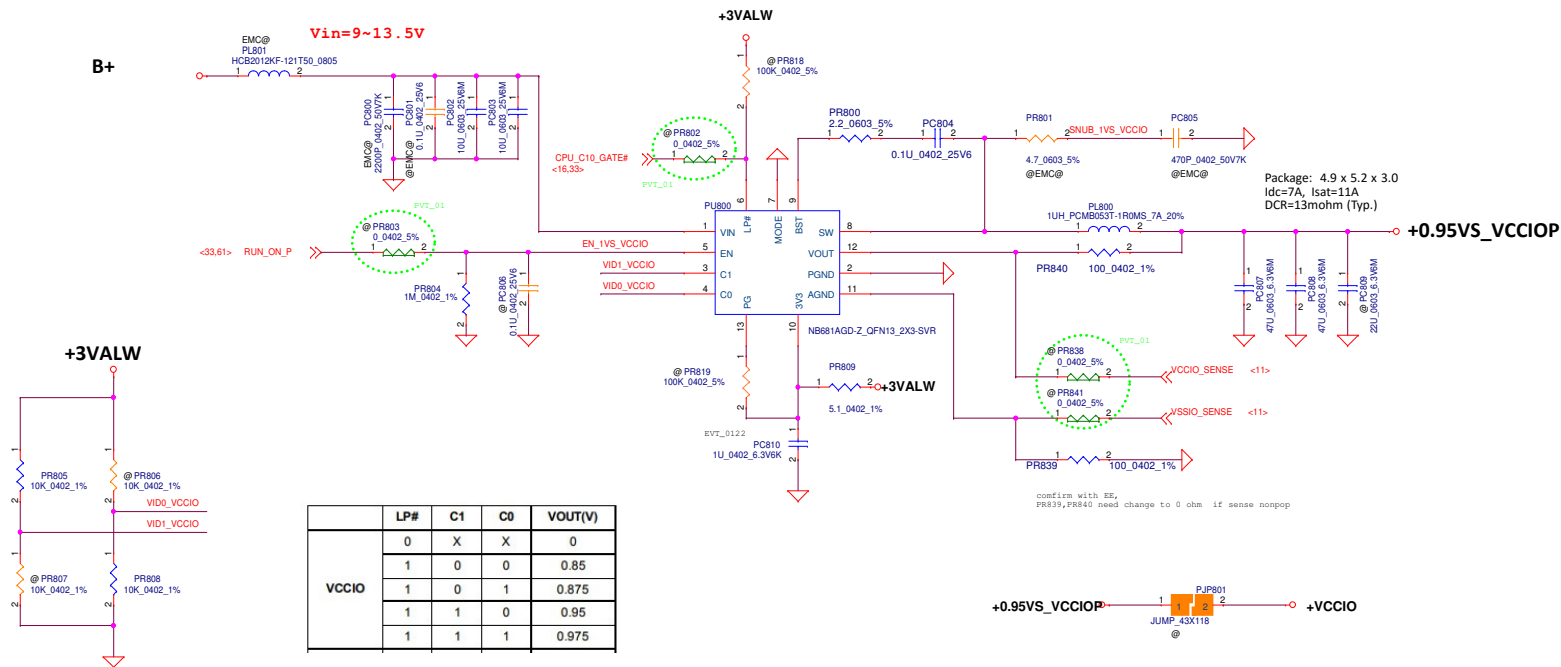
Security Classification		Compal Secret Data		Title	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	<b>Compal Electronics, Inc.</b> <b>PWR +1.35VRAM</b> Size: 600mm x 400mm <b>LA-E994P</b>	
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2.5V\_MEM controller(35.13), Support component(35.14)

```
+2.5V_MEM
TDC 0.86A
Peak Current 1A
OCP Current 1.46A
```



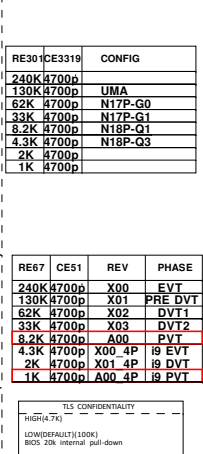
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title		
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				Size	Document Number	Rev
					<b>LA-F541P</b>	0.10
				Date:	Wednesday, June 06, 2018	Sheet 72 of 74



**+0.95VS\_VCCIO**  
 TDC 3.9A  
 Peak Current 5.5 A  
 OCP Current 6.6 A Fix by IC  
 TYP MAX

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
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35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

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RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	PVT
4.3K	4700p	X00_4P	i9 EVT
2K	4700p	X01_4P	i9 DVT
1K	4700p	A00_4P	i9 PVT

<p>----- TLS CONFIDENTIALITY -----</p> <p>HIGH(4.7K)</p> <p>LOW(DEFAULT)(100K)</p> <p>BIOS 20k internal pull-down</p>
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## Y76

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**L11**



