N-Channel 12 V (D-S) MOSFET

DESCRIPTION

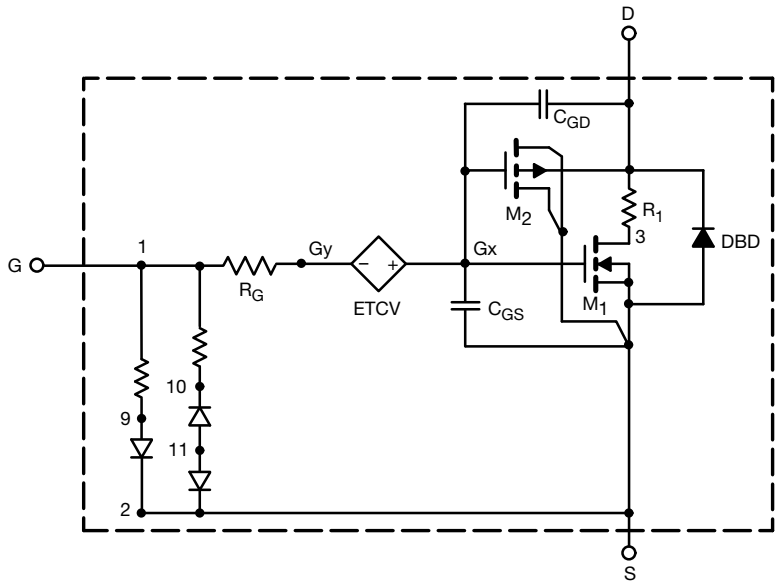
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

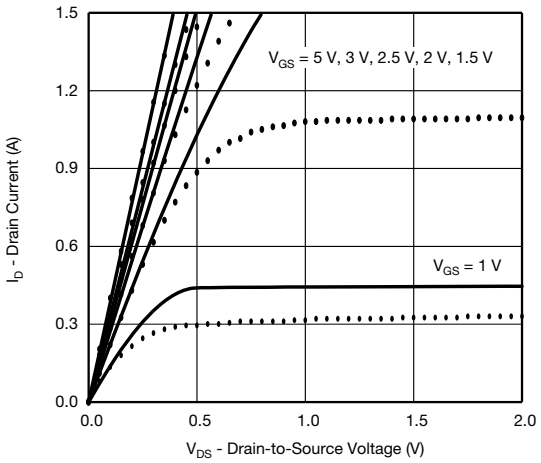
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.50	-	V
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.5 A	0.27	0.27	Ω
		V_{GS} = 2.5 V, I_D = 0.2 A	0.32	0.31	
		V_{GS} = 1.8 V, I_D = 0.1 A	0.38	0.37	
		V_{GS} = 1.5 V, I_D = 0.1 A	0.44	0.42	
		V_{GS} = 1.2 V, I_D = 0.05 A	0.55	0.55	
Forward transconductance [a]	g_{fs}	V_{DS} = 6 V, I_D = 0.5 A	2	1.6	S
Diode forward voltage	V_{SD}	I_S = 0.5 A	0.70	0.70	V
Dynamic [b]					
Input capacitance	C_{iss}	V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz	29	21	pF
Output capacitance	C_{oss}		14	13	
Reverse transfer capacitance	C_{rss}		8	7	
Total gate charge	Q_g	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 0.5 A	0.32	0.47	nC
Gate-source charge	Q_{gs}		0.04	0.04	
Gate-drain charge	Q_{gd}		0.07	0.09	

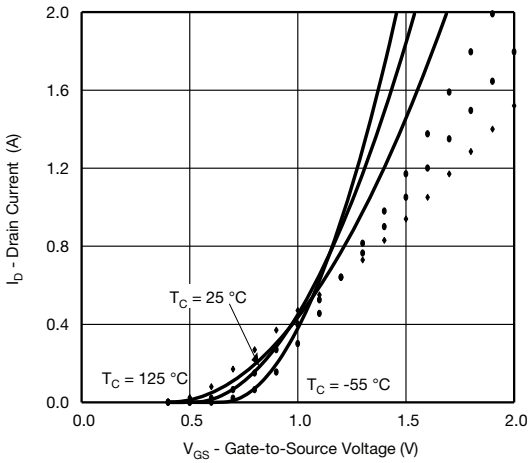
Notes

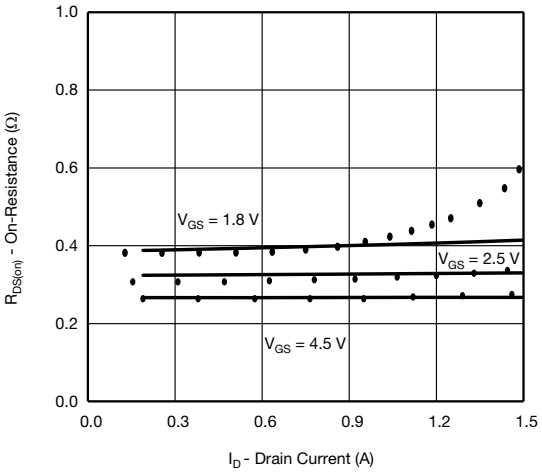
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

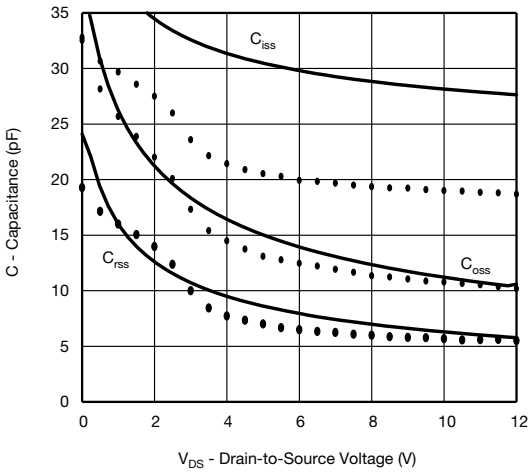
b. Guaranteed by design, not subject to production testing

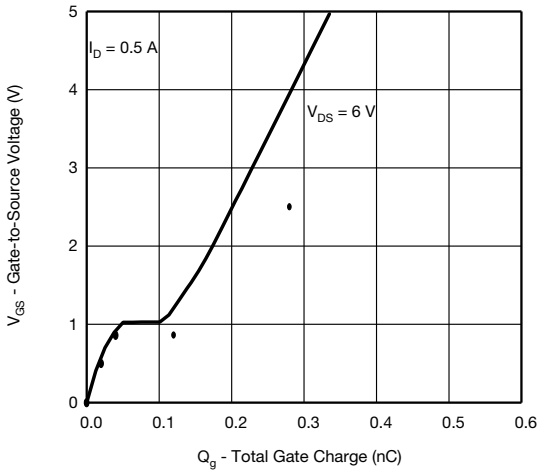
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

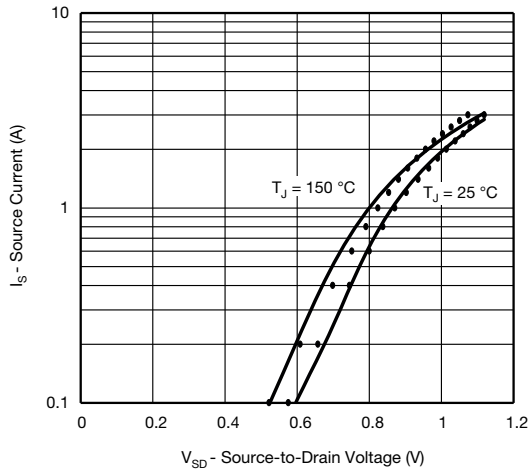












Note

- Dots and squares represent measured data