IMPROVED LINE VOLTAGE ZERO-CROSSING DETECTION TECHNIQUES FOR PV INVERTERS

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Abstract: This paper presents a comparison of two different zero-crossing detection techniques used in grid-connected photovoltaic Inverters. The current controlled Inverter should be synchronised with the supply grid to allow a steady power flow with a controlled power factor. The obvious and the most widely used method is by using a zero crossing detector. This however, is prone to errors due to various distortions found usually on the grid. A detailed grid distortion model is derived to be used for simulations. Two zero-crossing techniques based on predictive filtering and Phase-locked loops are modelled and simulated for comparison.

I Introduction

Grid-connected Inverters require synchronising its output current with the grid voltage. This is done by generating a sinusoid of the same phase and frequency as of grid voltage. This is then used as a reference to the PWM generator of the Inverter.

Currently a number of methods are in use. These methods can be categorised in to three main groups as follows:

- Noise reduction in the distorted grid signal by adaptive or Predictive digital filtering
- Use of Tracking filters (Phase Locked Loop techniques)
- Adaptive on-line Waveform reconstruction

The objective of a reliable zero-crossing detector would be to track the in-phase fundamental component of the distorted grid signal, with the required dynamic response. An obvious obstacle to this would be the noise content of the grid voltage signal. A detailed analysis was done and a model was developed to simulate grid supply distortions. This model has been used throughout to simulate different zero-crossing techniques under various types of distortions.
This paper is divided in to three main parts. A grid voltage noise model is derived, modelled and simulated in part II. Section III and IV contains a comparison of the first two techniques described above. A statistical tool to measure accuracy of zero crossing detection is designed and tested in section IV.

II Grid voltage noise model

Various non-linear loads connected to weak ac distribution systems contribute to Electromagnetic pollution of the system. This includes harmonic distortion, inter-harmonics, interference, flicker, commutation notches and dc component [1].

A test signal based on typical grid distortions (Simulink model shown in fig 1) is simulated and shown in fig 2. The signal consists of a 50 Hz sinusoid and its 3^{rd} and 5^{th} harmonic components, which are the main harmonic components encountered in the grid. The amplitudes of the 3^{rd} and 5^{th} harmonics are set at 0.2 and 0.1 respectively, while the amplitude of the fundamental is scaled to unity. The signal also contains a uniformly distributed white noise component, which depicts the high frequency noise due to the edges of the switching in switching power converters. [2]. A model to generate commutation notch type noise was developed. The model generates distortions with variable notch depth (set to 1.5 times the line voltage amplitude) and notch width. Notch width is set to 600 μs [=6.(1/10 kHz)], which is reported to be a typical value for commutation disturbances in PWM Inverters [3].

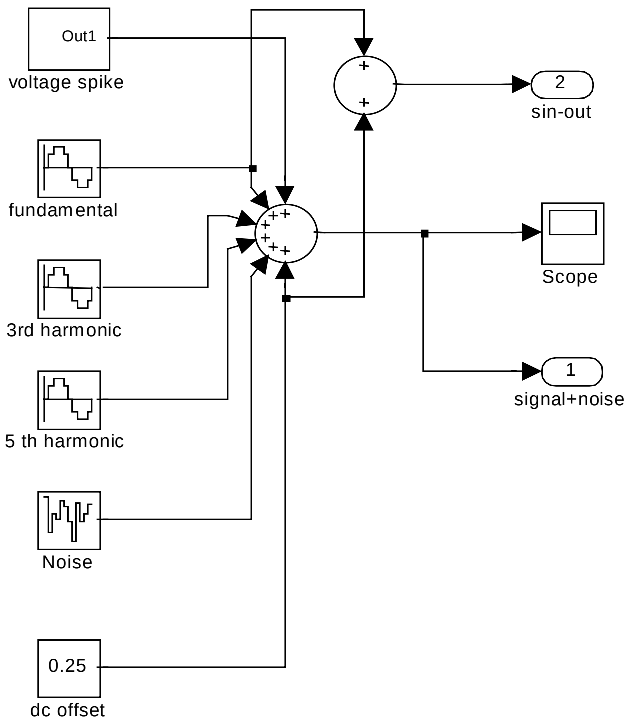


Fig 1 - Grid noise model in Simulink

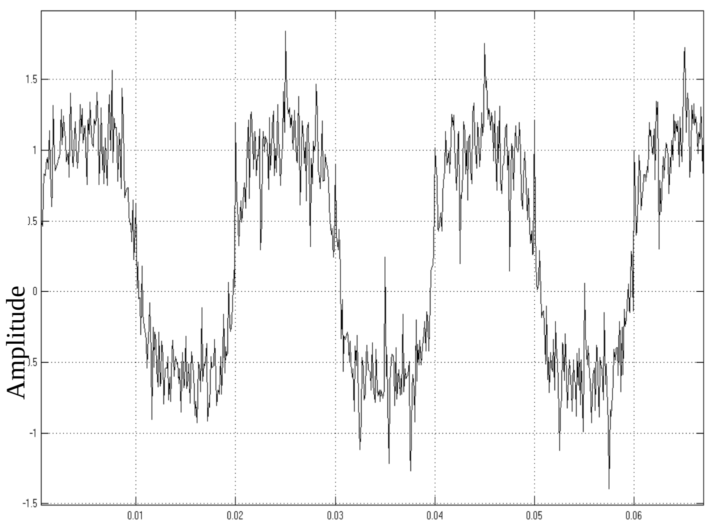


Fig 2 -Typical distorted grid voltage signal, simulated in Matlab using the grid voltage noise

III Noise reduction in the distorted grid signal - Design and simulation of a predictive digital filter

Noise types described in sec. II, causes spurious zero crossings at the output of the zero crossing detector (fig 4). This reduces the reliability of supply grid phase detection and therefore makes the task of synchronising to the grid more difficult.

The method described below is based on predictive digital filtering to minimise multiple zero crossings caused by distortions in the grid. The filtered signal is then used to calculate the true phase and the frequency of the grid signal. A sinusoidal signal synthesised using this information, will serve as a reference to the PWM generator of the Inverter. A simplified block diagram of the predictor is shown in fig 3.

The Predictor is based on a Least Mean Square (LMS) Adaptive filter, whose filter coefficients change adaptively to reduce the error (in a Least Mean Square sense) between the filter output and the desired signal [5]. The predictive nature of the algorithm guarantees zero phase shift between the grid and the filter output signal. The convergence of the error is guaranteed only if the filter input signal contains the noise component which is uncorrelated with the desired signal. This condition is achieved by delaying the noisy signal by one sample (Z^{-1}) before feeding in to the filter.

An IIR bandpass filter sampled at 100 HZ is used to suppress the dc component of the distorted signal. Phase shaping is used in designing this filter to guarantee zero phase shift at the nominal frequency.

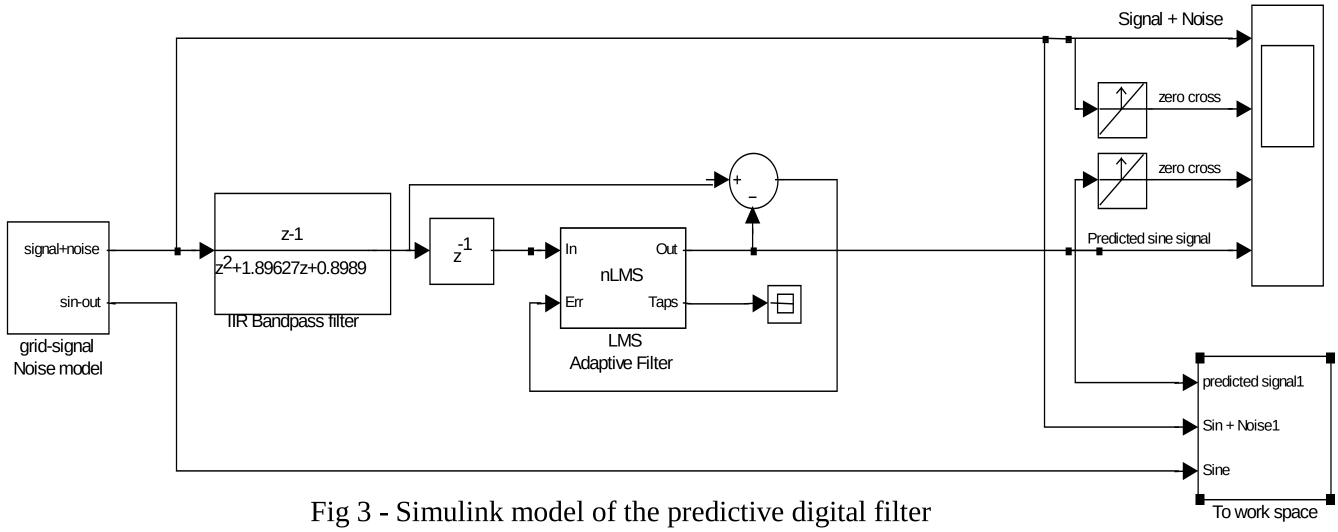
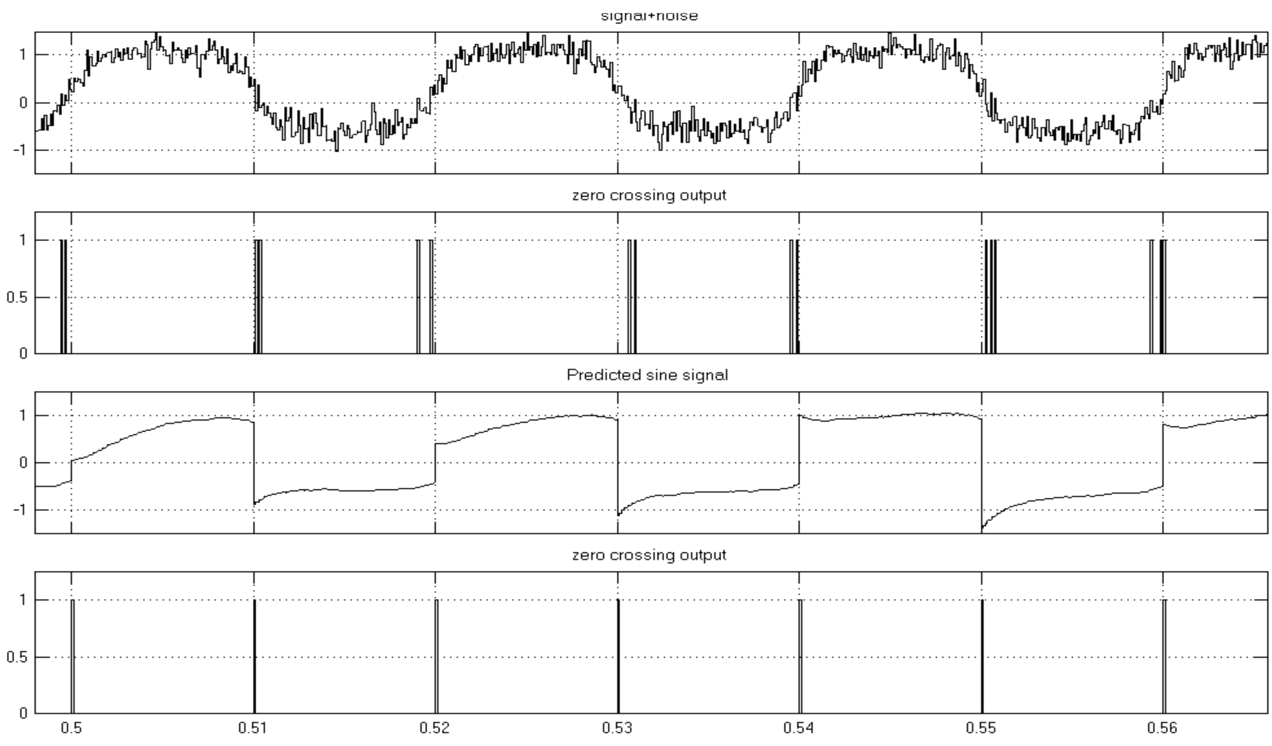


Fig 3 - Simulink model of the predictive digital filter

A - Simulation results



Time in secs

Fig 4 - Simulation results of a normalised distorted line voltage signal sample filtered through an adaptive predictor

A clear improvement in zero crossing detection is evident from the simulation results shown in fig 4. However the use of different sampling rates for the IIR pre-filter and the LMS adaptive filter adds to Implementation problems on a DSP environment. Another disadvantage of this filter is its inability to attenuate commutation notches type disturbances. A Median type filter used in cascade is proposed in [1], for notch suppression.

IV - Tracking filters - Phase Locked Loops

Another approach of improving zero crossing detection reliability is the use of tracking filters. Tracking filters are basically, Phased Lock Loops (PLL), designed to track the 50 (+/- 2%) Hz grid voltage with required dynamic response. A survey of theoretical and experimental work done on digital phase locked loops (DPLL) was published by Lindsay *et al.* [4].

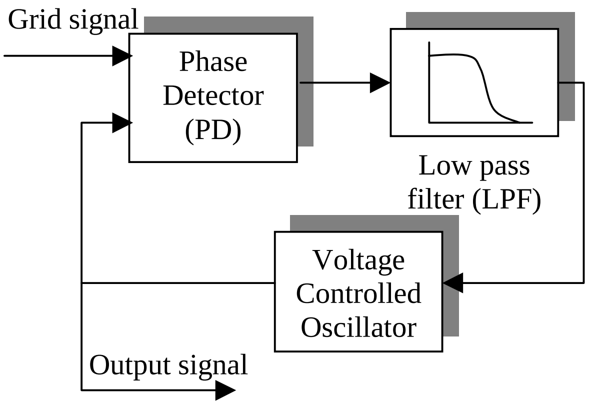


Fig 5 - Simplified block diagram of a PLL

The relative difference in phase is detected by the PD and filtered through LPF to be fed in to theVCO. The output of the VCO is a signal whose frequency is locked to the grid signal.
Robustness of the PLL is guranteed when the dynamic performance of the closed loop system satisfies, both fast tacking and good filtering (low pass) characteristics.However, both requirement cannot be satisfied simultaneously, as they contradict each other. Hence a trade off is found to optimise the filter's performance.
Lock in Range ($\Delta\omega_{L,}$ given in (1)) is the the range of frequencies where the PLL could lock in with minimum time [6].

$$\Delta\omega_L \approx 2*\xi*\omega_N \qquad (1)$$

where, ξ and ω_N are damping factor and natural frequency of resonance, of the system.

As seen from (1), a higher locking range requires a higher bandwith (assuming ξ to be constant), which in contrary leaves the system vulnerable to high frequency noise. Since the closed loop system could be modeled as a 2nd order system of the type :

$$H(s) = \frac{\omega^2{}_n}{S^2 + 2.\zeta.\omega_n.S + \omega^2{}_n} \qquad (2)$$

An optimum value for ξ (= 0.707) is found using the Weiner optimisation criteria [1].
This guarantees the delicate trade-off between fast tracking and noise immunity of the PLL.

Another approach to this is to implement the PLL with variable loop bandwidth (B_L).
In this method loop bandwidth will be a function of the Lock In state of the PLL. In pre-lock state B_L will increased (by varying values of the low pass filter) to accommodate quick Lock In. After locking in to the signal B_L will be restored to its default, which will ensure noise imminuty of the system.

B - Simulation results

Design and simulation of a PLL has been done on Matlab / Simulink platform and results are shown in fig 7 and fig 8.

The model synthesises a sinusoid, tracking the phase and the frequency of a distorted grid. This can then be directly used as a reference for the Inverter PWM generator.

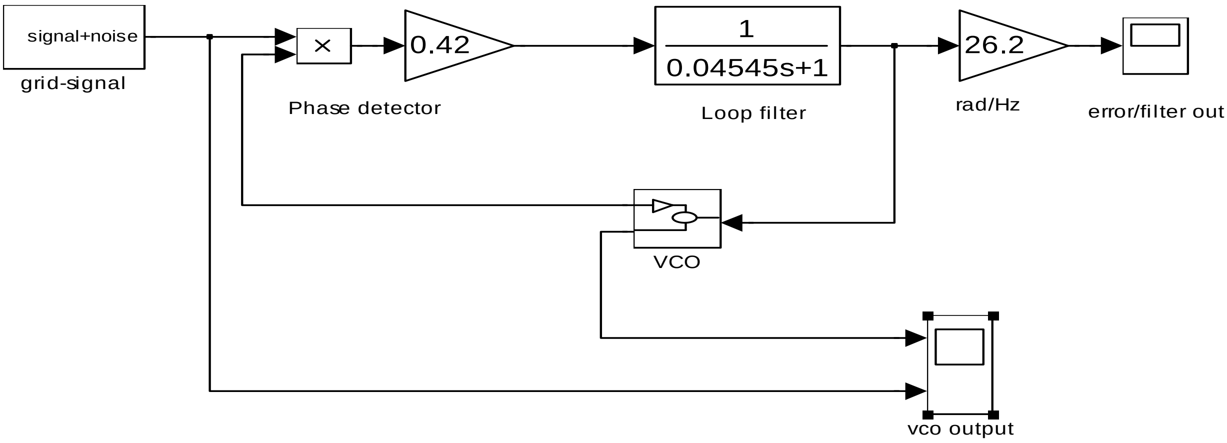
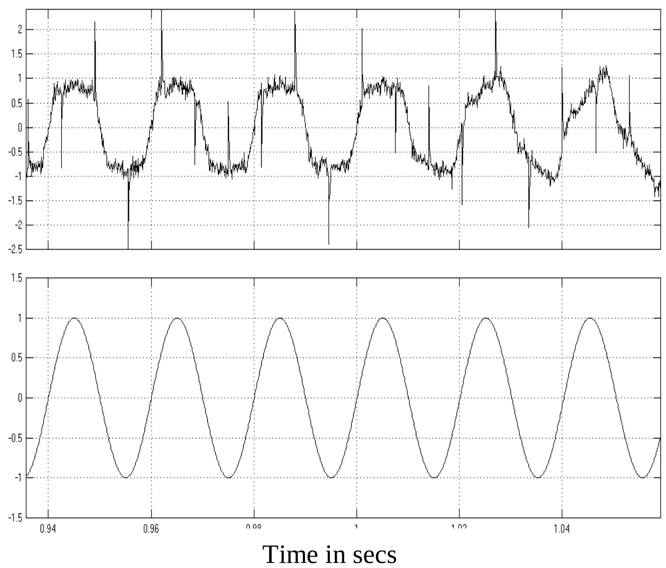


Fig 6 - Simulink model of a second order PLL



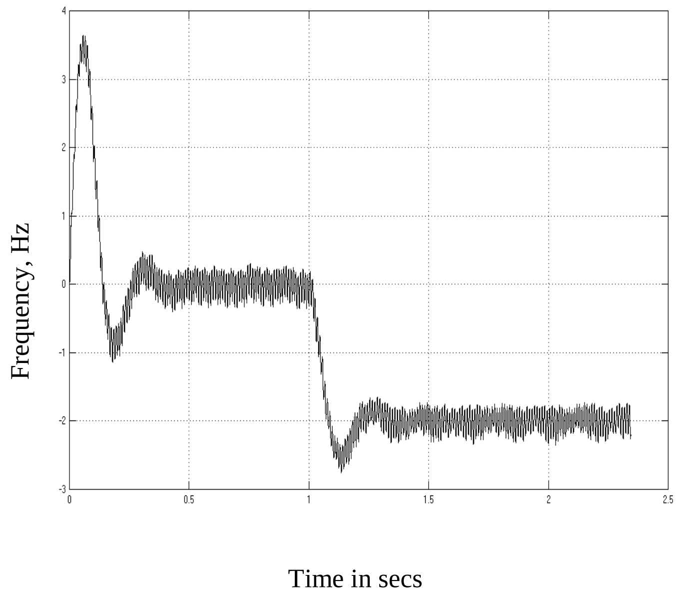


Fig 7 - Simulation results
A - Input signal (50 Hz → 48 Hz) at t = 1sec
B - PLL output waveform

Fig 8- Closed loop transient response of the PLL for a 2 Hz step change at t = 1 sec

V - Measuring the accuracy of zero-crossing detection

The need for an efficient tool to measure the accuracy of zero crossing detection has risen when comparing relative merits of different techniques. The method proposed in this paper, calculates misplacements of zero- crossings of a given distorted signal, relative to an ideal signal of the same frequency and phase. The misplacement is measured in samples and put in to bins to give a histogram output of the results.

The algorithm is realised in Matlab m-code. Fig 9 shows the results of the program run through signal data obtained through simulation results of sec. II (fig 4).

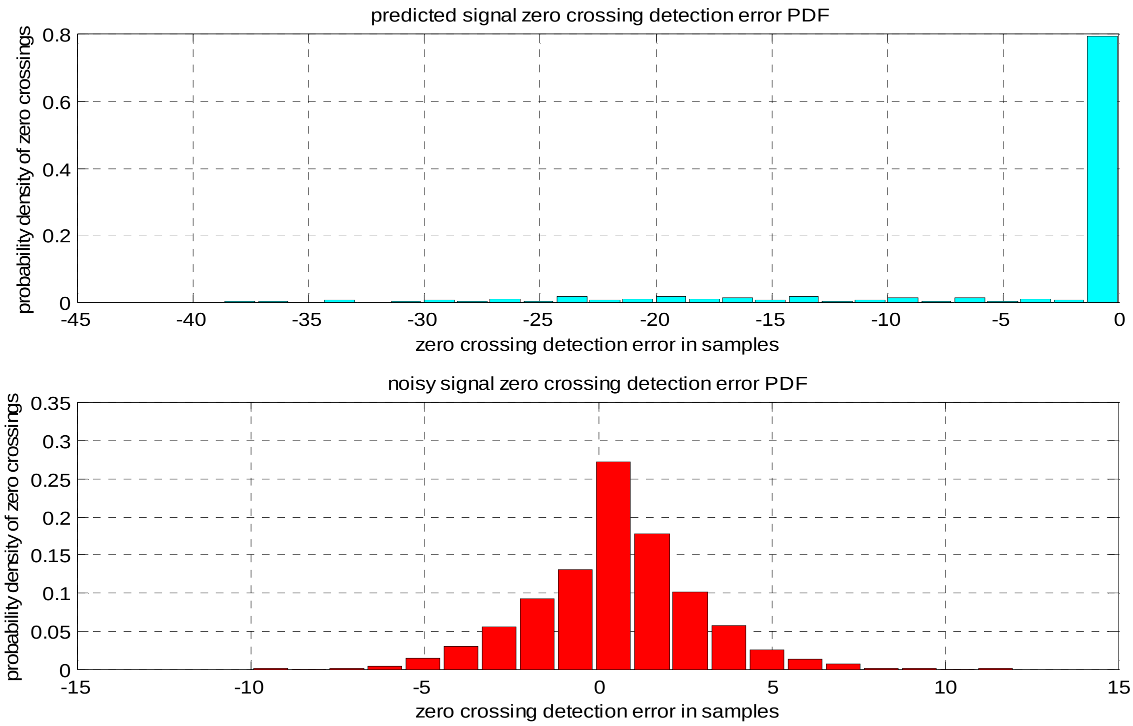


Fig 9 - Probability density functions of zero crossing detection error

VI - Conclusions

Models have been derived and simulated for two different zero-crossing detection techniques. The noise reduction approach based on Least Mean Square adaptive filtering requires different sampling rates. Further, an additional block is needed to calculate the frequency and the phase from the filter output. Hence the DSP implementation of this will be computationally intensive. On the contrary, the phase-locked loop approach has proved to be both simple and straightforward to implement.
Further work is continuing in this direction to implement the Adaptive PLL algorithm in C Language. This code can then be downloaded to the TMS320C31 DSP for real-time zero-crossing detection. A noise generator, based on the model described in sec.II, will be will be developed combining the DSP and a power amplifier.

References

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