Video Electronics Standards Association

E-DDC™ Standard

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ENHANCED DISPLAY DATA CHANNEL STANDARD

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Purpose

The purpose of this standard is to define a communications channel between an electronic display (e.g. CRT, LCD, etc. displays) and a host system. The channel may be used to carry configuration information to enable 'plug & play' and allow optimum use of the display. The channel may also carry display control information.

Summary

Today's computing and consumer electronic environments demands that systems offer user-friendly set-up. With the growing popularity of intuitive and simpler software user interfaces, hardware manufacturers are responding with plug-and-play systems and peripherals. However, for the user to receive full benefit from these advances, standardization is necessary. VESA, as the prominent standards organization for graphics subsystems, has developed a communications channel between the host and the display. This communication channel offers basic configuration information plus a standard way of communicating advanced functionality.

Caution:
The current requirement for +5 volt DDC is likely to be replaced in a future revision with a +3.3 volt requirement. In the current transition phase, it is recommended that new monitor designs work with a 3.3 volt supply and are tolerant of a +5 volt supply for backward compatibility.

Preface

Scope

This revision of the DDC Standard is intended to eliminate sections that support standards that have not been adopted by the industry. This will simplify the document while maintaining compatibility with previous revisions of this standard for displays and systems.

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates DDC, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

- Fax 408-957-9277, *direct this note to Technical Support at VESA*
- e-mail support@vesa.org
- mail to Technical Support
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Revision History

Version 1 September 2, 1999

Initial release of the standard. The body of the standard is derived from the VESA DDC version 3 standard. The major changes were the addition of the E-DDC protocols, removal of DDC1 protocol and clarification to the DDC power requirements.

Version 1 Revision 1 March 24, 2004

This revision is primarily to update the E-DDC standard and not to introduce major changes. The scope has been expanded to encompass usage in consumer electronic products and video interfaces other than VGA with text clarified in several places.

Support for the P&D and FPDI-2 standards has been eliminated along with recommendation that new designs do not support DDC1.

Warning about the possible future change of the "DDC +5V" to a 3.3 volt supply has been added.

Pins 4 and 11 of the VGA connector have been changed from "optional" to "reserved - no connection" designation.

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1. OVERVIEW

1.1 Summary

The Enhanced Display Data Channel (E-DDC) described in this document, allows the display to inform the host about its identity and capabilities using an I^2C bus. It is enhanced from DDC by enabling the communication channel to address a larger set of data. The communication channel, as used for this purpose, is uni-directional from display to host using the E-DDC operational modes except for the command to initiate an EDID data transfer which the host device sends to the display. The contents and formats of data are described in the VESA Enhanced Extended Display Identification Data Standard (E-EDID) and a number of E-EDID extension block standards.

The scope of this document is detailed description of the operational modes of DDC and their implementation.

However, in addition to serving to request and transmit EDID data, DDC also allows communication that is truly bi-directional between the display and host. This enables control of display functions affecting the displayed images and possibly use of other devices attached to the I^2C bus. The bi-directional communication modes are described outside of this standard in the VESA Display Data Channel Command Interface Standard (DDC/CI) and the associated VESA Monitor Command and Control Set (MCCS) standard.

DDC communications has been widely implemented in a number of video interfaces including VGA (15 pin high-density D-sub), DVI (Digital Visual Interface), HDMI (High Definition Multimedia Interface).

This document does not specify how the E-DDC interfaces to the host CPU address and I/O spaces.

Earlier versions of DDC and E-DDC standards introduced and supported the DDC1 operational mode. With this revision, VESA ceases to support DDC1 for new designs (host and display), it is expected that all new designs will support a minimum of DDC2B.

1.2 Background

Early personal computer monitor identification schemes were only capable of handling a limited number of display types and parameters. Since these schemes carried very little information about the capabilities of the display, they were of limited value.

Earlier versions of DDC and EDID defined a communication method and configuration data appropriate for traditional CRT displays, but were limited in support of other display types and the amount of data that could be supported in the display. As new display technologies have been introduced to the market, support for communication methods and configuration information suitable for these displays has become a necessity In recent years displays intended for digital and high definition television have also started to use the DDC protocols.

1.3 Standard Objectives

The E-DDC standard was developed by VESA to meet, exceed and/or complement certain criteria. These criteria are set forth as Standard Objectives as follows:

- Support Microsoft® Plug and Play definition
- Provide information to allow the graphics subsystem to be configured based on the capabilities of the attached display
- Ensure scaleable, low cost, fast market acceptance

- Allow for base level to be achieved with minimal hardware cost penalties in host controller and display
- Retain compatibility with most existing graphic controller chips at minimum configuration level
- Define a full communication channel capable of sending E-EDID as well as allowing control of display parameters from the host.
- Remain compatible with and continue to support DDC2B protocols for existing monitors.

1.4 Significant Changes in Current E-DDC Revision

This version (1.1) updates the E-DDC standard but does not introduce any major changes. Changes may be summarized as:

- Deletion of references to P&D and FPDI-2 standards
- DDC1 support is strongly discouraged for new designs
- Support for E-EDID extensions explicitly added
- Pins 4 and 11 of the VGA connector are redefined as “reserved – do not use”. Previously undefined.
- Recognition that E-DDC is supported on multiple interfaces

1.5 Reference Documents

Versions identified here are current but users of this standard are advised to ensure they have the latest versions of reference standards and documents.

Source	**Name**	**Version / Date**
VESA	Video BIOS extensions for Display Data Channel (VBE/DDC)	1.1 / Nov. 1999
	Enhanced Extended Display identification Data (E-EDID)	A.1 / Feb. 2000
	Monitor Command and Control Set (MCCS)	2 / Oct. 2003
	Display Data Channel – Command Interface (DDC/CI)	1 / Aug. 1998
	Plug and Play	Proposed standard
Philips	The I^2C Bus Specification	2.1 / Jan. 2001
Microsoft	Windows and the Plug and Play Framework Architecture	March 1994
	Plug and Play for Windows 2000 and Windows XP	December 2001
	Windows XP – Plug and Play Overview	
	Plug and Play Technology	December 2001
IBM	IBM Personal System/2 Hardware Interface Technical Reference-Common Interfaces Video Subsystem	1987

Table 1.4: Reference Documents

1.6 Compatibility with Non-DDC System Units / Graphic Cards

Old computer graphics subsystems and boards which use the ID bits to identify the attached monitor type may have a problem with a DDC monitor since ID bits 1 has been redefined and may be read as either a '1' or '0' dependent on when it is read.

Use of one of the following options should be considered to avoid this problem:

- Avoid compatibility claims for these systems and boards
- Clearly label monitor as suitable for DDC capable graphics subsystems and boards only
- Provide or recommend a pass-through connector which isolates the monitor DDC lines from the graphics subsystem or board
- Implement a switch (hardware or software) to allow user to disable the monitor DDC function

Note: This is likely to be a problem only with graphic sub-systems designed before the mid-90s.

2. DEFINITIONS

In the following sections there are references such as “EDID 1.x”, this refers to EDID data structure version 1, revision x. Increments of the revision number indicate backward compatibility with earlier revisions, and increments of the version number indicate some degree of incompatibility with earlier versions - see the latest VESA E-EDID standard for details.

2.1 Data formats

2.1.1 Enhanced Extended Display Identification Data: E-EDID

Data structure containing the display identity and the basic display specifications. E-EDID defines a 128-byte structure and extensions to the structure in 128-byte increments. E-EDID is fully compatible with EDID version 1 data structure. Details can be found in the VESA E-EDID standard.

2.1.2 Enhanced Extended Display Identification Data Extension Blocks

A number of VESA standards have been approved which define EDID Extension Blocks – reference document list. Note, new Extension Block standards will likely be developed periodically, check the VESA website for the latest standards.

The CEA has also developed a Timing Extension Block for use with digital television products compliant with the EIA - 861b specification.

2.2 Communication Protocols

The original DDC standard supported two modes, a very simple mode called DDC1 and a I^2C bus (see Philips I^2C specification) based mode called DDC2. There are a number of DDC2 protocols with different features and capabilities … DDC2B provides the base level of bi-directional communications, E-DDC provides the same set of functions as DDC2B but with a larger accessible memory space and DDC/CI extends the range and type of communications available.

2.2.1 DDC1 (for reference only … *not recommended for new designs*)

A protocol which utilizes a uni-directional data channel from the display to the host to carry continuous transmission of the EDID information.
Note: DDC1 cannot be used to support E-DDC displays

2.2.2 I^2C Bus

A standard protocol two-wire (clock and data) serial data bus. Note that all devices on an I^2C bus are allocated fixed addresses by Philips. In the case of displays, addresses are A0h and A1h. See I^2C specification for details.

2.2.3 Display Data Channel – Bi-directional (DDC2B)

A protocol based on I^2C and used on a bi-directional data channel between the display and host. In DDC2B mode the only transmission from the host to the monitor is a request for EDID data. This request is implemented by accessing the device at the I^2C address of A0h / A1h

2.2.4 Enhanced DDC (E-DDC)

A protocol based on I^2C and used on a bi-directional data channel between the display and host. This protocol accesses devices at I^2C address of A0h / A1h as well as the address 60h. The 60h address is used as a segment register to allow larger amounts of data to be retrieved than is possible using DDC2B protocols. The protocol is compatible with DDC2B protocols.

2.2.5 DDC Command Interface (DDC/CI)

A set of protocols based on I^2C and used on a bi-directional data channel between display and host. The protocols provide a mechanism to send commands to the display; data may also be sent/received to/from the display. Details can be found in the VESA DDC/CI Standard. Compatible with DDC2B and E-DDC.

2.3 DDC addressing

DDC accesses data from the display by using I^2C protocols to access particular device addresses.

2.3.1 DDC address (A0h / A1h)

The base DDC address pair of A0h / A1h is used to access EDID data structure 1.x. The address pair allows access of up to 256 bytes of data, which enables reading of two EDID 1.x data blocks. Larger data sizes cannot be accessed using the base DDC address alone.

2.3.2 Segment pointer (60h)

Enhanced DDC allows access of up to 32 Kbytes of data. This is accomplished using a combination of the A0h / A1h address pair and a segment pointer. For each value of the segment pointer 256 bytes of data are available at the A0h / A1h address pair. An unspecified segment pointer references the same data as when the segment pointer is 0. Each successive value of the segment pointer allows access to the next two blocks of EDID (128 bytes in each block). This is illustrated in Figure 2.1. The value of the segment pointer register cannot be read since it is reset at the completion of each command.

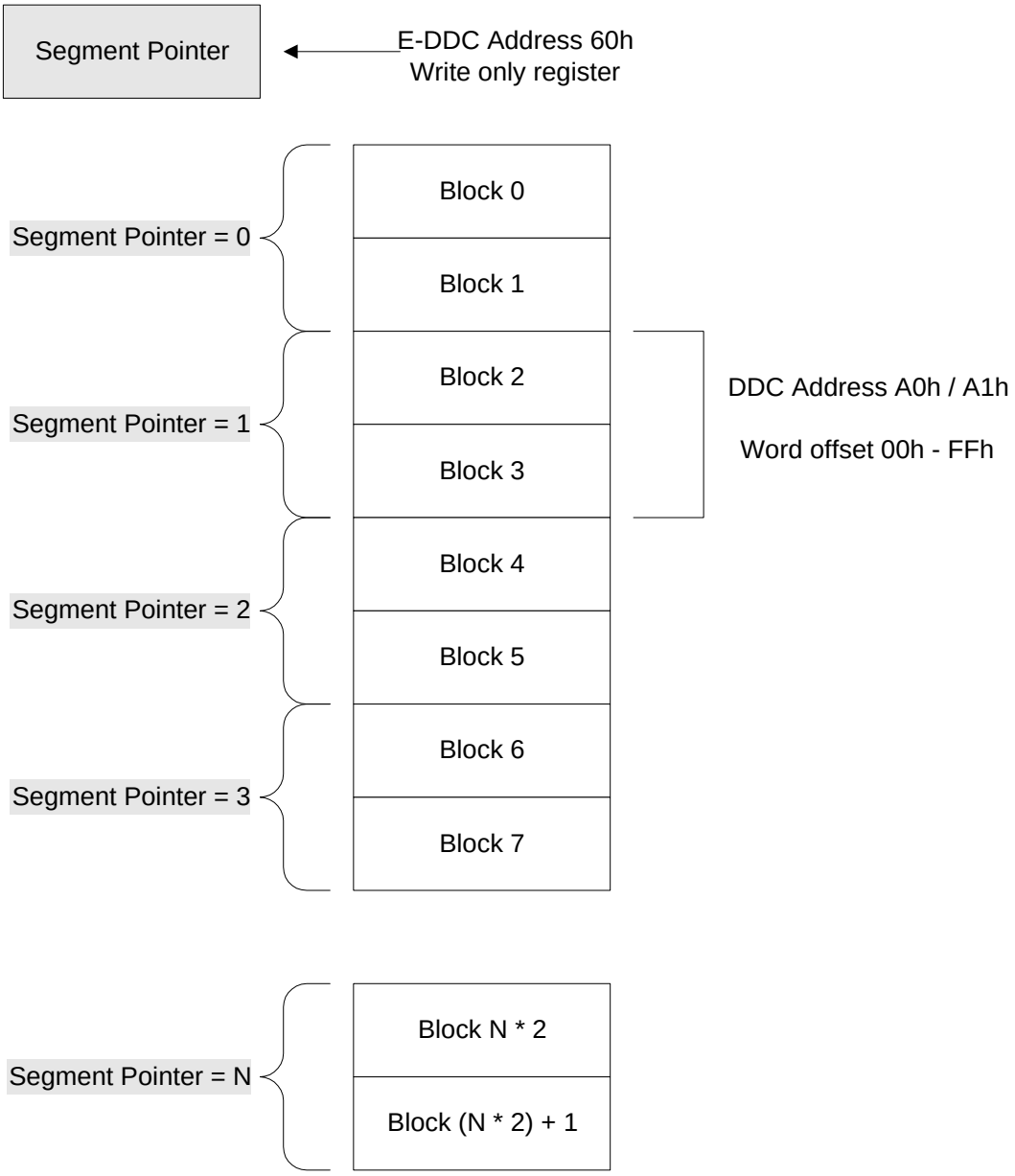

Figure 2.1 - E-DDC Segment Pointer and Block Layout

2.4 Display Types

2.4.1 Non-DDC Display

- Display with no DDC capabilities

2.4.2 DDC Display

- DDC2B capable
- Display containing EDID 1.x data (128 bytes) plus an optional EDID Extension block (128 bytes) at DDC address A0h / A1h
- Older displays may support DDC1 … *not recommended for new designs.*

2.4.3 Enhanced DDC Display

- Enhanced DDC read compliant
- Display with EDID 1.3 (or higher) data and up to 255 extension blocks, each 128 bytes (up to 32K bytes total EDID memory).
  Note that a single extension may occupy multiple 128 byte blocks.

2.5 Host System Types

2.5.1 Non-DDC Host

- Host without DDC capabilities

2.5.2 DDC1 Host

- Host using DDC1 protocols to read EDID 1.x. It is recognized that some DDC1 host and graphics cards may still be in use but DDC1 is not recommended for new designs.

2.5.3 DDC2B Host

- Host using DDC2B protocols
- Reads EDID 1.x plus an optional EDID Extension block (128 bytes) at DDC address A0h / A1h

2.5.4 Enhanced DDC Host

- Host using E-DDC protocols
- Reads EDID 1.x at DDC address 60h / A0h / A1h
- Reads Enhanced EDID extensions at DDC address 60h / A0h / A1h

2.6 DDC System/Display Matrix

The matrix in Table 2.1 shows interoperability of DDC operations between monitors and systems of different types. For each case where interoperability is possible, the matrix shows the EDID block size, the DDC mode used and the DDC address where the data is found.

	Non DDC Display	**DDC Display**	**Enhanced DDC Display**
Non-DDC Host	No DDC function	No DDC function	No DDC function
DDC2B Host	No DDC function	EDID 1.x and an optional EDID extension at DDC Addresses A0h / A1h	EDID 1.3 (or higher) and an optional EDID extension in Segment 0 at DDC Addresses A0h / A1h
Enhanced DDC Host	No DDC function	EDID 1.x and an optional EDID extension at DDC Addresses A0h / A1h	EDID 1.3 (or higher) and any EDID extensions at E-DDC Addresses 60h / A0h / A1h.
Legacy Mode			
DDC1 Host	No DDC function	EDID 1.x using DDC1 protocol	No DDC function

Table 2.1 - DDC System/Display Matrix

3. Enhanced DDC System / Display Combinations

This section addresses issues most likely to arise in computer/display systems. Figure 3.1 through Figure 3.5 illustrate typical communication sequences.

3.1 Interoperability

There are two scenarios that can occur where the display and host system support different versions of EDID standards. This potentially raises issues of compatibility and interoperability between standards (existing and proposed). These are discussed in the following sections.

3.1.1 DDC2B Host System Connected to an E-EDID Display

The first scenario of potential concern is that of an existing, DDC2B / EDID 1.x compliant, system connected to a monitor that supports the E-EDID standard. This situation is addressed by the full backward compatibility of the E-EDID standard. A unique situation can potentially occur where an EDID 1.x graphics controller can utilize a software driver to utilize the extended features of the proposed new standard. In this situation it is possible that a system reset can be initiated while the software driver is performing an extended EDID operation, in which the segment pointer has been set to point to a segment other than segment 0. If the extended EDID operation has not been completed when the system resets, then the segment pointer will not be reset and the graphics controller BIOS would then be unable to recognize the monitor. In order to address this issue, this standard requires that the segment pointer be reset to 00h when a NO ACK or a STOP condition is received.

3.1.2 Enhanced DDC Host System Connected to a Legacy DDC Display

The second scenario is one in which the graphics controller supports the Enhanced EDID standard, and the monitor is EDID 1.x compliant only. In this case, the system issues the START condition and the DDC Address byte for the E-EDID command (60h) but the display memory device will not respond to this address - in effect issue a NO ACK. Since a NO ACK is a valid response, the host will continue by writing the segment pointer. (Since the attached display is a legacy DDC display the host can't assume that there are any other segments than segment 0, hence the segment pointer must be segment 0 in order to read EDID 1.x.) The display will once again not respond, in effect issue a NO ACK. Also here, the NO ACK is a valid response and the host will continue with the read process. The rest of the process is identical to the legacy DDC2B EDID 1.x read operation and the display will respond with its EDID data.

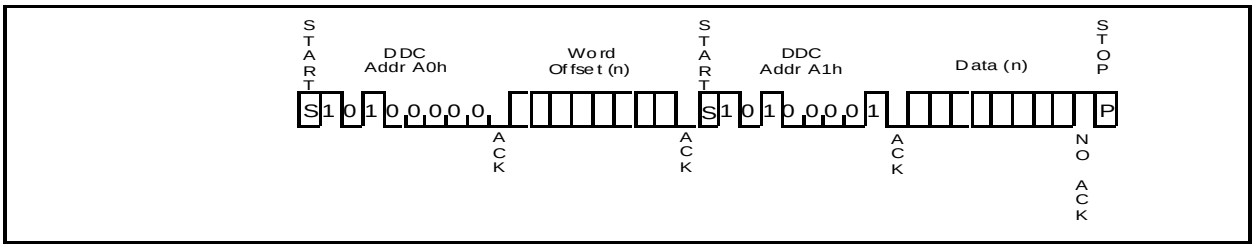

Figure 3.1 - DDC2B Random Address Read (Segment 0 only)
(For reference only)

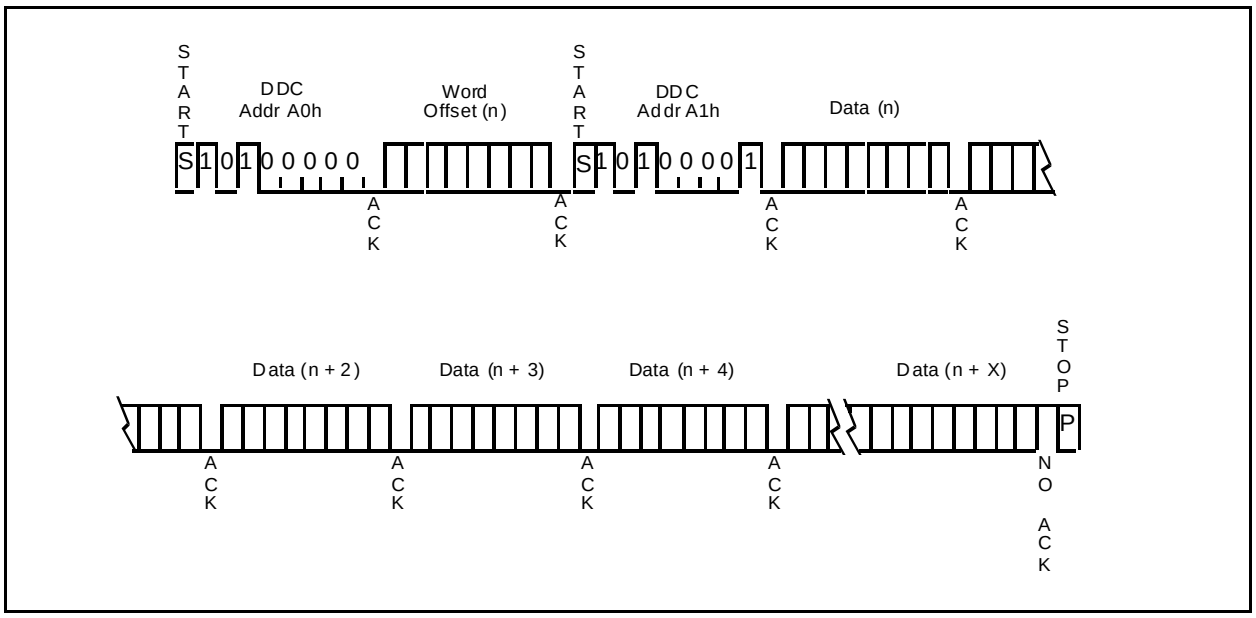

Figure 3.2 - DDC2B Sequential Read (Segment 0 only)
(For reference only)

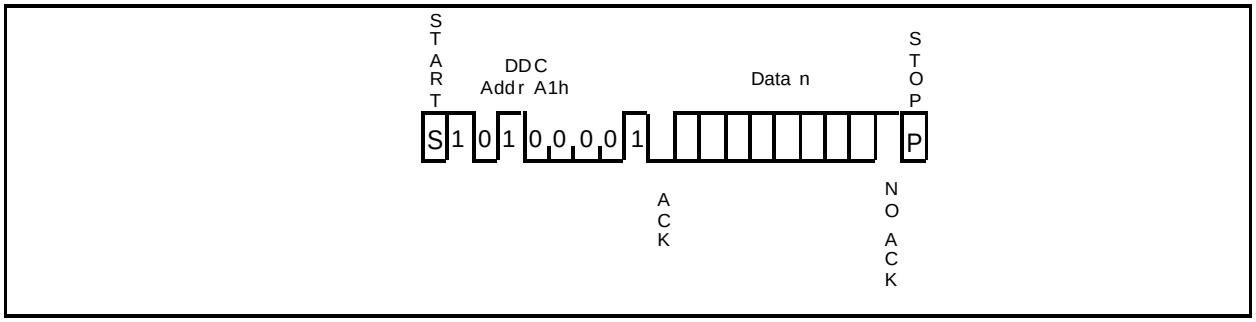

Figure 3.3 - DDC2B Current Address Read (Segment 0 only)
(For reference only)

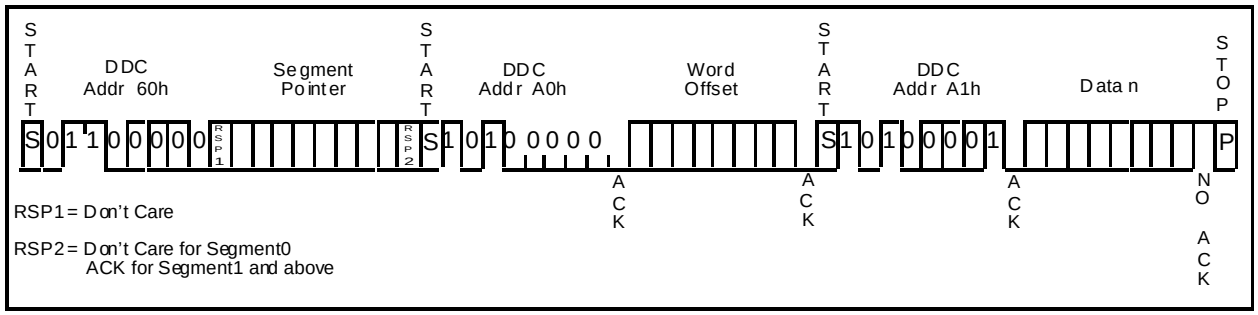

Figure 3.4 - Enhanced DDC Read

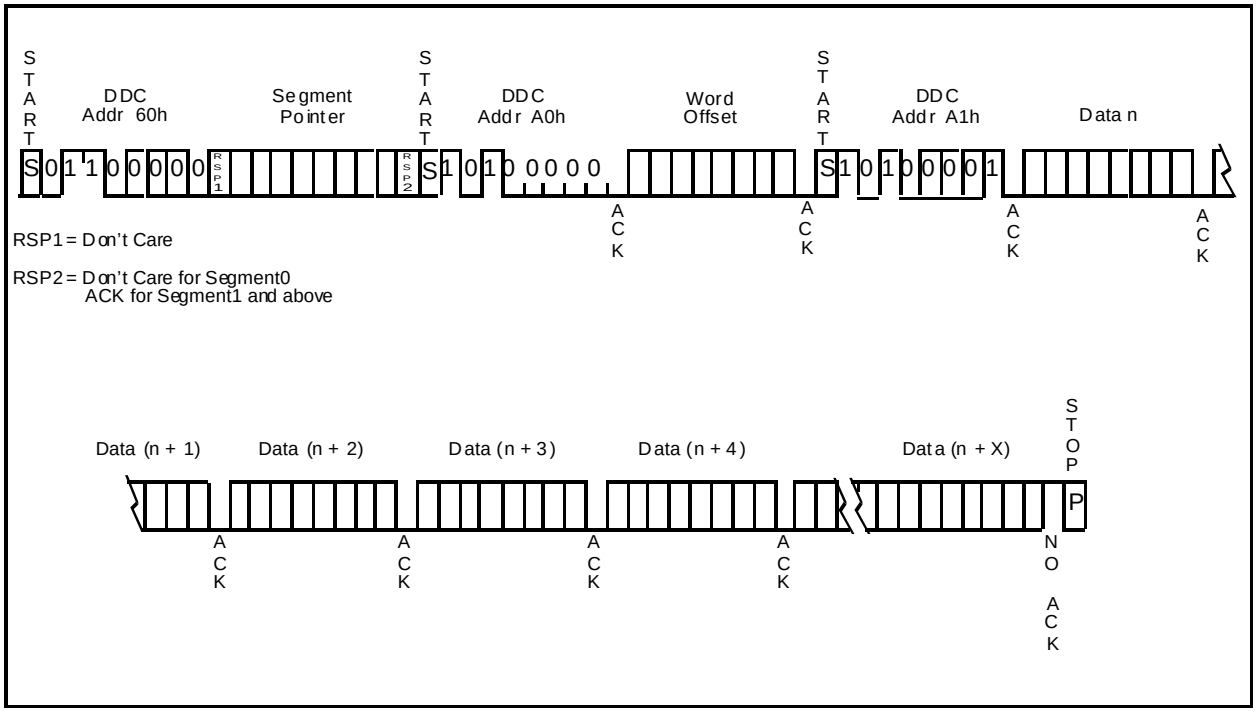

Figure 3.5 - Enhanced DDC Sequential Read

4. Physical Connections

DDC2B, E-DDC and DDC/CI can be implemented on any video interface supporting the E-DDC standard. Examples include the 15 pin VGA (Video Graphics Array), DVI (Digital Visual Interface) and HDMI (High Definition Multimedia Interface). Details of the VGA interface are included here but the appropriate specification should be consulted for details of other video interfaces.

4.1 Display ⇔ Host Graphics Controller

4.1.1 Purpose

To provide a standard mechanical and electrical interface between the display and host graphics controller through which DDC communications can pass. This standard specifies the interface through the standard 15-pin VGA connector. Other interface standards implement DDC on alternate connector types and pin allocations, check the appropriate specification for details.

4.1.2 Mechanical - VGA Connector

The mechanical specification for DDC is backward compatible with the standard 15-position VGA-type connector with the following exceptions.

- Socket # 9 shall be recessed by 0.050 inches for DDC compliance. Socket to retain contact capability.
- The host side connector color, plastic part, shall be “royal blue” to clearly indicate that socket is DDC compatible

Suitable connectors are available from a number of sources; the following are listed for reference. This does not imply that VESA recommends or approves these particular connectors:

- AMP p/n 787066-1 787066-2 787506-1
- Molex p/n 89263-*7** 89141-70** 89046-70**

4.1.2.1 Connector Pinouts

Pin #	Legacy VGA	DDC2B Host	E-DDC Display
1	Red video	Red video	Red video
2	Green video	Green video	Green video
3	Blue video	Blue video	Blue video
4	Monitor ID bit 2	Monitor ID bit	Reserved - No connection
5	Test (ground)	Return (ground)	Return
6	Red video return	Red video return	Red video return
7	Green video return	Green video return	Green video return
8	Blue video return	Blue video return	Blue video return
9	No connection (mechanical key)	DDC +5 volt supply (mandatory supply)	DDC +5 volt load (See section 4.5)
10	Sync. return	Sync. return	Sync. return
11	Monitor ID bit 0	Monitor ID bit 0	Reserved - No connection
12	Monitor ID bit 1	Bi-directional data (SDA)	Bi-directional data (SDA)
13	Horizontal sync.	Horizontal sync.	Horizontal sync.
14	Vertical sync.	Vertical sync.	Vertical sync.
15	Monitor ID bit 3	Data clock (SCL)	Data clock (SCL)

Table 4.1 - 15-pin D-type Connector Pinouts

4.1.3 Mechanical – Other connectors

DDC signals assignments on other connectors are defined in the respective documents.

4.1.4 Electrical

4.1.4.1 General

Graphics controller boards should provide pull-up resistors of ≥ 1.5 KΩ and ≤ 2.2 KΩ to a +5 volt reference or a 3 mA current source for the SCL and SDA open drain signals.

All SDA and SCL pull up resistors should be located within the host system except for the 47 KΩ pull up resistor on the SCL line.

4.1.5 Timing

4.1.5.1 DDC2 Timing

Data is synchronized with the clock signal and timing shall comply with the I^2C specification. Refer to I^2C specification for details.

4.2 Host DDC +5 Volt Source

The system unit or graphics card shall supply +5 volts (+/- 5%) whenever the video port is active. The required current capability is 50mA with over current protection limited the maximum current to no more than 1A.

4.3 Display DDC +5 Volt Load

When the display is not AC powered and / or the power switch is in the off position it may draw up to

50mA from the +5 volt supplied by the host.
When the display is AC powered and the power switch is the on position it shall not draw more than 1mA from the +5 volts supplied by the host.

4.4 Display DDC Signal Availability

The display should be capable of providing EDID information over the DDC channel whenever the DDC 5v signal is provided. EDID information should be available within 20ms after the 5v signal is provided.

4.5 Future of +5 Volts Supplied by the Host

As noted in section 4.2 there is currently a requirement for the host device to supply 5 volts ± 5% to the display to ensure that the EDID data can be read even if the display is switched off. It is anticipated that this requirement will change to 3.3 volts in a future revision of this standard.
In order to ensure an orderly migration with maximum interoperability it is recommended that new display designs operate using a 3.3 volts AND are tolerant of a 5 volt supply from the host.

5. Data Transfer Protocols

*5.1 DDC1 (***for reference only –** ***not recommended for new designs)***

A uni-directional channel from display to host. The 128-byte EDID is continuously transferred from the display to the host on the serial data line (SDA), clocked by Vsync.

5.2 DDC2B and Enhanced DDC

DDC2B is an uni-directional channel from display to host. The host computer uses base level I^2C commands to read information from a display with a slave address of A0h / A1h

Enhanced DDC uses the same command structure with one modification. A segment pointer is used to allow addressing outside of the normal 256-byte limit of the A0h address. The Enhanced DDC protocol sets the segment pointer before the remainder of the DDC command.

Display type	EDID base address	Data size	EDID extension address	Data size
DDC	A0h Device 00h word offset	128 bytes	A0h device 80h word offset	128 bytes
E-DDC	00h segment pointer A0h Device 00h word offset	128 bytes	Segment pointer 00h -7Fh A0h device 00h or 80h word offset	128 bytes

Table 5.1 - DDC2B device addresses

5.2.1 Basic operation for Enhanced DDC access:

Read EDID

SET Segment 0, device A0h, start address 00h, READ 128 bytes
IF no valid response
THEN display is not DDC capable
IF Extension flag is not equal to zero
THEN Optional Extended EDID extension blocks of 128 bytes each can be read at subsequent segments and start addresses

e.g. A single optional EDID block can be read with the command:
Segment 0, device A0h, start address 80h, read 128 bytes

6. Compliance with this Standard

Compliance with the VESA E-DDC Standard requires that all requirements of Sections 1 to 5 inclusive, for whichever level of the DDC Standard is being implemented, are met.

6.1 Older Designs

Older DDC displays and graphics subsystem designs will generally comply with the DDC Standard Versions 1, 2 or 3 only and not support the new features added in the E-DDC Standard.
Designs based on the DDC1 protocol are not compliant with the E-DDC standard, DDC1 is not recommended for any new design.

6.2 New Display Designs

It is recommended that new DDC monitor designs comply with E-DDC Standard Version 1.1. Displays are not required to implement the segment pointer if all data can be accessed in segment 0.

6.3 New Host Subsystem Designs

It is recommended that new DDC host designs comply with E-DDC Standard Version 1.1. Designs compliant with DDC Standard Version 3 or earlier may be unable to access complete data in an E-DDC display.

7. Appendix A - Answers to Commonly Asked Questions

	Question	Answer
1	Why is +5 volts on pin 9 of the VGA connector mandatory for hosts and/or graphic cards?	Ref.: Section 4.2 It has become common for system management software to interrogate peripheral devices for product type and serial number as a form of asset management. This is usually scheduled for nighttime but if the monitor is powered off then no data can be collected. Providing +5 volts allows the DDC circuit in the monitor to remain active even when the monitor itself is powered off. It also allows for EDID to be available to the host even if the user has not switched on the monitor yet i.e. it enables display plug and play
2	Is +5 volts mandatory for portable computers?	Ref.: Section 4.2 Portable computers that want to be able to claim compliance with VESA DDC standard version 2 (and later) must provide the +5 volt output.
3	Is +5V from the host required to be continuously active?	Ref.: Section 4.2. +5V should be provided whenever the host video port is active, or when the host is attempting to read the monitor's EDID data. In particular, hosts running on battery power may disable the +5V output when the host video port is not active, to conserve battery power.
4	What are the intended uses for the +5V output?	Ref.: Sections 4.2& 4.4. +5V is needed as a power source for the DDC and EDID circuits of a display monitor when the host is attempting to read the monitor's EDID data and the display's own local power supply is not yet turned on. This capability is especially important when a host is initially booting up or when a mobile host user enables the external video port, so that the host can properly detect the type of display attached. This is the main use of +5V defined in the Enhanced DDC Standard. (The EDID and DDC circuits in a display should always be powered from the display's own local power supply whenever it is available.) The E-DDC Standard does not directly define or constrain other possible uses for the +5V output, provided that the specified load limits are not exceeded. For example, when the display is powered on, +5V may be used as a logic signal to control display power states, i.e., signaling to the display whether or not the host video port is active, so that the display can decide when to go into a reduced power mode. This is the reason why the +5V must be provided continuously whenever the host video port is active. Since the host might be a portable device running on battery power, the total load on the +5V from the host must be limited to 1 mA maximum when the display has local power.
5	Is clock stretching required?	Ref. Section 2.2

	Question	Answer
		Yes, compliance with VESA E-DDC standard requires that the requirements of the I^2C specification are fully met.
6	Will +5 volt supply continue to be required?	As noted in section 4.2 there is currently a requirement for the host device to supply 5 volts ± 5% to the display to ensure that the EDID data can be read even if the display is switched off. It is anticipated that this requirement will change to 3.3 volts in a future revision of this standard. In order to ensure an orderly migration with maximum interoperability it is recommended that new display designs operate using 3.3 volts AND are tolerant of a 5 volt supply from the host.

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