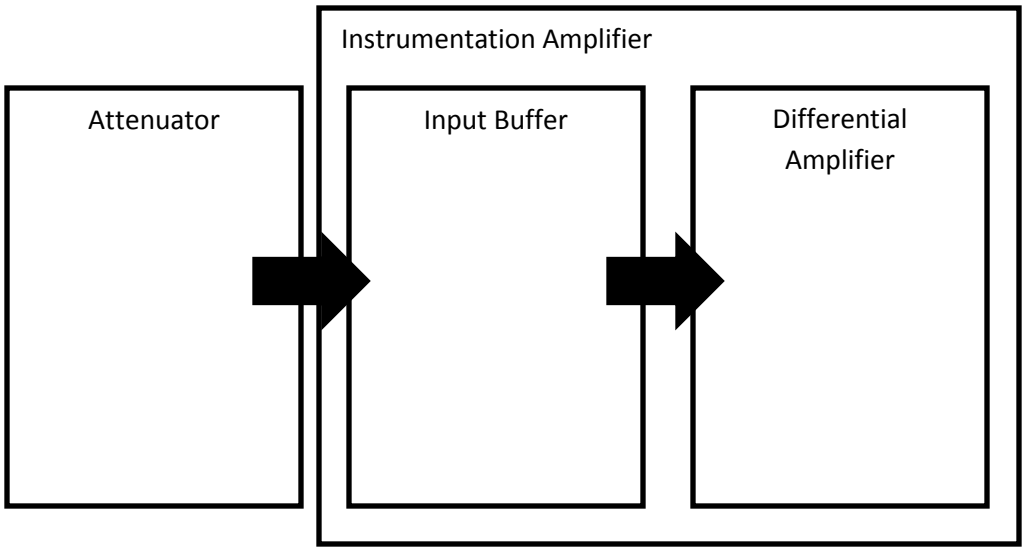
High Voltage Differential Probe Design

Requirements:

- 20+ MHz of bandwidth
- 1/1000 and 1/100 attenuation
- +-2kv differential input (maybe up to 5)

Top-Level Description:



The attenuator is a high-impedance voltage divider.

The next two stages are just an instrumentation amplifier. The input stage uses high-impedance JFET input op-amps to buffer the input signal for the differential amplifier.

In my drawings:
Red is in the top plane
Green is in the bottom plane
VCOM is ground
VCC is +5V
VDD is -5V

Attenuator

Large value resistors rated for 1kV are used to build the voltage divider for both the positive and negative inputs of the probe. A switch selects between 1/100 and 1/1000 attenuation by shorting one of the resistors in the divider. The node labeled INP is the input to the positive buffer.

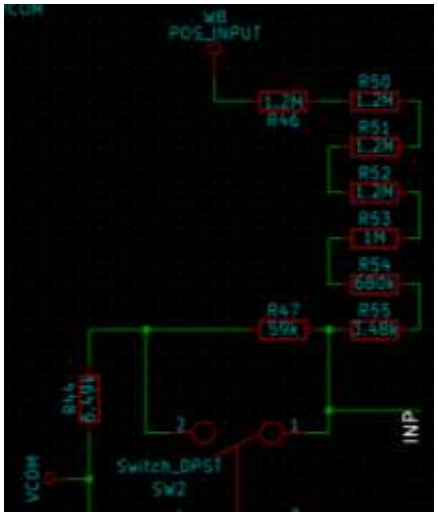
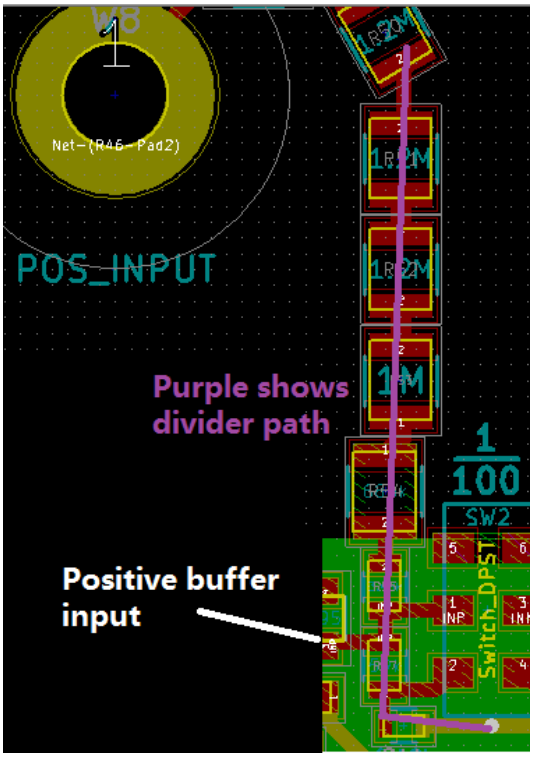


Figure 1: Schematic of the positive input voltage divider. The switch shorts R47 to change the attenuation from 1/100 to 1/1000.

Copper around the inputs and the voltage divider is removed on both the top and the bottom layers to prevent arcing from the divider to the ground plane. Copper beneath the pads of the node going to the buffer input is removed to reduce capacitance (according to layout recommendations on the data sheet for OPA659.) Note that the input node extends through the switch if the switch is set for 1/1000 attenuation. Figure 2a shows the circuit layout for the positive divider. The green hash marks show keep-out areas in the ground plane where the ground plane will not be poured.



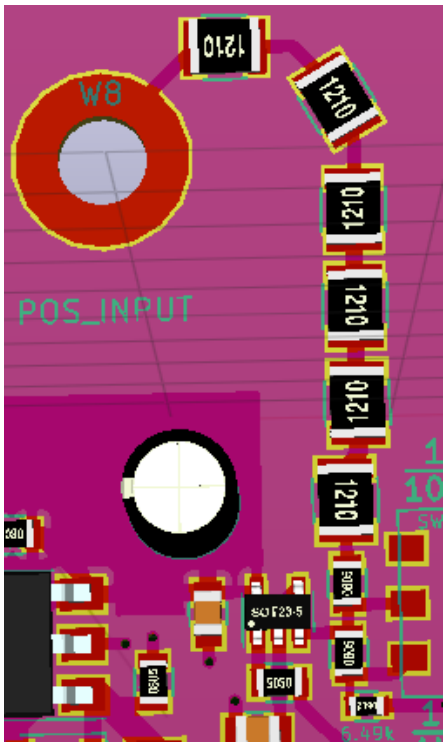


Figure 2:
Left- the circuit layout for the positive resistive divider.
Right- 3D model showing the spacing of the parts

Input Buffer

JFET input-op amps were used for their high input impedance. The OPA659 seemed to have good characteristics for this application. The positive and negative buffers are symmetric. Values for the decoupling capacitors were taken from the layout recommendations section in the datasheet.

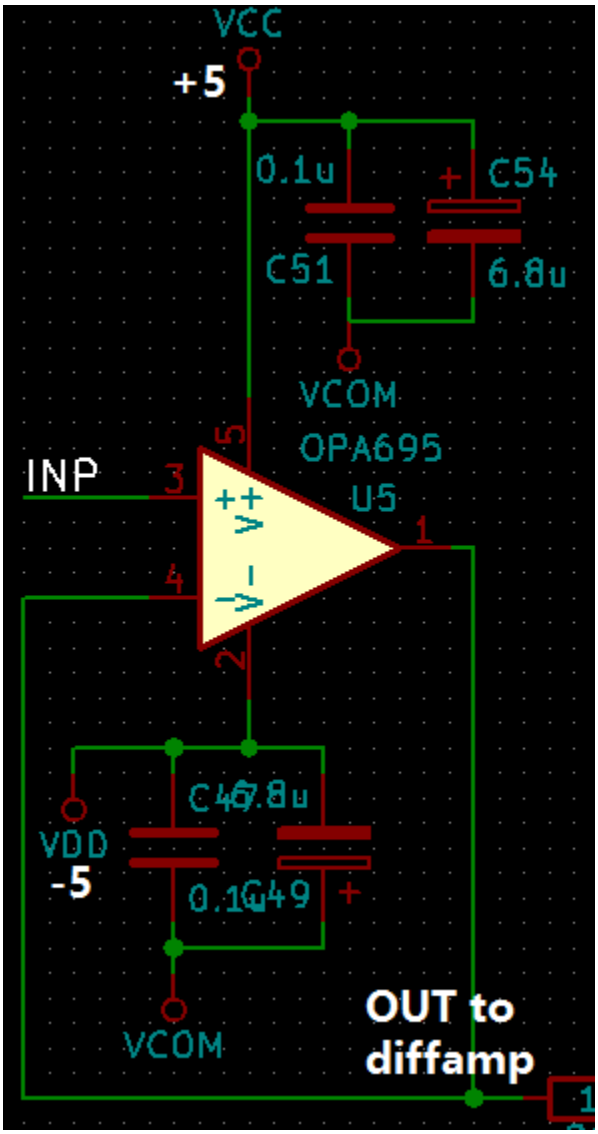


Figure 3: The high input-impedance input buffer circuit.

In the layout, I attempted to keep trace lengths as short as possible and minimize parasitic capacitance around the op amp. The ceramic decoupling capacitors were placed very close to the supply pins of the op amp. I am concerned with how the output resistor crosses over the negative supply because I am not sure if this will cause problems. Figure 4 shows the layout.

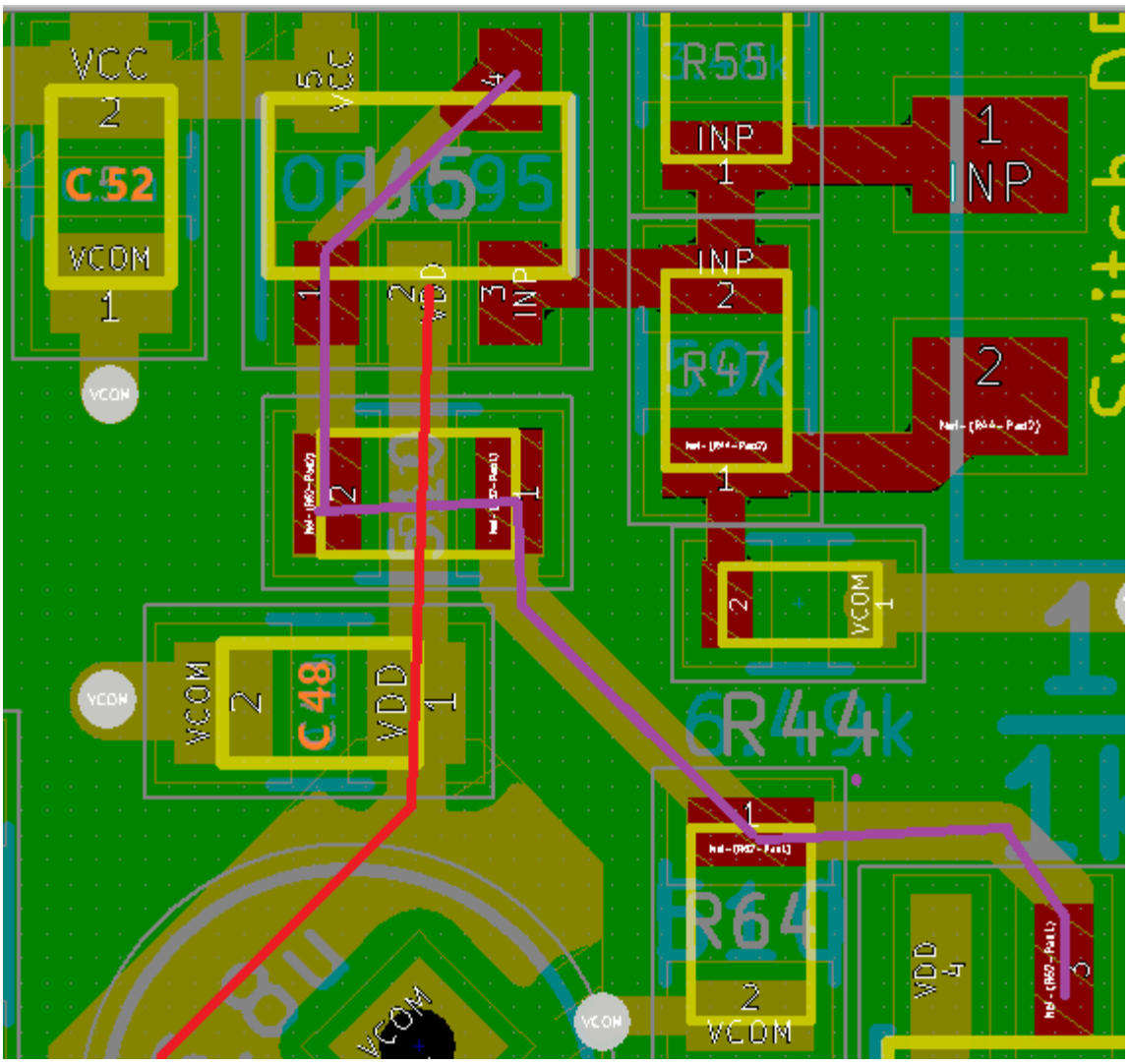


Figure 4: Positive input buffer layout
C52 and C48 in orange are the decoupling capacitors for the supply pins. The purple line shows the feedback path between the op amp pins as well as the output through a resistor to the differential amplifier input. The output crosses over the negative supply shown in red. Will this layout have any negative impacts on performance?

The circuits are symmetric, but the layouts are not, so I will post the negative input side as well, although it is very similar, so I will include the negative layout as well.

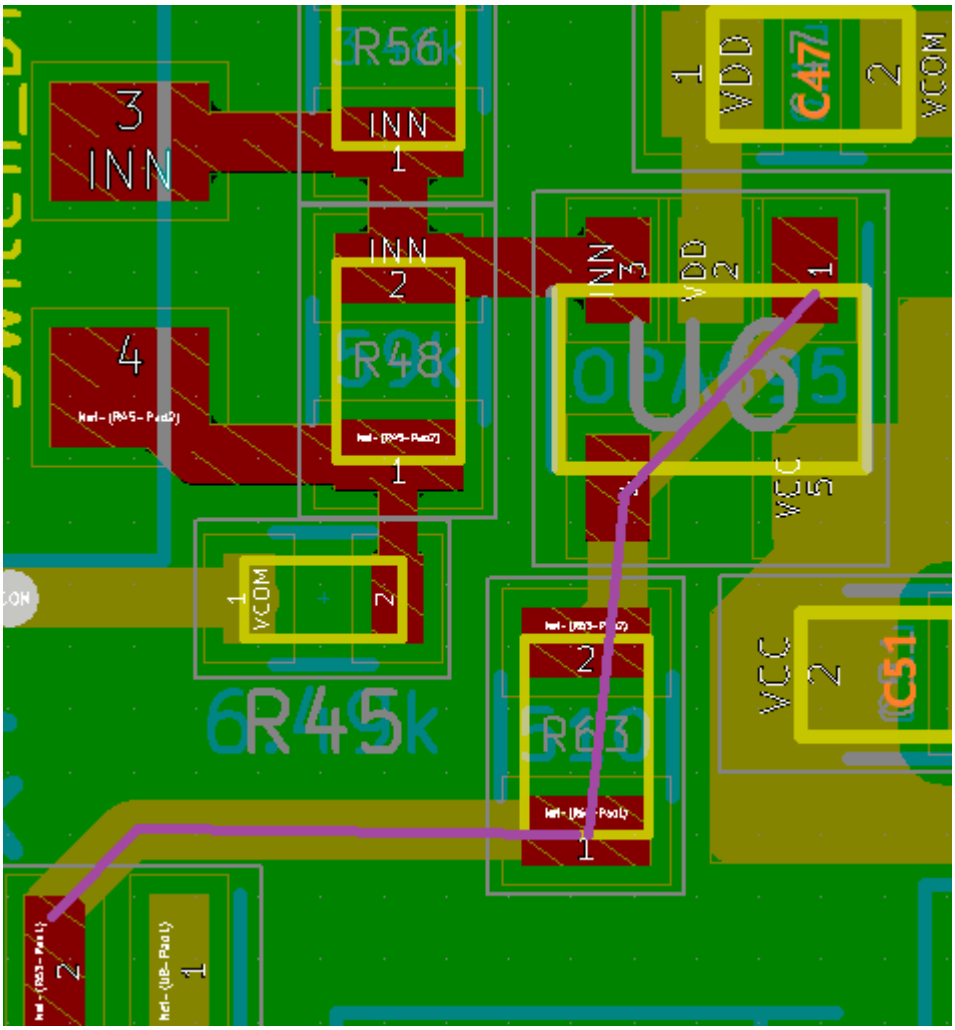


Figure 5:
The negative input buffer.
The orange capacitors are the ceramic decoupling capacitors and the purple line shows the feedback path and output to the differential amplifier.

I also included a 3D view of the positive and negative buffers below.

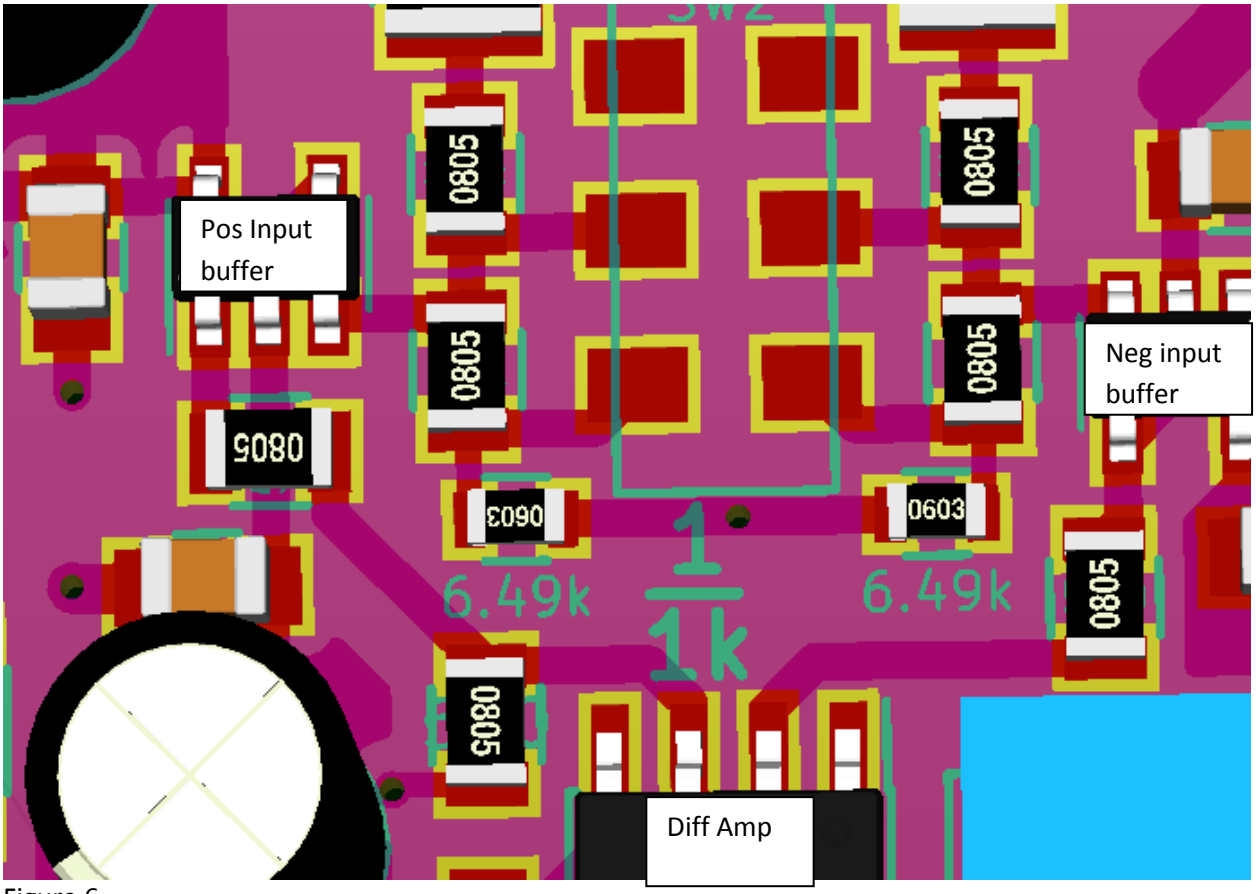


Figure 6
A 3D view of the input buffers and their connection to the differential amplifier.

Differential Amplifier

The LM7171 was used for the difference amplifier. This part was tricky to select because optimizing stability and bandwidth was an issue. The THS3091 had a very good frequency response with less phase shift, but the CMRR decayed to -25 or -30dB at 20MHz which seems pretty bad.

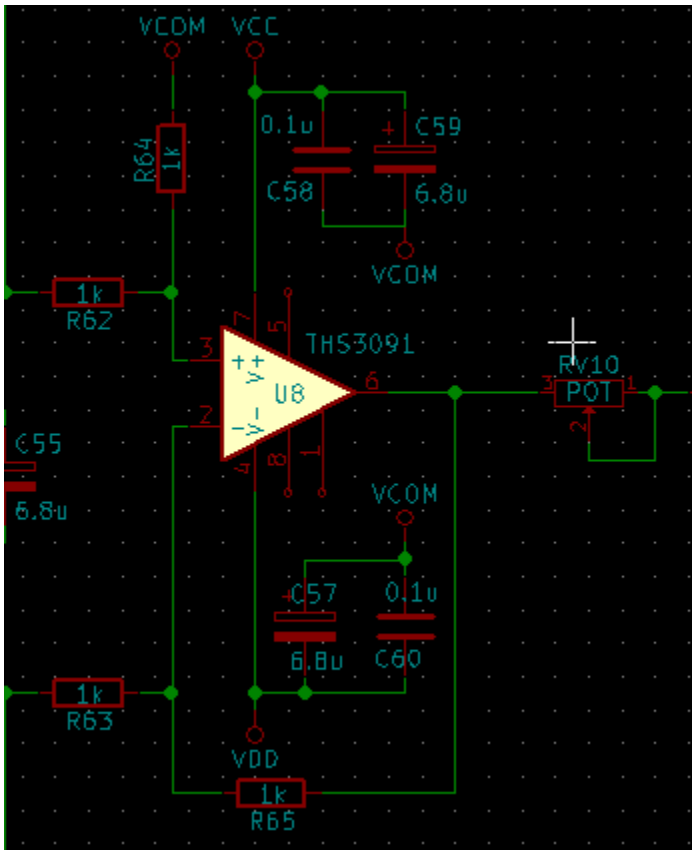


Figure 7:
Difference amplifier set for unity gain. The potentiometer at the back is a 200ohm 25 turn trimmer to adjust frequency response depending on the capacitance of the load.

The inputs to the difference amplifier are the two outputs from the input buffers. Similar steps were taken to reduce capacitance on the inputs.

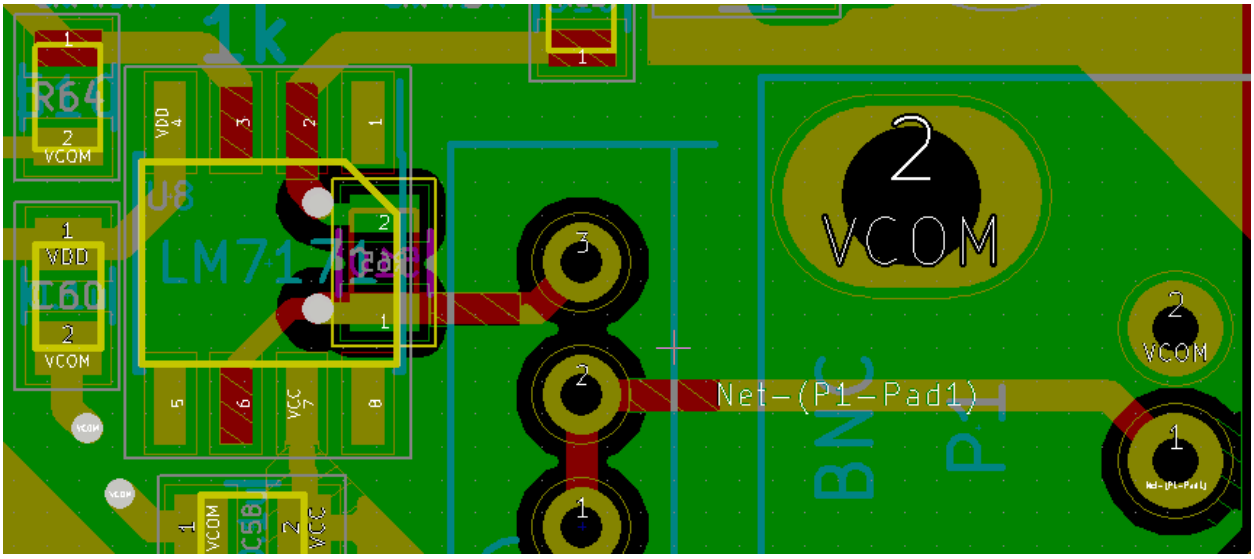


Figure 8:
The difference amplifier.
C58 and C60 are ceramic decoupling capacitors. The 200ohm trim potentiometer is on the right with its output headed to a BNC jack. The feedback resistor is on the back side of the board to reduce the length of the feedback loop.

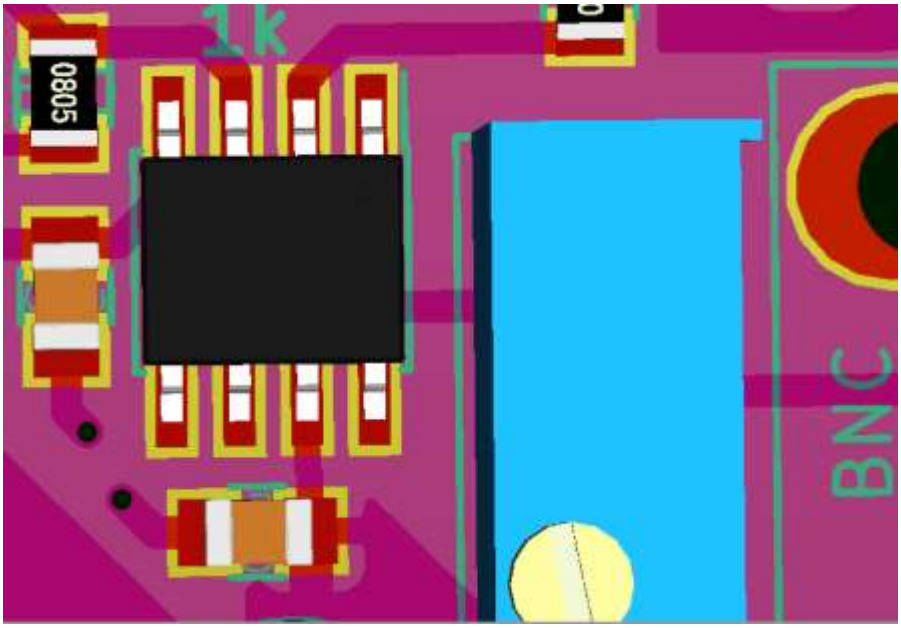


Figure 9:
A 3D view of the difference amplifier.

I have seen quite a bit of stuff about putting waveguides on longer traces. Is this something I should consider for some of my longer traces? I am not too familiar with reflections and that sort of thing either. Do I need to worry about it much at 20-40MHz?

Power

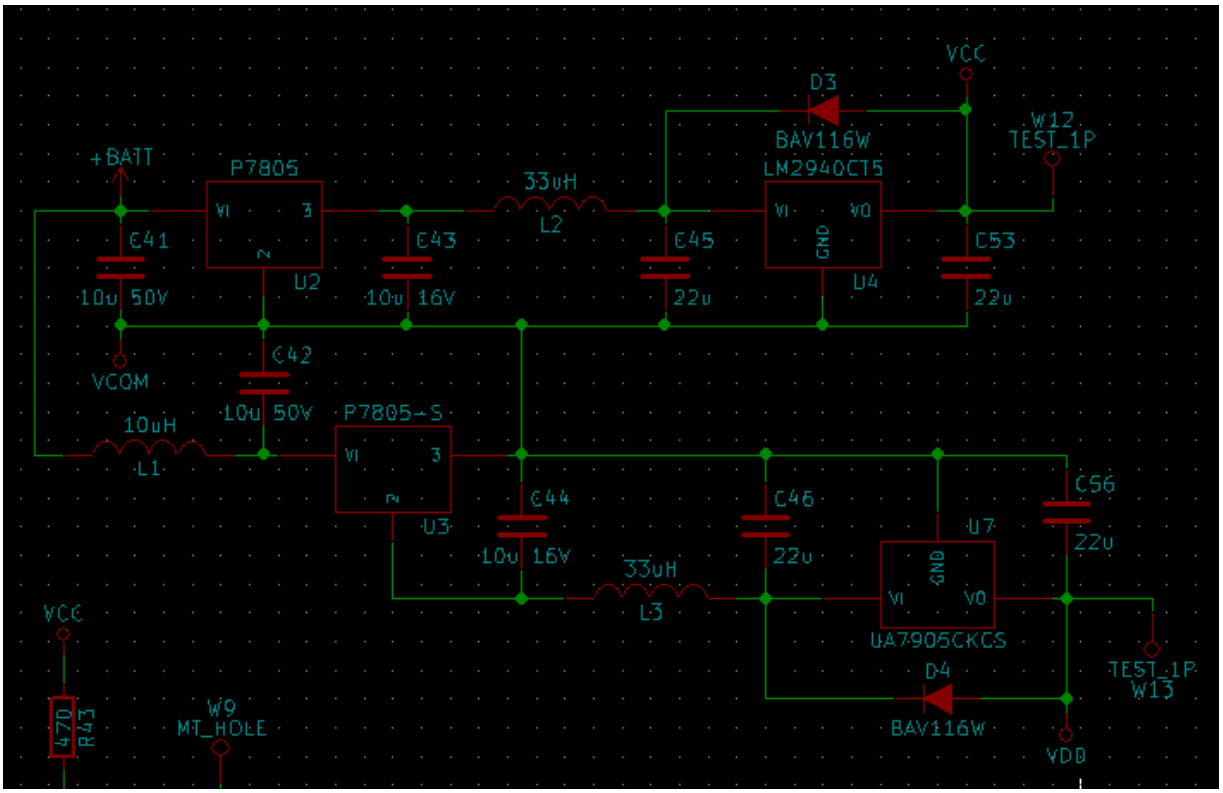


Figure 10:
Schematic of the power section

This is the schematic for my power supply. It uses two + and – 6.5V switching supplies to take 9V from a battery down to ±6.5V. After some filtering the power is passed to some linear regulators which hopeuflly knock any ripple down below 1mV.

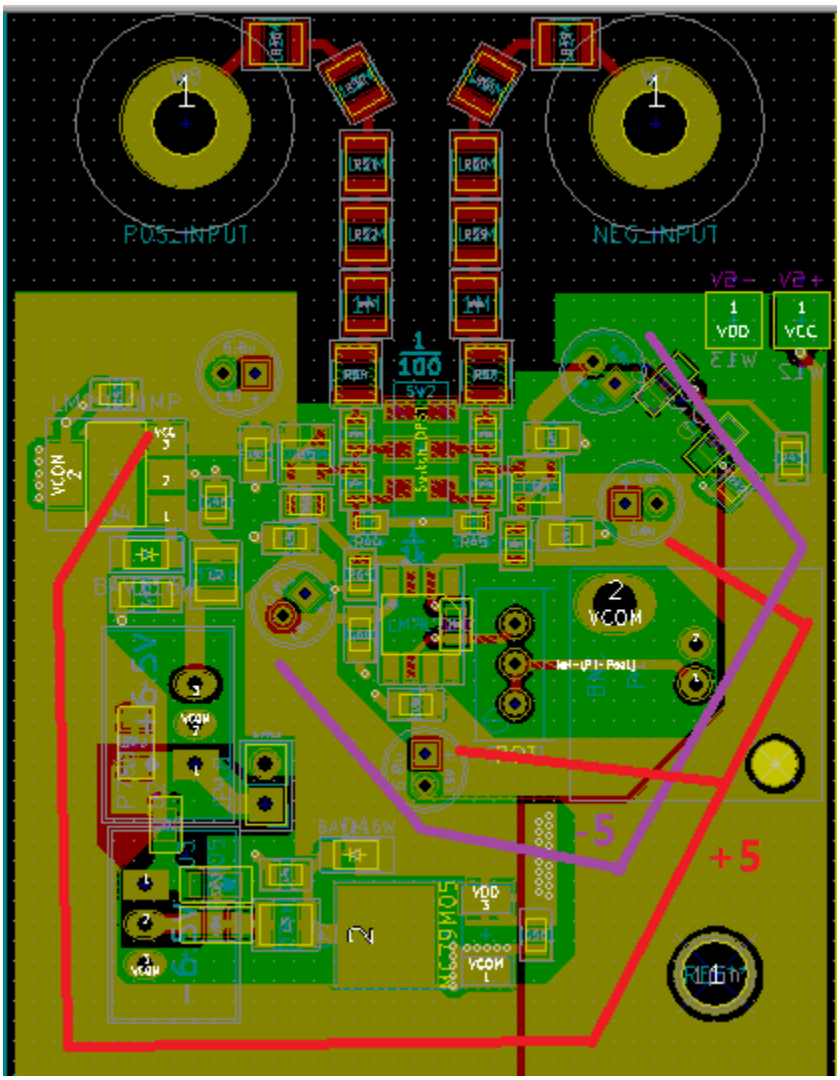


Figure 11:
Power Distribution. The red lines indicate +5V distribution and the purple lines indicate -5 Distribution. The ground plane is the green plane on the left half of the drawing.