Texas Instruments
High Speed Amplifiers

Simple Transimpedance Designs Using High Speed Op Amps

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Agenda

- Basic Issues
- Detailed Design equations
- Examples of Simple Design
- Advanced Transimpedance Designs
- Measuring Frequency response for Capacitive source circuits

- Detecting and amplifying the often very small current signal coming from a photodiode, can present a considerable challenge. The achievable gain, bandwidth, and input referred noise current are all coupled together in a few design variables.
- Most of this material comes from a series of articles referenced at the end where that material is also summarized in TI application note SBOA122.
- Many of the slides include more detail in the notes pages.

Design Issues Covered

1. Op Amp based, high performance, transimpedance designs can be analyzed using a single pole op-amp model to give a 2nd order closed loop transfer function. Although the full transfer function doesn't suggest a design approach, some judicious simplifications will lead to a very simple, and accurate, amplifier compensation methodology.

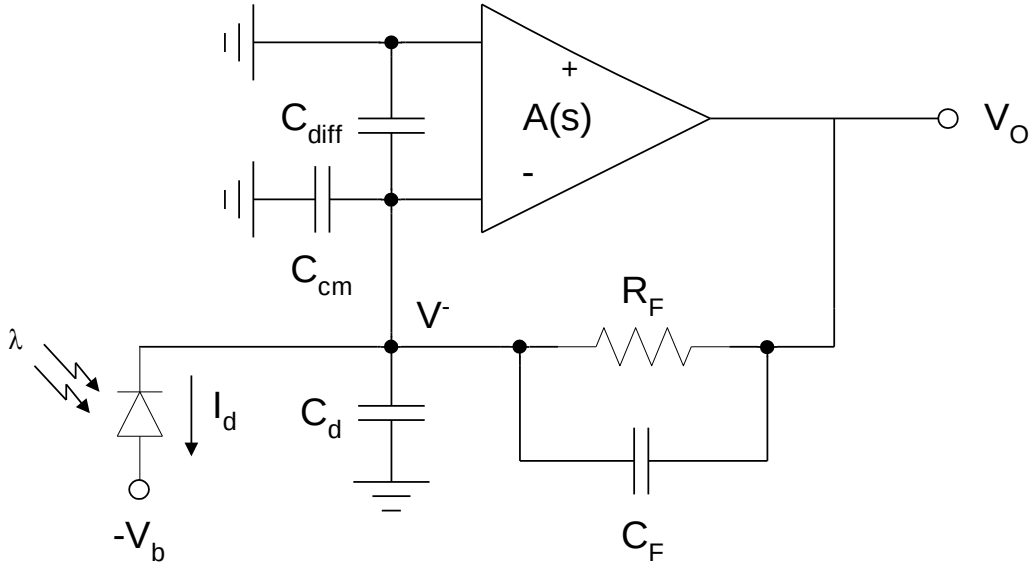
2. A simple equivalent input noise current equation, correctly including all of the high frequency terms (but neglecting 1/f effects), will allow an easy comparison between design solutions for their achievable sensitivity

Transimpedance Design (cont.)

- Numerous articles and discussion in the literature - several key misconceptions have complicated this application for many designers.
- Unity gain stability in the op amp is not required - a lot of literature suggests that it is.
- Feedback compensation is required even if a unity gain stable op amp is used.
- Many applications have an output noise spectrum dominated by the effect of the input noise voltage (not current) gained up to the output by the differentiator formed by the diode capacitance at the inverting node and the feedback resistor - this is often neglected.
- Putting the feedback pole at the intersection of the noise gain zero and the open loop gain curve is ideal? This is actually incorrect and yields a closed loop 2^{nd}-order response with a $Q \approx 1$ giving a step response that will overshoot and/or a frequency response that is peaking 1.25dB.

Transimpedance Frequency Response Analysis Circuit

- Deceptively simple looking circuit - that causes considerable difficulty in application. C_d is the diode capacitance plus wiring parasitic. C_s, used for design, is the total on the inverting node.



$C_s = C_d + C_{cm} + C_{diff}$

$V_O = -V^- A(s)$

Controlling the Frequency Response

- Key variables required to determine C_f to get the desired frequency response
  1. Total Capacitance on the Inverting node
     - Be careful to include the op amp input parasitic capacitance. Cd is the detector diode capacitance under the expected reverse bias plus wiring parasitic.
  2. Gain Bandwidth Product of the op amp
     - The higher the gain bandwidth, the higher the resulting closed loop transimpedance bandwidth. In general, the op amp does NOT need to be unity gain stable. As will be shown, loop gain x-over typically occurs at a very high noise gain - so very wideband, non-unity gain stable, op amps can be used to get their lower input voltage noise.
  3. Desired transimpedance gain or bandwidth
- These are interrelated - for a particular op amp selected, targeting the gain will set the maximum bandwidth or, conversely, targeting the bandwidth will set the maximum gain.

Full Laplace Transfer Function for the Transimpedance Op Amp Configuration

$$\frac{V_O}{I_D} = R_F \cdot \frac{\frac{A_{OL}\omega_A}{R_F\left(C_s + C_F\right)}}{s^2 + s\left(\omega_A\left(1 + A_{OL}\frac{C_F}{C_s + C_F}\right) + \frac{1}{R_F\left(C_s + C_F\right)}\right) + \left(\frac{\left(A_{OL}+1\right)\omega_A}{R_F\left(C_s + C_F\right)}\right)}$$

Transimpedance Gain

Where:

$$A_{(s)} = \frac{A_{OL}\omega_A}{s + \omega_A}$$

Single pole, open loop gain model

$$\frac{A_{OL}\omega_A}{2\pi} =$$ Gain Bandwidth Product (GBP)

Standard ω_O and Q form for this 2nd-Order Transfer Function.

$$\frac{V_O}{I_D} = R_F \cdot \frac{A_{OL}}{A_{OL}+1} \cdot \frac{\omega_O^2}{s^2 + s\frac{\omega_O}{Q} + \omega_O^2}$$

$$\omega_O = \sqrt{\frac{(A_{OL}+1)\omega_A}{R_F(C_S+C_F)}} = F_O(2\pi)$$

$$Q = \frac{\sqrt{\frac{(A_{OL}+1)\omega_A}{R_F(C_S+C_F)}}}{\omega_A\left(1+A_{OL}\frac{C_F}{C_S+C_F}\right)+\frac{1}{R_F(C_S+C_F)}}$$

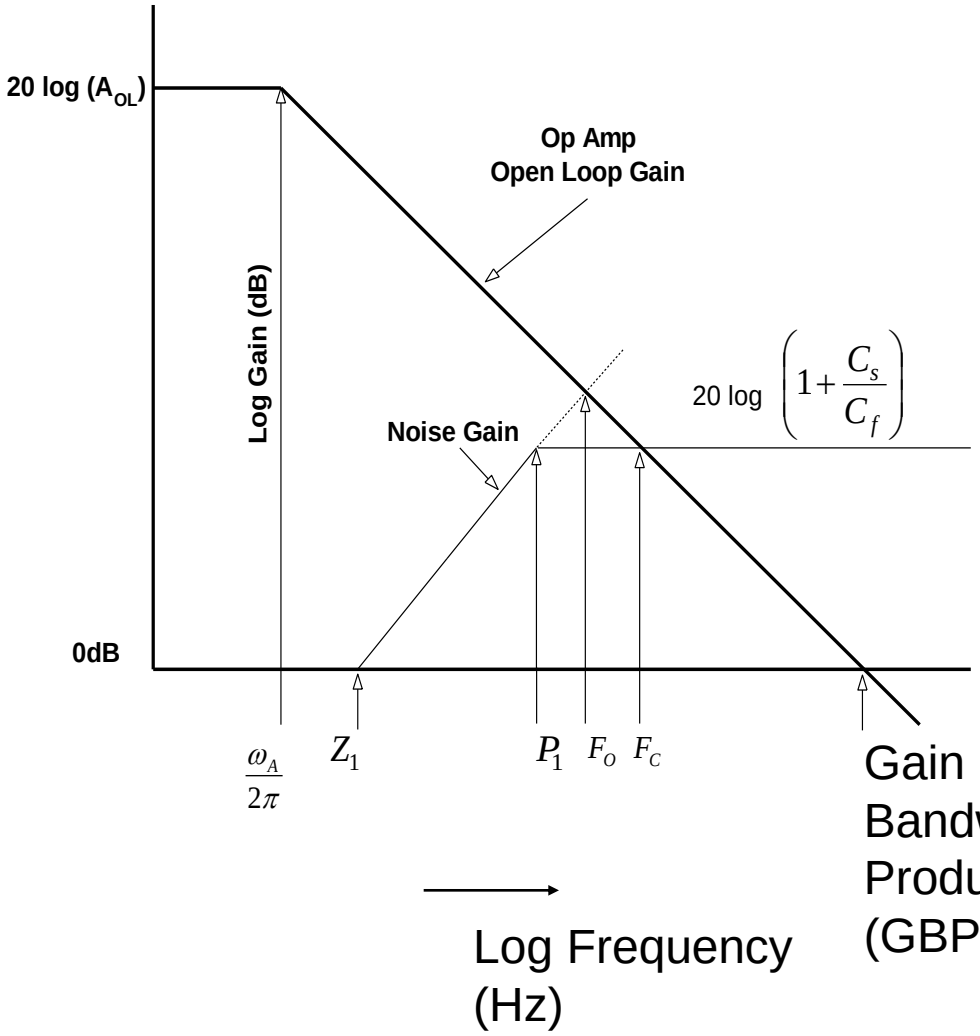
Loop Gain Analysis

- It is often instructive to look at the op amp circuit in loop gain form to view what each of the critical elements in the design mean graphically.

- The loop gain plot shows the open loop characteristic of the op amp with the noise gain superimposed - that gain starts out at 1 (0dB) then rises at Z_1 with single zero response caused by the feedback resistor and inverting input capacitance (C_s) up to the pole formed by R_f and C_f. Several important points to note -

    1. F_O is in fact the characteristic frequency of the closed loop response.
    2. Noise gain at x-over is $1+C_s/C_f$ which can be very high - hence, unity gain stability in the op am is not required.

Bode Plot of the Loop Gain for the Transimpedance Op Amp Configuration



$$Z_1 = \frac{1}{2\pi R_F (C_s + C_F)} Hz$$

$$P_1 = \frac{1}{2\pi R_F C_F} Hz$$

$$F_0 = \sqrt{Z_1 GBP}$$

$$F_C = GBP \Big/ \left(1+\frac{C_s}{C_F}\right)$$

Analysis Simplifications

- Algebraic simplifications to get an easy compensation solution.
  1. With $C_s >> C_f$, drop C_f from Z_1 Equation

  2. Let $(A_{OL} + 1).\omega_a/2\pi$ = GBP (gain bandwidth product in Hz)
     - This is simply neglecting the “1”

  3. Drop the “1” in $(1 + A_{ol}(C_f/(C_s+C_f))$

Simplified Expressions for Fo and Q

$$F_O = \sqrt{Z_1 \cdot GBP}$$

The 2nd-order characteristic frequency is fixed by
- the Amplifier Gain Bandwidth Product
- and the zero formed by the transimpedance gain resistor and the source capacitance

$$Q = \frac{F_O}{Fc} = \frac{P_1}{F_O}$$

The Q of the 2nd-order closed-loop transfer-function is simply the ratio of the pole frequency set in the feedback path to the characteristic frequency (P_1/F_O) which is also equal to the ratio of the characteristic frequency to the intersection of the open loop response.
with the high frequency noise gain ($1+C_s/C_f$) - this is F_O/F_c.

Design Methodology

- The next slide steps through finding the maximum available transimpedance gain for a given op amp and diode if a maximally flat Butterworth response is the target design. This target is interesting in that if we set P_1 at $0.707*F_O$, it circles back to give us a F_{-3dB} equal to F_O. Kind of unique and interesting design point.

- More general targets with peaking can be designed using the initial equations.

- A very useful alternative way to use these equations is to know your desired transimpedance gain and bandwidth and use them to solve for the minimum required GBP. Then the compensation capacitor (C_f) can be calculated using an amplifier with a GBP > than that minimum, along with this target transimpedance gain. The calculation for C_f is shown on the next slide.

Design Simplifications

- If a target of Q = 0.707 is set, a very simple design methodology results.
- At Q = 0.707, the 2nd-order closed-loop response gives an $F_{-3dB} = F_O$
- So, if we set $P_1 = 0.707*F_O$, we get an $F_{-3dB} = F_O$
- Assuming this - and then targeting an F_{-3dB}, sets the F_O target in a design.

$$F_{-3dB} = F_O = \sqrt{Z_1 GBP} \quad \text{(With Q = 0.707)}$$

$$Z_1 = \frac{\left(F_{-3dB}\right)^2}{GBP} = \frac{1}{2\pi R_F C_s}$$

Maximum achievable gain given $C_s, GBP,$ and target F_{-3dB}

$$R_F = \frac{GBP}{\left(F_{-3dB}\right)^2 2\pi C_s}$$

Simplified Design Continued

– With maximum achievable gain (R_F) set, can go back and set C_f to put P_1 where it needs to be for Q = 0.707

–
$$\frac{1}{2\pi \cdot R_F C_f} = P_1 = 0.707 \cdot F_O = 0.707 \cdot F_{-3dB}$$

$$C_F = \frac{1}{R_F(0.707) \cdot 2\pi F_{-3dB}}$$

Total Equivalent Input Current Noise Calculation

- The total input referred current noise equation that often appears in the High Speed Amplifier group de-compensated voltage feedback op amps uses several simplifying assumptions to arrive an approximate expression. Specifically -
  1. This is an integrated noise analysis that uses spot noise over frequency - not intended as a spot noise equation for narrowband applications.
  2. We are assuming the application is DC-coupled, pulse oriented where the integrated noise is of interest.
  3. The final signal bandwidth for both the transimpedance design and any post-filtering is >10X the 1/f noise corner for any of the op amp noise terms - this allows those effects to be neglected for integrated noise purposes
  4. While the amplifier must be compensated with a feedback capacitor, it is much simpler for noise calculation purposes to assume a noise power bandwidth lower than this that will be set further downstream in the signal path. This means the target transimpedance bandwidth should be set > than the bandwidth that will be set by post-filtering.

Total Input-Referred Equivalent Input-Noise Current for Wideband Transimpedance Design

$$i_{EQ} = \sqrt{i_b{}^2 + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n 2\pi F C_s\right)^2}{3}}$$

Simplified Transimpedance Noise Analysis

- A thorough expression for transimpedance output noise can be extremely complicated This principally arises from two issues –

1. Including 1/f effects in the analysis - neglecting those for broadband applications creates a slight error but considerable simplicity.

2. Allowing each noise term to be combined at the output with a frequency response set only by the transimpedance amplifier design itself. If we assume the transimpedance stage is designed to provide > than the desired final signal bandwidth, a post-filter downstream can be assumed for noise power bandwidth limiting purposes. That frequency “F” can then be used to calculate integrated noise.

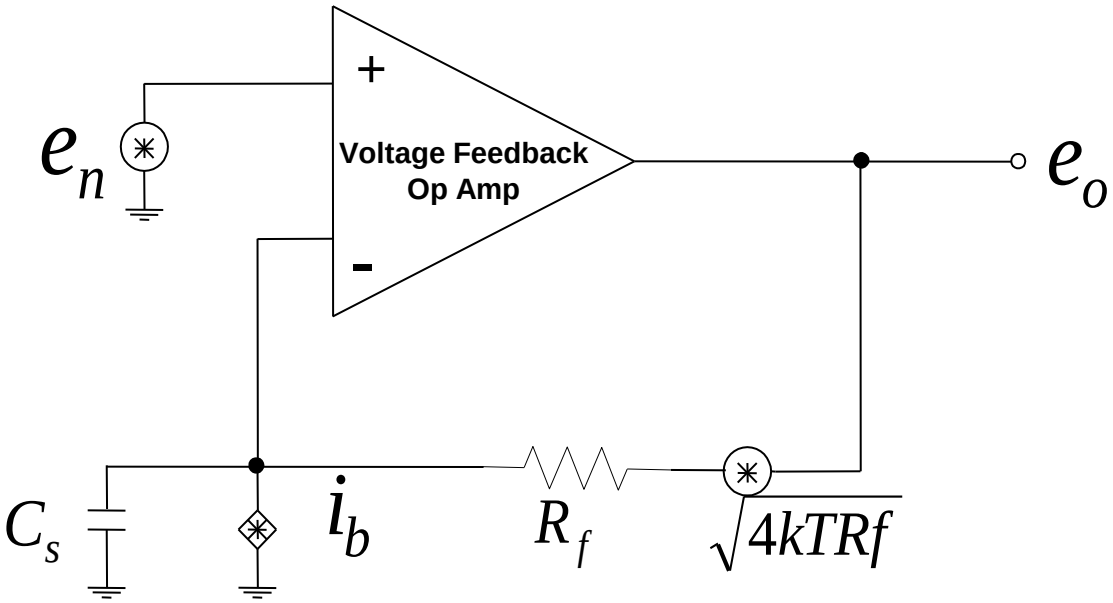
Input Noise Terms

- The input noise terms needed for a transimpedance design are shown on the next slide. These include –

1. Non-inverting input voltage noise (e_n - this will have a gain to the output of “1” at DC then increasing at 20dB/decade beyond $(1/2\pi R_f C_s)$Hz which is the zero frequency (Z_1) in the noise gain.
2. Inverting input current noise (i_{bi}) –
3. Feedback resistor noise voltage = $\sqrt{(4kTR_f)}$

- These last two terms will, strictly speaking, have a response pole to the output set by P_1. Since we will be assuming a post-filter below P_1, we will neglect this internal band-limit and just apply an integration frequency of “F” to all the noise terms.

Transimpedance Noise Analysis Circuit



Gain for the Noise Terms to the Output

- The resistor voltage noise shows up directly at the output with no gain. Square that to get noise power

- The amplifier's inverting input current noise shows up at the output times the feedback resistor. Square that to get the noise power

- The amplifier's input voltage noise has a gain to the output that traces out the noise gain curve shown earlier in the Bode analysis. Only the zero is considered here since we will assume a frequency of integration that is less than the pole and set by a post-filter. Again, square this output noise voltage term to get power.

Total output noise power

- To get the total output noise power, take each noise term times its gain to the output, square it, then add.

- Note that this circuit does not show a feedback capacitor - that capacitor (C_f) is absolutely required for stability but is not shown here since the noise integration frequency is assumed to be less than the pole set by $(1/2\pi R_f C_f)Hz = P_1$

$$e_o^{\,2} = 4kTR_f + (i_b R_f)^2 + e_n^{\,2}[1 + (2\pi f C_s R_f)^2]$$

Input-Referred Equivalent Input Noise Current

- Input refer e_o^2 by dividing by R_f^2

$$i_{eq}^2 = \frac{4kT}{R_f} + i_b^2 + \frac{e_n^2}{R_f^2} + e_n^2(2\pi \cdot f \cdot Cs)^2$$

Frequency dependent term

Getting an average value for the last term.

- The final term in the total input-referred noise-current expression increases with frequency - this is the differentiated input noise voltage of the op amp that will appear at the output. To get an average equivalent value, this must be integrated over F then divided by F. Strictly speaking, a starting integration value of 0Hz is not physically correct - but can be used as a simplification.

For f = 0 $\longrightarrow$ F

Average the noise power
of the 4th term over the noise power bandwidth - “F”

$$\frac{1}{F}\int_0^F (e_n 2\pi \cdot f \times Cs)^2 df = \left[\frac{(e_n 2\pi \times C_s)^2}{F} \times \frac{f^3}{3}\right]_0^F = \frac{(e_n \cdot 2\pi \cdot C_s \cdot F)^2}{3}$$

Input Referred equivalent input noise current

- This average value over “F” for the last term may now be combined with the other 3 terms that have no frequency dependence to get the total equivalent input referred current noise expression.
- This input referred spot noise current will integrate to the same total output noise power as the actual output noise spectrum if the frequency span of integration is limited to “F”. This expression is what shows up in the data sheets.

$$i_{EQ} = \sqrt{i_b^{\,2} + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n \cdot 2\pi \cdot F \cdot C_s\right)^2}{3}}$$

Equivalent Input Spot Current Noise for Output Noise Integrated to F < P_1

$$i_{EQ} = \sqrt{i_b{}^2 + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n \cdot 2\pi \cdot F \cdot C_s\right)^2}{3}}$$

Where:

i_b = Inverting input spot current noise for the op amp

$4kT = 16 \times 10^{-21}$ J at 290K

R_F = the feedback resistor value

e_n = Non-inverting input spot voltage noise for the op amp

C_s = Total capacitance on the inverting node of the op amp

F = Frequency limit of noise integration ($\leq P_1$)

Design Examples - Getting a Target Bandwidth Given a Source Capacitance

1. Select an Op Amp with a particular GBP - include its input parasitic capacitance + the source diode capacitance to solve for Z_1 given the desired bandwidth and actual GBP. With Z_1 set, solve for achievable maximum gain, = R_f to get the minimum input referred noise current.

2. Set P_1 at Q * F_O. Use this and R_f to solve for C_f.

3. Check that 1 + C_s/C_f > minimum stable gain for the op amp selected

Wideband VFB Op Amps Suitable for Transimpedance design

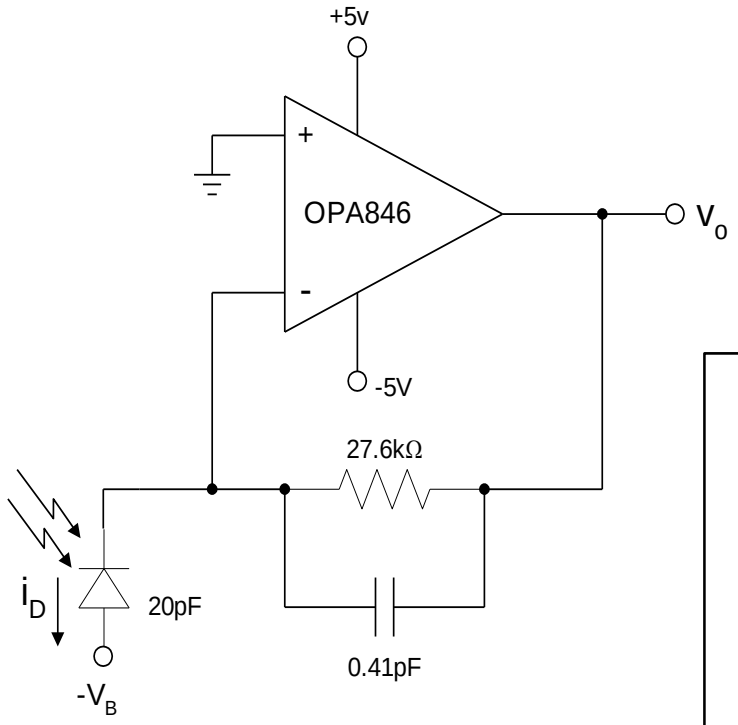
VOLTAGE FEEDBACK AMPLIFIERS SUITABLE FOR TRANSIMPEDANCE APPLICATIONS										
THIS IS LIMITED TO GBP > THAN 200MHz										
Part #	Input Type	GainBandwidth Product(MHz)	Minimum Stable Gain (V/V)	Input Voltage Noise (nV)	Input Current Noise (pA)	Min. Supply Voltage	Max. Supply Voltage	Supply Current(mA)	Multi-Channel Versions	
OPA820	Bipolar	240	1	2.4	1.6	5	12.6	5.6	Quad	
OPA690	Bipolar	300	1	5.5	3.1	5	12.6	5.5	Dual,Triple	
OPA842	Bipolar	200	1	2.6	2.7	7	12.6	20.2		
OPA843	Bipolar	800	3	2	2.8	7	12.6	20.2		
OPA846	Bipolar	1750	7	1.2	2.8	7	12.6	12.6	Dual	
OPA847	Bipolar	3900	12	0.85	2.5	7	12.6	18.1		
OPA656	JFET	230	1	7	0.002	7	12.6	14		
OPA657	JFET	1600	4	4.8	0.002	7	12.6	14		
THS4021	Bipolar	1400	7	1.5	2			8.1	Dual	
THS4031	Bipolar	200	1	1.6	1.2			8.5	Dual	
OPA355	CMOS	200	1	4	0.002			8.3	Dual,Triple	

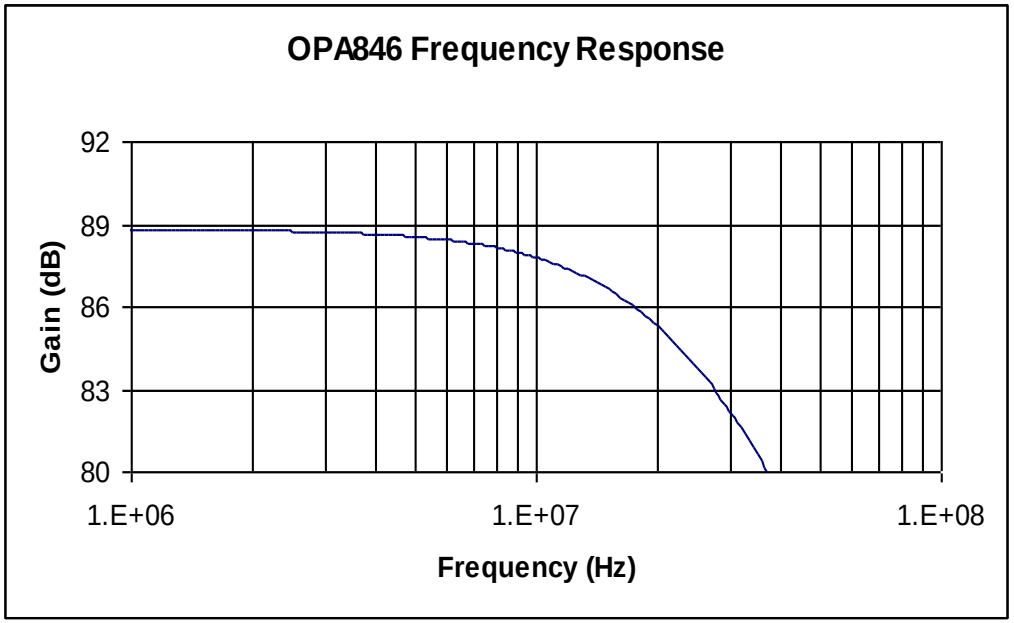
Example Design #1, 20Mhz from 20pF

In this case we are starting with a source capacitance a target bandwidth and an amplifier and seeing how high a transimpedance gain we can get, then we compute the input-referred noise, integrating through P_1.

OPA846 WIDEBAND, LOW NOISE, OP AMP	$1.59/(in thousands)
Gain Bandwidth Product (non-unity gain stable)	1750MHz
Non-inverting Input Voltage Noise	1.2nV/root Hz
Inverting Current Noise (Bipolar Input)	2.8pA/root Hz
Common-mode parasitic Input Capacitance	1.8pF
Differential parasitic Input Capacitance	2.0pF
Diode source Capacitance	20pF
Desired Butterworth (Q=.707) Bandwidth	20MHz
Maximum allowed Rf to get Bandwidth	27.6kohm
Required Cf	0.41pF
High Frequency Noise Gain (1 + Cs/Cf)	59V/V
Equivalent Input Current Noise Density (integrated to P1= .707*20MHz)	3.3pA/?Hz
Equivalent Input Integrated Noise (IRMS = IEQ*?P1)	12nARMS

Example Design Using a Wideband Bipolar Input Op Amp.



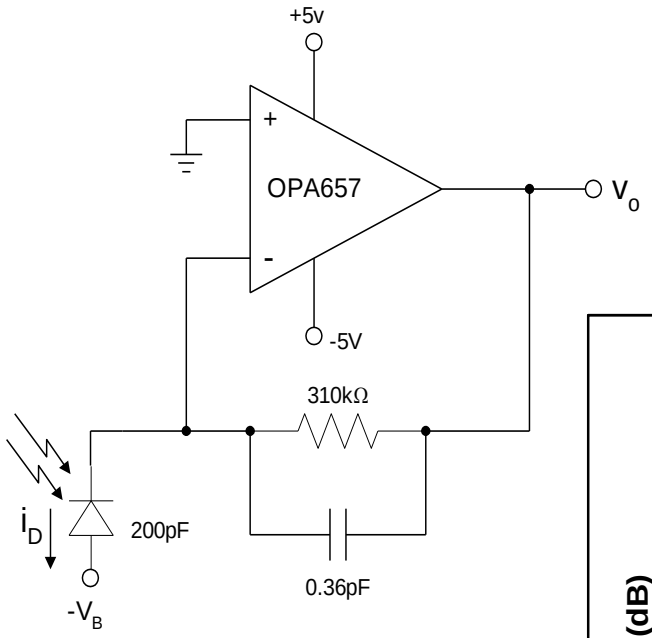


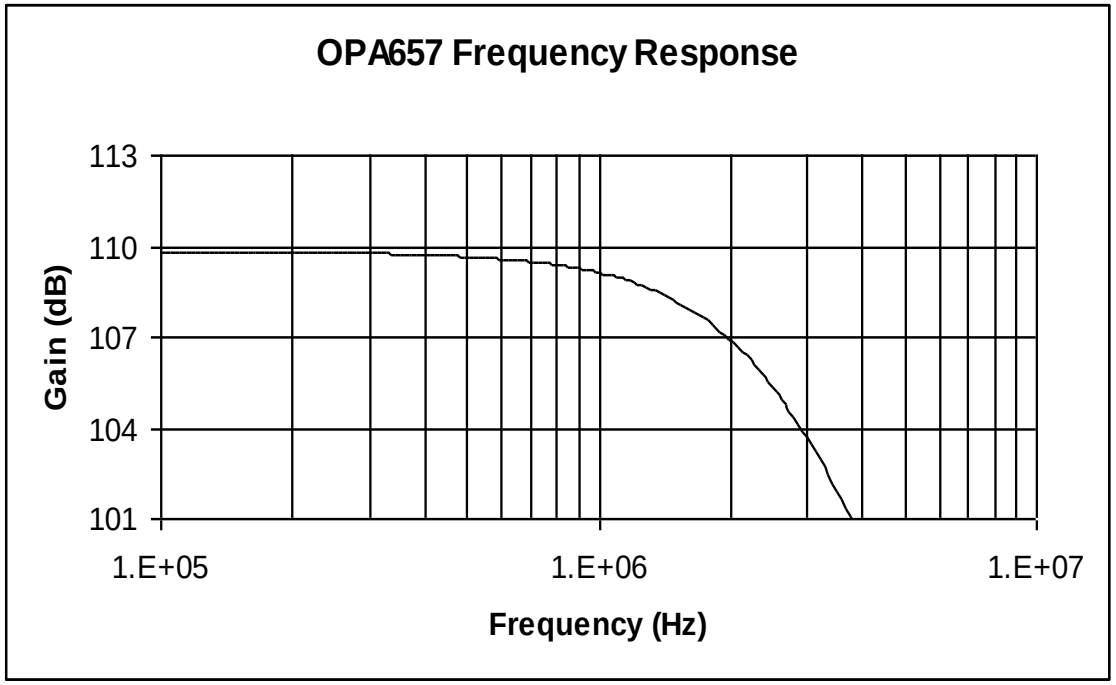
Example Design #2, 2Mhz from 200pF

In this case we are starting with a source capacitance a target bandwidth and an amplifier and seeing how high a transimpedance gain we can get then computing the input-referred noise, integrating through P_1. Here we select a JFET device as the R_f will be too high for a bipolar input bias current

OPA657 SPECIFICATION AND DESIGN	$3.59/(in thousands)
Gain Bandwidth Product (non-unity gain stable)	1600MHz
Non-inverting Input Voltage Noise	4.8nV/?Hz
Inverting Current Noise (Bipolar Input)	1.3fA/?Hz
Common-mode parasitic Input Capacitance	4.5pF
Differential parasitic Input Capacitance	0.7pF
Diode source Capacitance	200pF
Desired Butterworth (Q=.707) Bandwidth	2MHz
Maximum allowed Rf to get Bandwidth	310kohm
Required Cf	0.36pF
High frequency noise gain (1 + Cs/Cf)	380V/V
Equivalent Input Current Noise Density (integrated to P1= .707*2MHz)	5pA/?Hz
Equivalent Input Integrated Current Noise (IRMS = IEQ*?P1)	6nARMS

Example Design Using a Wideband JFET Input Op Amp



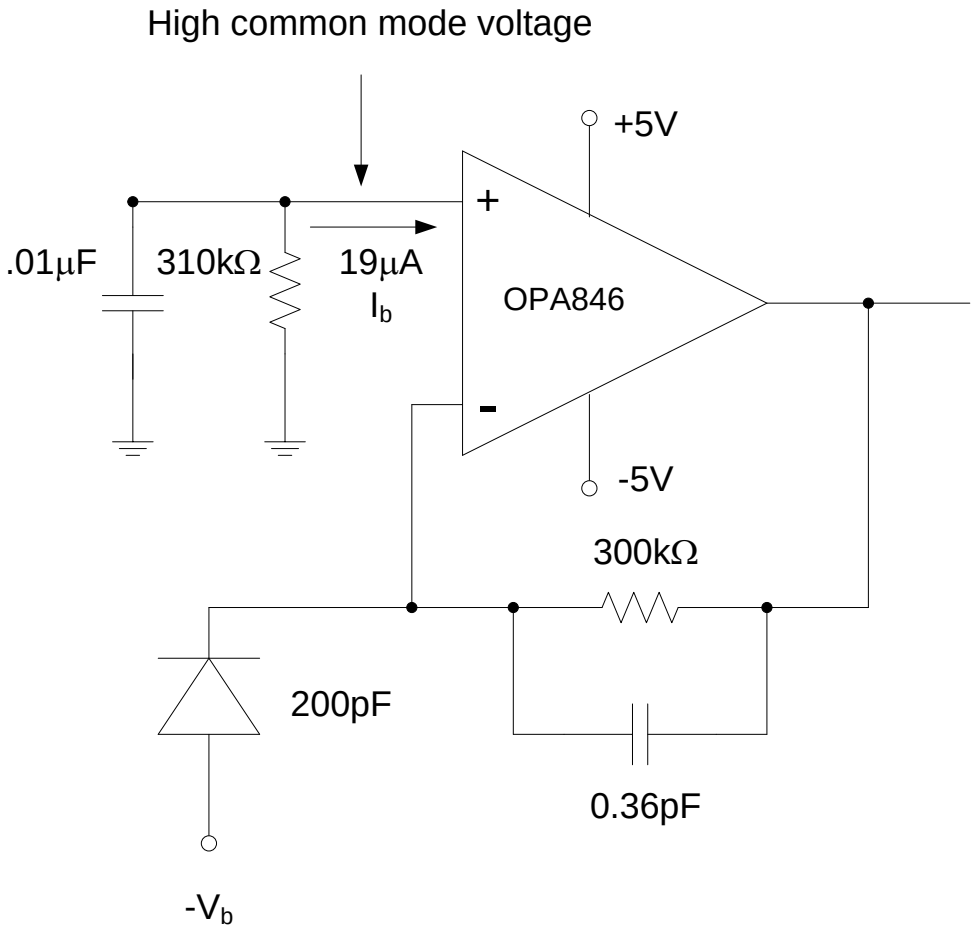


Design Discussion

- The OPA657 design yielded 5pA equivalent input noise current if we assume a noise power bandwidth limit set to 1.4Mhz. This is totally dominated by the 3rd-term of the total noise equation – the effect of the rising portion of the noise gain curve times the relatively high 4.8nV input voltage noise for the OPA657.
- Repeating this design using the OPA846, with its much lower voltage noise but much higher current noise, actually yielding a lower equivalent input noise current. – Specifically, the OPA846 will give the same bandwidth and an input noise of 3pA vs. 5pA for the OPA657.

- So why don't we use the OPA846??

High Gain Design Repeated with the OPA846



OPA846 Options at 310kΩ

- If we look at the effect of the OPA846's 19μA input bias current using a 310kΩ feedback, we would see a 5.89V output-offset voltage.

- Adding a 310kΩ resistor on the non-inverting input will allow bias current cancellation, but will now put a 5.89V common mode voltage on the inputs – which is out-of-range for a +/-5V operation.
- There is a way around this -

- The T-feedback structure has the interesting effect of also reducing the required input-matching resistor to get bias-current cancellation. This can be used to bring the input common mode voltage into range.
- Whenever this bias current cancellation is used for a transimpedance design, it is imperative to decouple that resistor to kill its noise contribution.

Adapting a Transimpedance Design to the T-Feedback structure

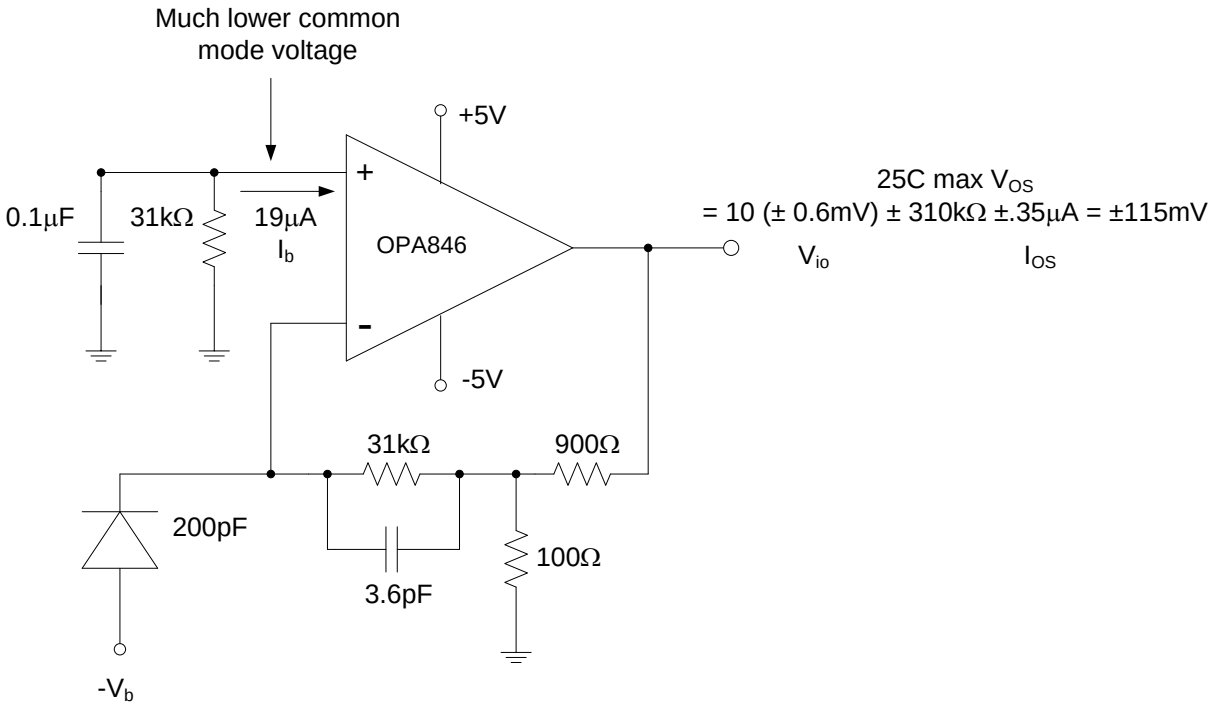
- Essentially, we implement an equivalent feedback impedance with an initial resistor out of the summing junction towards the output then implement a voltage divider that will have the effect of gaining up that impedance.

- From an initial single resistor design, decide how much voltage divider gain you want, divide the original resistor by that value and multiply the compensation capacitor by that value.

- The 310kΩ design is adapted to the OPA846 by using a gain of 10V/V resistor divider – this will reduce the required bias current cancellation resistor to 31kΩ significantly reducing the common-mode voltage generated by the input bias current.

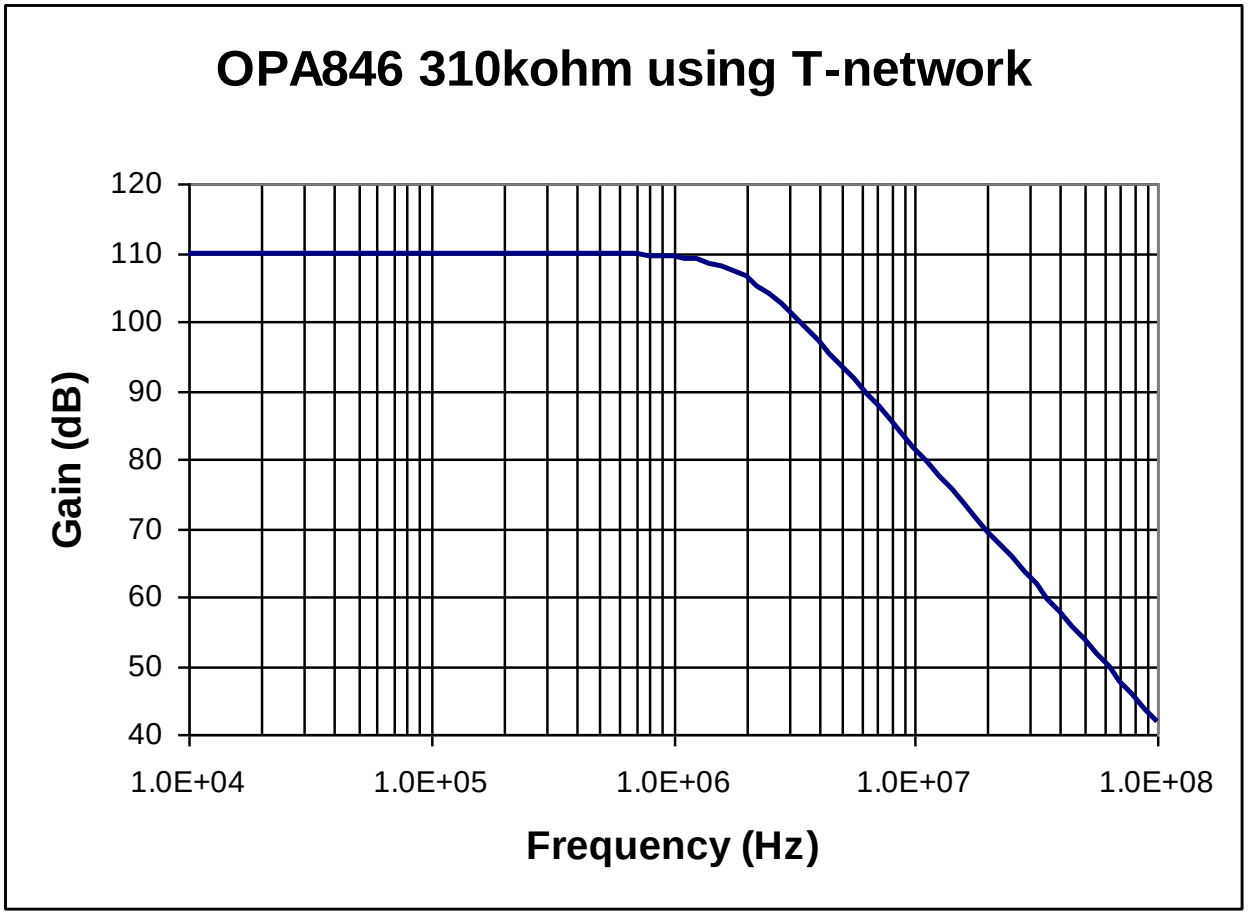
- That new circuit is shown on the next slide.

High Gain Design Repeated with the OPA846 Modified to the T-network in the feedback



This approach does work, but will have much higher output-offset voltage than the OPA657.

Modified OPA846 Transimpedance Frequency Response

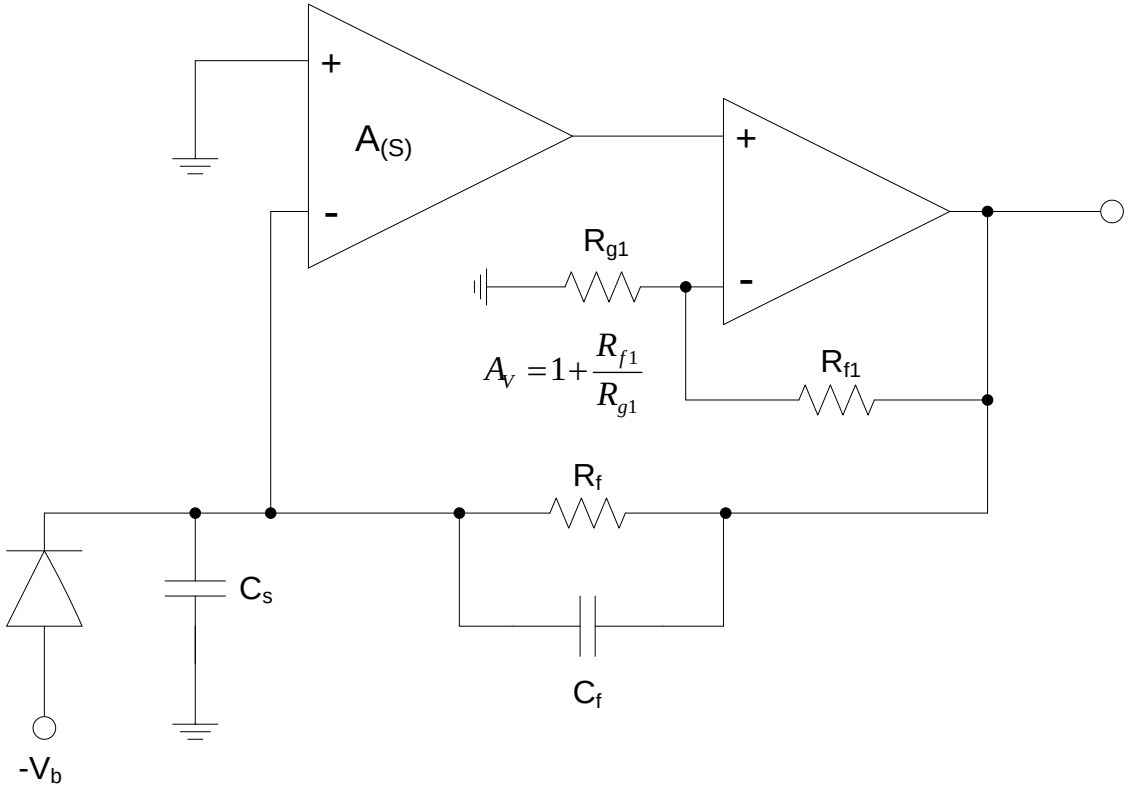


This also simulated out to approximately 3pA input-referred current-noise if F = 1.4MHz

Increasing Performance of a Transimpedance Design.

- If the required design does not reach the needed gain or bandwidth for a given detector capacitance, one way to improve performance without impacting noise too much is to use an imbedded gain stage.
- Adding a wideband gain stage inside the loop increases the gain-bandwidth product directly. This allows either the bandwidth for a targeted gain to be increased or the gain for a targeted bandwidth to be increased at a square-root rate.
- For instance, adding a gain of 4 inside the loop will give the option of either a doubled gain or bandwidth.

Embedded Gain Transimpedance Design



Use Av *GBP to work through this design.

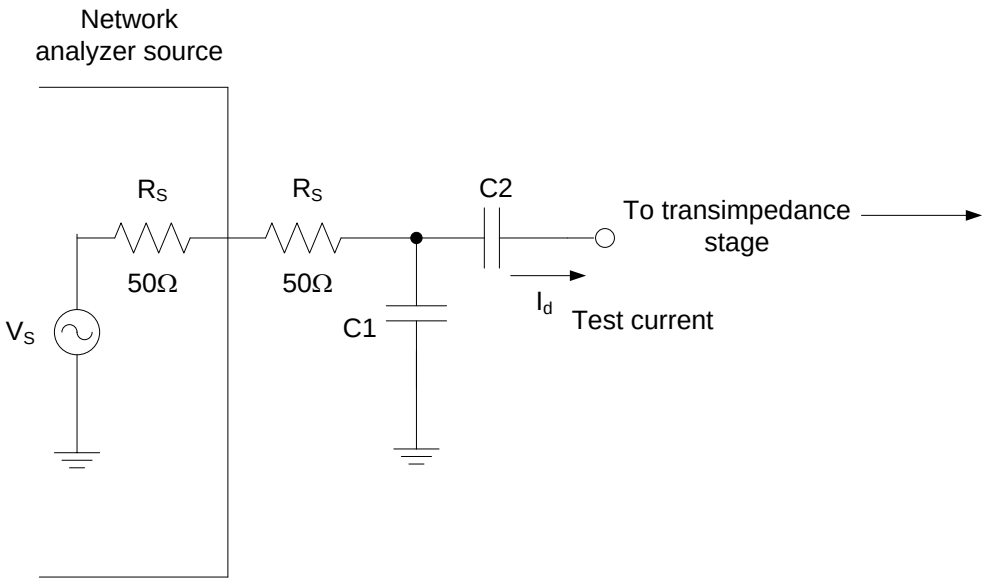
Using a Network Analyzer to Test a Transimpedance Amplifier Design

- Often, the actual diode and its response is not well known. It is very useful to be able to separately test the AC performance of a proposed design.

- This can be done using a network analyzer where it feeds first into a 50ohm series resistor and then into a capacitive divider.

- At higher frequencies, the capacitors short out and the network analyzer see its desired 50ohm termination.
- The caps. Act like a current divider sending a small portion of the current through the series 50ohm into the series cap that connects to the circuit under test.
- The apparent source impedance looking back into the circuit becomes the series capacitor at high frequency

Using a Network Analyzer to Test a Transimpedance Amplifier Design



Added Transimpedance Design Resources

- 1.“Control Frequency Response and Noise in Broadband, Photo detector Transimpedance Amplifiers” Michael Steffes
  - EDN, Design Feature - July 4th, 1996 pp113-125

- 2.”Embedded gain supercharges FET- transimpedance amplifier”. Michael Steffes
  - EDN, Design Feature – May 22nd, 1997 pp129-142

- 3. “Here’s an Easy Way to Test Wideband Transimpedance Amplifiers”. Michael Steffes
  - Electronic Design, Analog Application Issue - June 8th, 1998 pp74-80

- “Transimpedance Considerations for High-Speed Operational Amplifiers”. Xavier Ramus
  - http://focus.ti.com/general/docs/litabsmultiplefilelist.tsp?literatureNumber=sboa122

- High Speed Amplifiers offering from Texas Instruments that include a transimpedance design discussion and greater than 1.5GHz GBP.
  - OPA657, JFET Input, 1600MHz Gain Bandwidth
  - OPA846, Gain of 7 stable, 1750MHz Gain Bandwidth
  - OPA2846 dual, gain of 7 stable, 1750 MHz GBP
  - OPA847, Gain of 12 stable, 3900MHz Gain Bandwidth

Conclusions for Transimpedance Compensation and Noise Analysis

1. The closed loop response is a 2nd order low pass, where:
   1. The characteristic frequency is always the geometric mean of the zero in the noise gain and the op amp's gain bandwidth product.
   2. Placing the feedback pole only changes the Q of the response. Setting $P_1 = 0.707 * F_O$ will give a closed loop Butterworth response with $F_{-3dB} = F_O$
2. Since the noise gain always crosses over the open loop gain at a high value if compensated correctly, the op amp does not need to be unity gain stable.
3. The output noise can be strongly influenced by the peaked up voltage noise term.
4. Generally, Bipolar Inputs are better for low to moderate gains at wider bandwidths while JFET inputs are better for high transimpedance gains at lower bandwidths.
5. With Bipolar inputs, a resistor equal to R_f is placed to ground on the non-inverting input to improve DC accuracy - this must be bypassed with a capacitor to kill its noise contribution.
6. If high Rf are needed on a bipolar solution, consider the T-network approach to keep the common mode voltages in range.