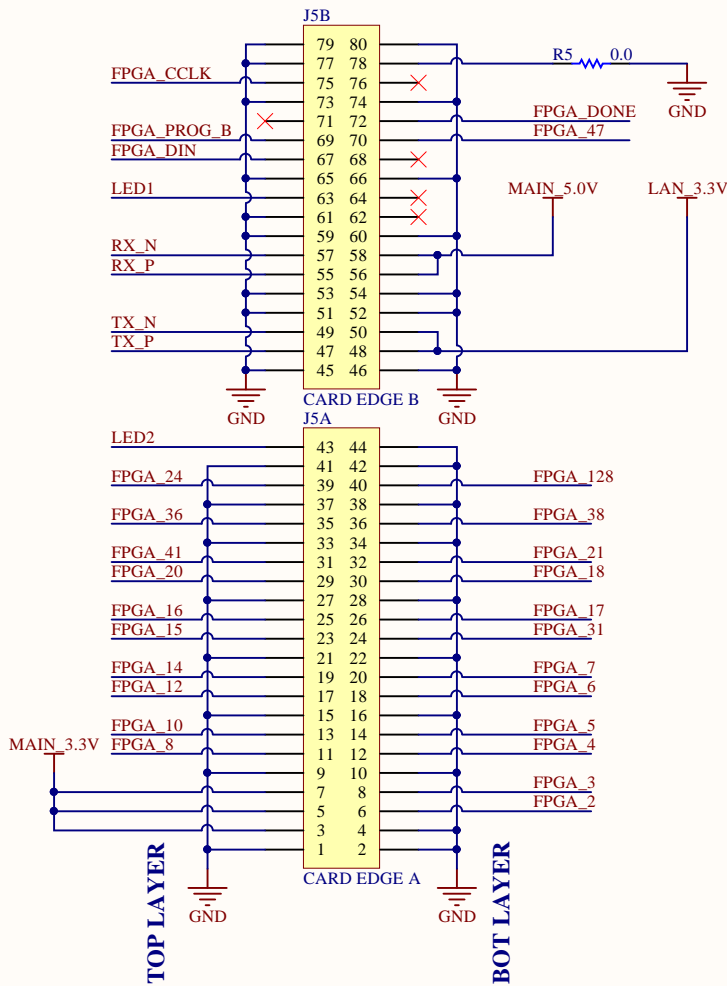
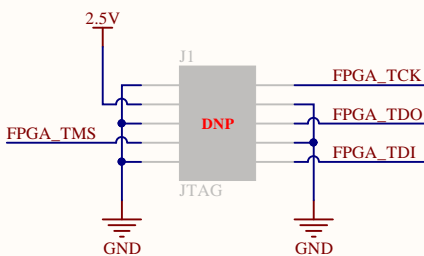


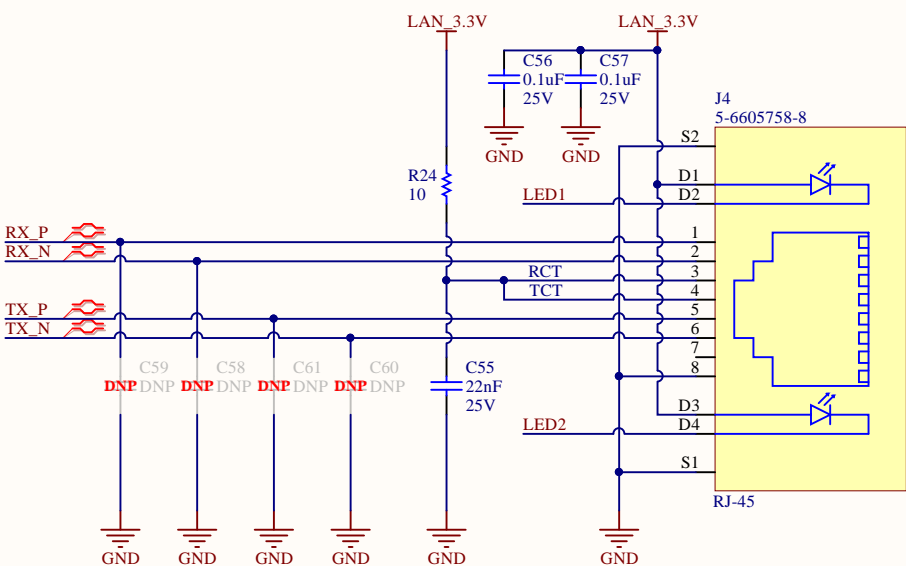
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1	INITIAL REVERSE-ENGINEERED DESIGN	06/11/2019	M LEWIS
2	ADDED MISSING CONNECTIONS	08/02/2019	M LEWIS



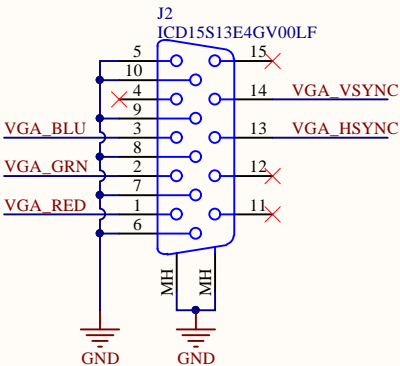
CARD EDGE CONNECTOR



JTAG



LAN INTERFACE

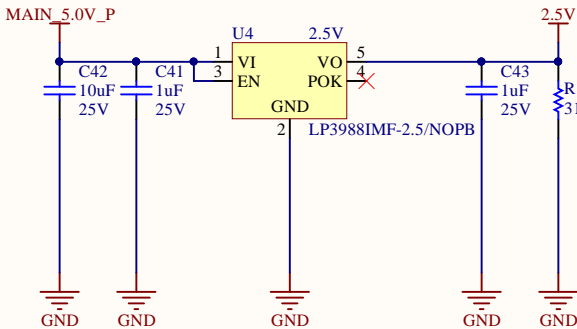


VGA CONNECTOR

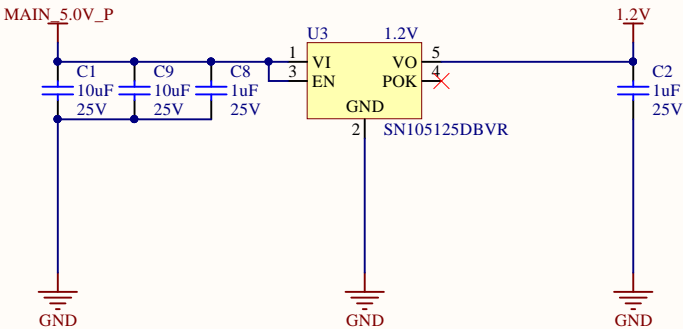
Title DSFAUXLAN MODULE			TEK15 SOLUTIONS	
Size: B	Number: ADB19-03	Revision: 2	M LEWIS	
Date: 8/3/2019		Sheet 1 of 5	(c) JUNE 2019	
File: (1)Connectors.SchDoc			DERSTROM8@AOL.COM	

Tek15

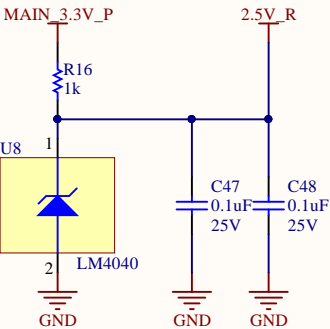
REV	DESCRIPTION	DATE	REVISED BY
1	INITIAL REVERSE-ENGINEERED DESIGN	06/11/2019	M LEWIS
2	ADDED MISSING CONNECTIONS	08/02/2019	M LEWIS



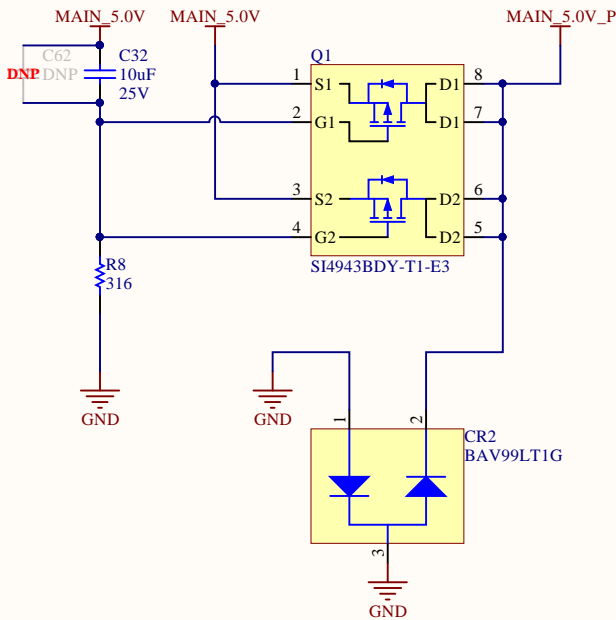
2.5V REGULATOR



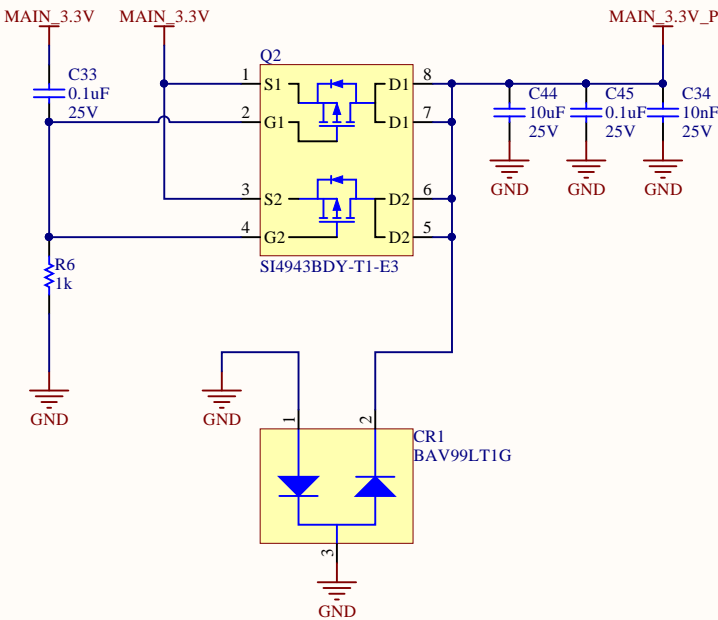
1.2V REGULATOR

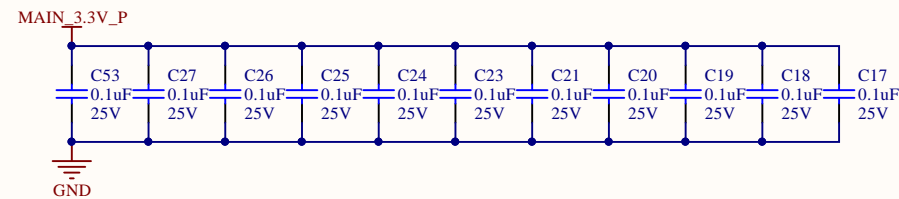


2.5 VOLT REFERENCE

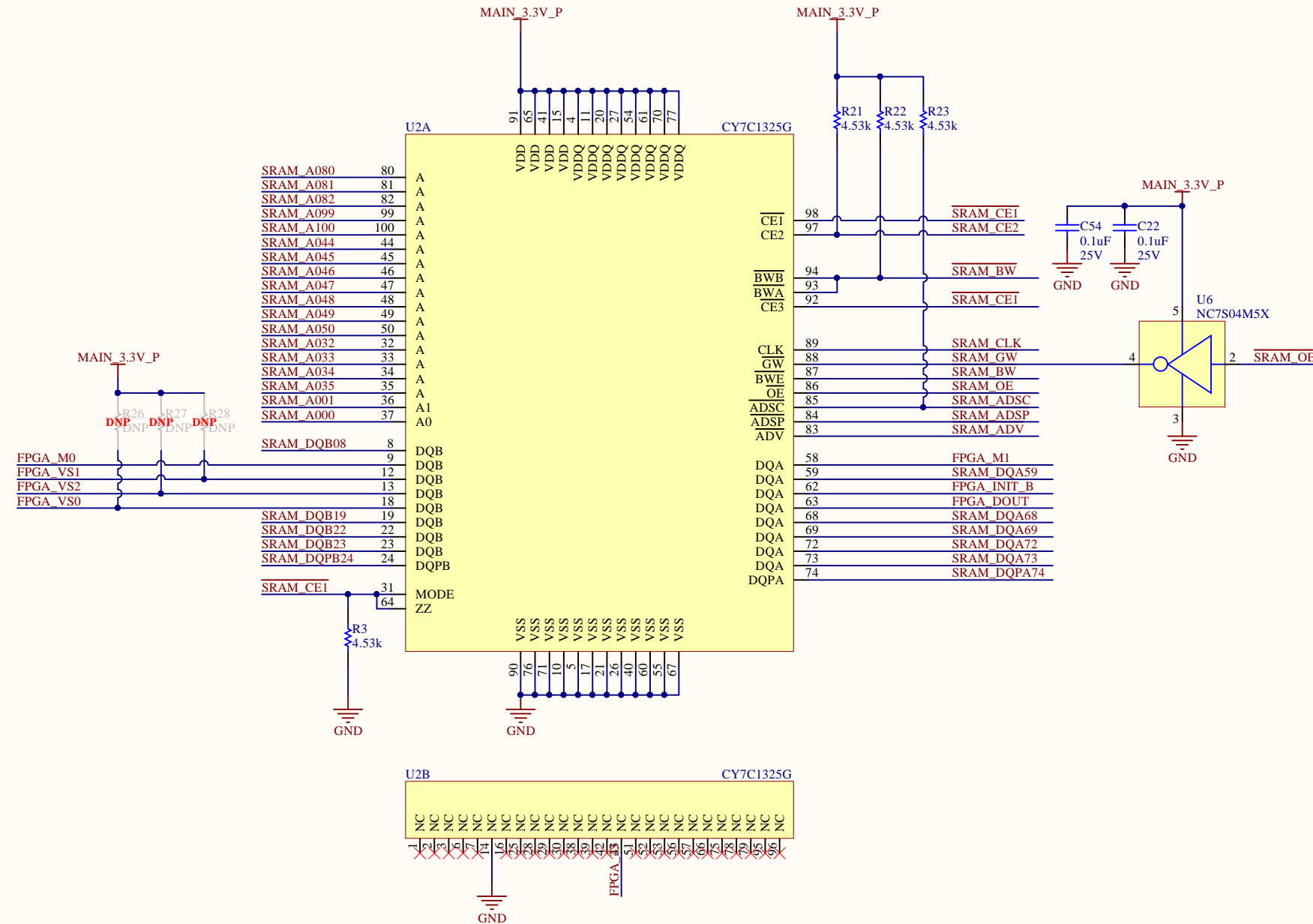


INRUSH CURRENT LIMITING





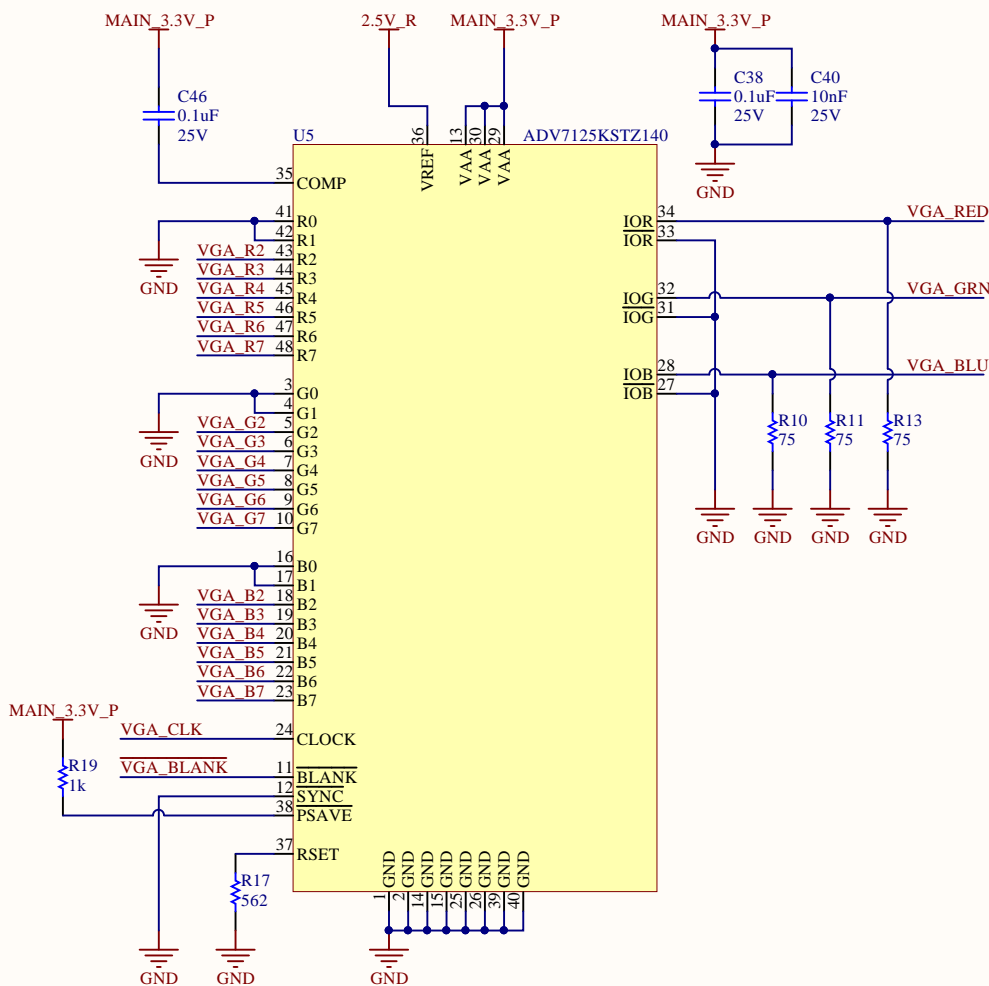
REV	DESCRIPTION	DATE	REVISED BY
1	INITIAL REVERSE-ENGINEERED DESIGN	06/11/2019	M LEWIS
2	ADDED MISSING CONNECTIONS	08/02/2019	M LEWIS



STATIC RAM

Title <i>DSFAUXLAN MODULE</i>			<i>TEK15 SOLUTIONS</i> <i>M LEWIS</i> <i>(c) JUNE 2019</i> <i>DERSTROM8@AOL.COM</i>		<div>Tek15</div>
Size: B	Number: ADB19-03	Revision: 2			
Date: 8/3/2019	Sheet 3 of 5				
File: (3)SRAM.SchDoc					

REV	DESCRIPTION	DATE	REVISED BY
1	INITIAL REVERSE-ENGINEERED DESIGN	06/11/2019	M LEWIS
2	ADDED MISSING CONNECTIONS	08/02/2019	M LEWIS



VIDEO DAC

Title DSFAUXLAN MODULE			TEK15 SOLUTIONS		<div>Tek15</div>
Size: B	Number:ADB19-03	Revision: 2	M LEWIS		
Date: 8/3/2019	Sheet5 of 5		(c) JUNE 2019		
File: (5)Video DAC.SchDoc			DERSTROM8@AOL.COM		