13.56 MHz Class E Power Amplifier with 94.6% Efficiency and 31 Watts Output Power for RF Heating Applications

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***Abstract*—Radio frequency power amplifiers (RF PA) are widely used for several applications e.g. wireless communication, wireless power transmission (WPT) and radio frequency heating. In general, the choice of power amplifier's operating class is based on requirements regarding linearity and power efficiency. For applications in which linearity is not a critical issue whereas high efficiency is desired, switched-mode amplifier e.g. class E is suitable. Switched-mode operation of class E offers high efficiency with a simple topology, leading to optimal costs of production and system operation. This work presents design and implementation of a high power and high efficiency 13.56 MHz class E power amplifier with parallel load circuit. As a power device, LDMOS was chosen. The fabricated class E PA provides Power-Added Efficiency (PAE) of 94.6% with 21.92 power gain when maximum output power of 44.92 dBm (31 W) is delivered to the load.**

Industrial, Scientific and medical (ISM) bands Class E PA with parallel load circuit.

Keywords—Class E; Power amplifier; Laterally Diffused Metal Oxide Semiconductor (LDMOS); Power-Added Efficiency (PAE); ISM band.

I. Introduction

For industrial heating applications, the RF frequency bands for industrial, scientific and medical (ISM) utilization including 13.56 MHz, 27.12 MHz and 40.68 MHz are widely used. The technique of using radio frequency electromagnetic energy to heat load materials referred to as dielectric heating [1] is suitable for materials with high dielectric loss e.g. fruit, meat, and grains [2]. One important part of the system is the high power RF source which contains a signal generator and a power amplifier. Efficiency and optimum power transfer are the key factors to be considered in the system design, which can be achieved by a proper design of power amplifier. High efficiency power amplifiers are also useful for wireless power transmission, which requires high efficiency of operation in order to achieve maximum power delivered to the load. A class E PA for wireless power transfer systems was demonstrated, for example, in [3]. For this reason, Class E PA, first proposed by Sokal [4], is widely used in various applications. The main advantages are its simple topology and high efficiency ideally up to 100%.

This paper presents design and implementation of a class E PA with 13.56 MHz operating frequency and parallel load circuit that can provide better efficiency than primitive shunt capacitance and shunt inductance circuit [5]. Load-pull technique was used to find the optimum load impedance for maximum PAE [6] during the design process. The aimed application of this high efficiency PA is acceleration of chemical reaction using RF electromagnetic energy in biodiesel research as there are promising results reported in the literature [16].

II. Design of Class E Power Amplifier

Class E power amplifier was proposed by Sokal in 1975. Several years later, a Class E amplifier with parallel circuit was proposed by A.V. Grebennikov [7], which provided better efficiency. Class E PA has maximum theoretical efficiency of 100%, the basic structure of Class E PA consists of an active device working as switch and a passive load network designed to minimize the overlap between drain (or collector in case of a bipolar junction transistor) voltage and current waveforms to avoid power dissipation in the active device, leading to maximum efficiency of operation.

A basic schematic of class E PA with parallel load circuit is shown in Fig. 1. The circuit consists of a power transistor as an active device and a load network. In the load network, there are a finite-dc feed inductor L, a shunt capacitor C, a series L_o-C_o resonant circuit, which tuned the output to fundamental frequency, and an optimum load resistor R.

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The design equations for load resistor R, finite-dc feed inductor L, and shunt capacitor C have been proposed by A.V. Grebennikov as follows.

$$R = 1.365 \frac{V_{CC}^2}{P_o} \quad (1)$$

$$L = 0.732 \frac{R}{2\pi f_C} \quad (2)$$

$$C = \frac{0.685}{2\pi f_C R} \quad (3)$$

The parameters of the series L_o-C_o resonant circuit, depending on an assumed load quality factor Q_L, can be determined by the following equations.

$$C_o = \frac{1}{2\pi f_C R Q_L} \quad (4)$$

$$L_o = \frac{1}{(2\pi f_C)^2 C_o} \quad (5)$$

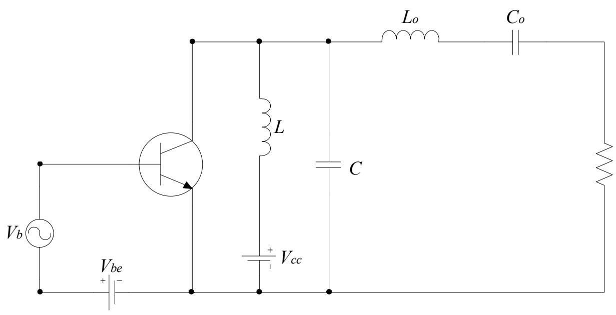

Fig. 1. Basic schematic of class E power amplifier with parallel load circuit.

In this work MRF6V2150BNR1 (LDMOS power transistor) from Freescale Semiconductor was chosen as the active device of the proposed class E PA. This transistor offers operating frequencies from 10 MHz to 450 MHz, maximum output power of 150 W, 110 V_{dc} breakdown voltage. For low frequency of operation, Si-LDMOS is a more suitable device technology compared to GaN MESFET or HEMT due to lower cost for mass fabrication. For the circuit design and simulation on PC using Agilent's Advanced Design System (ADS), a nonlinear transistor model of this device is provided by Freescale.

The design process started with the proper gate bias voltage selection. Since Class E PA operating point is the same as in Class B PA [8], the gate bias voltage should be set at the threshold level of the transistor, which is between 1 to 3 V as per manufacturer's document. Due to simulation of the I-V curves, the gate bias voltage was set to 2.2 V with 32 V drain supply voltage for an expected output power of 30 W in the first design.

The load resistance R depends on the value of the drain supply voltage and the output power, and can be calculated by equation (1). The shunt capacitance C and dc feed inductance L can be calculated by equations (2) and (3). The calculated value are 46.6 Ω, 175 pF, and 400 nH, respectively. For the resonant circuit, the values of a series L_o-C_o depend on the load quality factor Q_L. The equations (4) and (5) were used to find L_o and C_o in order to tune the output to the fundamental frequency of operation. From calculation, L_o is 547 nH and C_o is 252pF.

Since, load-pull simulation technique can provide optimum load impedance and flexibility to the designer to choose compromising load impedance, where the PAE can be traded with an increased output power, so the value of load impedance from simulation was used instead of the calculated load resistance R [6]. From the load-pull simulation, maximum PAE of 90.37% can be achieved with the output power of 45.21 dBm at a load impedance $\underline{Z_L}$ = 12.818 + j13.543 Ω. This impedance was selected, since the proposed design requires high efficiency of operation.

For optimal simulation result and circuit implementation, all calculated parameters and simulated load impedance were used for class E circuit simulation for the optimization in terms of efficiency and output power. Due to product availability, the value of each capacitor are slightly changed, so that the circuit required tuning to achieve the optimal point of operation. In this work, each inductor was designed, measured and fabricated in our laboratory, so the inductor can be easily used as tunable components. The final step in the design process was the design of input and output matching networks. Whereas the input matching network transforms the input impedance to 50 Ω at the generator side, the output matching network transforms the 50 Ω load to the optimal simulated class E output load impedance $\underline{Z_L}$.

III. SIMULATION AND MEASUREMENT RESULTS

The proposed class E PA was fabricated on a FR 4 substrate with a relative dielectric constant of 4.3 and thickness of 0.8 mm. The ADS schematic of the proposed PA is illustrated in Fig. 2. The circuit consists of gate and drain supply circuits, which provide proper bias voltages to the active device; an input matching network connected to input sinusoidal driving signal; LDMOS transistor operated as a switch; class E load network which enables class E operation and tunes the output to the operating frequency and output matching network, which transforms the 50 Ω load impedance to the optimal impedance determined by load-pull simulation. After optimization, the designed class E PA can provide the maximum PAE of 93.45% and the maximum output power of 45.31 dBm when the input power was 22 dBm. Simulated drain voltage and drain current waveforms at 13.56 MHz are presented in Fig. 3. The peak drain voltage is 109 V and the peak drain current is 3.2 A and the overlapping areas between two wave forms are small, which means that low power dissipation on the transistor and thus, high efficiency can be achieved. Fig. 4 shows the fabricated prototype of the proposed class E PA. During the fabrication of the PA, the maximum PAE and the output power can be optimized by tuning each inductor at the output network. The fabricated inductor was calculated, fabricated and measured by Agilent A4285A LRC meter to confirm the calculation. Most inductors at the output side were designed by using the concept of air core inductor, since the value of each inductor is quite low.

The measurement results in terms of the output power, power gain and PAE versus input power compared with the simulation results are illustrated in Fig. 5, Fig. 6 and Fig. 7, respectively. Fig. 5 shows the output power over the input power, the proposed class E PA provides the output up to 45 dBm. Fig. 6 shows that the maximum power gain of 30.29 dB occurred at input power of 11 dBm, then started to compressed when the input power exceeded this level.

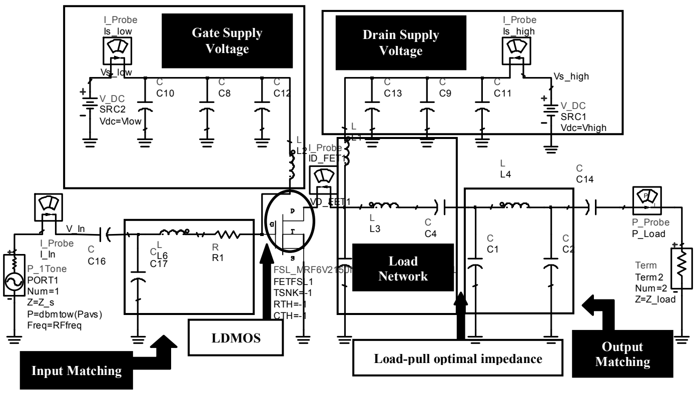

Fig. 2. ADS schematic of proposed class E power amplifier.

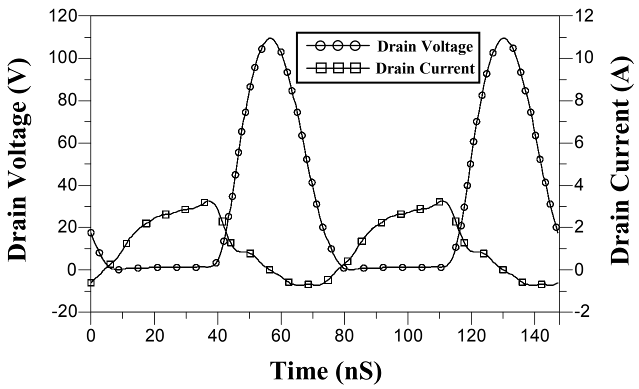

Fig. 3. Simulated drain voltage and drain current of the LDMOS transistor at the output power of 45.31 dBm with PAE 93.45%. Drain supply voltage, gate supply voltage, and input power are 32 V, 2.2 V and 22 dBm, respectively.

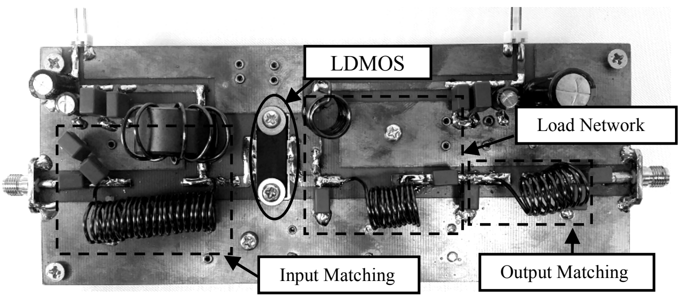

Fig. 4. Fabricated 13.56 MHz class E power amplifier with parallel load circuit.

In Fig. 7, the peak PAE reached the maximum value of 94.6% at the input power of 23 dBm whereas power gain was 21.92 dB and output power of 44.92 dBm was provided as can be observed in Fig. 5 and Fig. 6. The measured waveforms of gate-source and drain-source voltages using Agilent DSO6054A oscilloscope is presented in Fig. 8. During the "on" state, the value of gate voltage is positive whereas the drain voltage is close to zero and vice-versa during the "off" state showing that switched-mode operation of the amplifier is provided. Finally, this work is compared with some previous works concerning class E PA design with frequencies of operation in the ISM bands around 13.56 MHz and 27.12 MHz. Table I shows PAE, output power and operating frequency of 13.56 MHz and 27.12 MHz class E Pas including the one presented in this work. More information are available in [9].

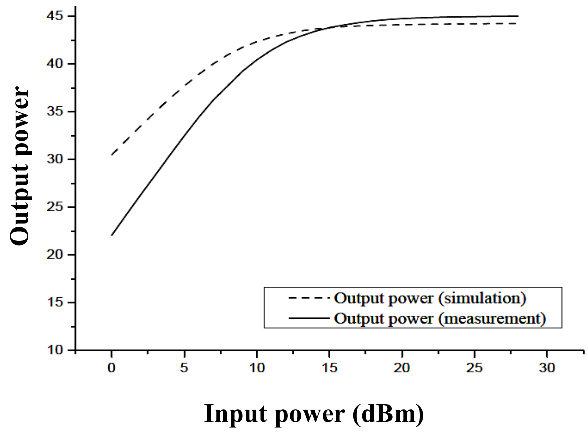

Fig. 5. Simulation and measurement results of output power versus input power at 13.56 MHz.

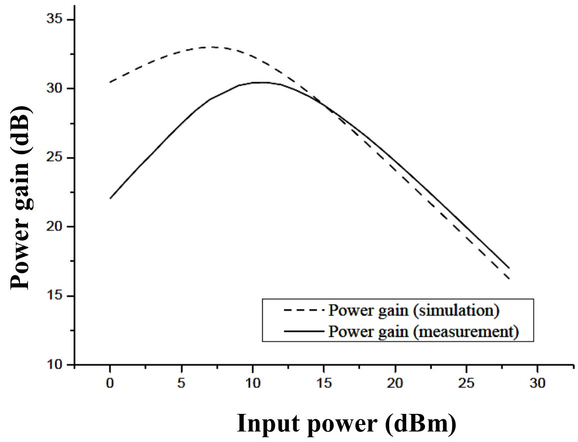

Fig. 6. Simulation and measurement results of power gain versus input power at 13.56 MHz.

CONCLUSION

This work presents design and implementation of high efficiency 13.56 MHz, class E PA with parallel load circuit for wireless power transmission and heating applications. The proposed PA used LDMOS as the power device and load-pull technique to determine the optimum load impedance. The fabricated class E PA provides a peak PAE of 94.6%, power gain of 21.92 dB at the output power of 44.92 dBm (31 W). This work has been compared with other class E PAs reported previously in the literature.

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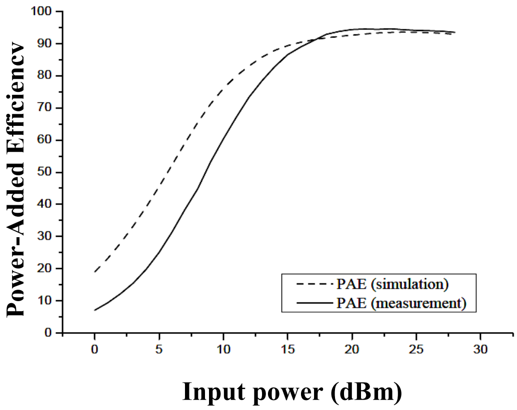

Fig. 7. Simulation and measurement results of PAE versus input power at 13.56 MHz.

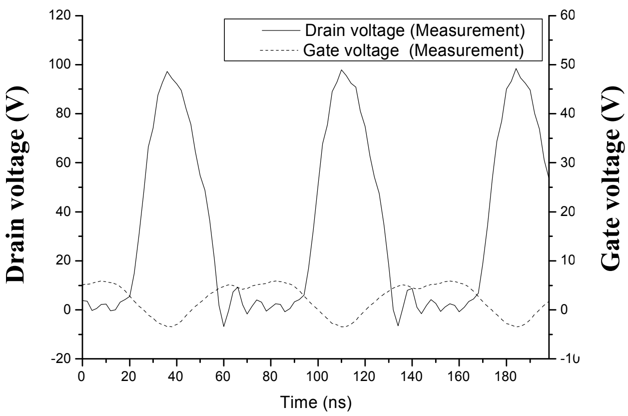

Fig. 8. Measured waveforms of gate source and drain source voltages.

TABLE I. CLASS E POWER AMPLIFIER DESIGN COMPARISON

Ref.	Power-Added Efficiency (%)	Output power (dBm)	Frequency (MHz)
This work	**94.6**	**44.92**	**13.56**
[3]	93.6	44.08	13.56
[10]	91	54.77	13.56
[11]	90	53	18
[12]	89.6	41.4	27.1
[13]	85.5	48	14
[14]	83	57	27.12
[15]	82	30	13.56

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