Character Construction

Characters are not constructed on the face of a CRT by whim or desire alone. Character construction involves a combination of beam blanking (or unblanking) and beam deflection. The characters in the EC/130 are constructed on a seven bar figure 8 pattern. In order to identify the bars, or segments, they are numbered in order of construction. Thus, segment 0 is constructed before segment 1, and segment 7 is constructed before segment 12, etc. Figure 1 shows the basic figure 8 digit and the numbers assigned to each segment. Note that there are more segments shown than are strictly needed

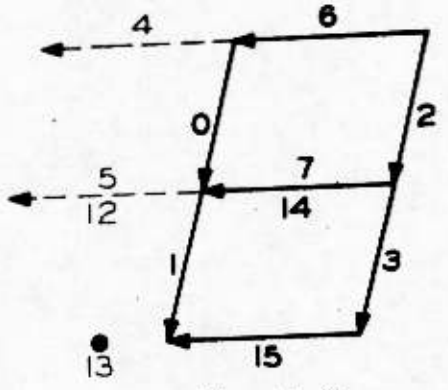


Figure 1

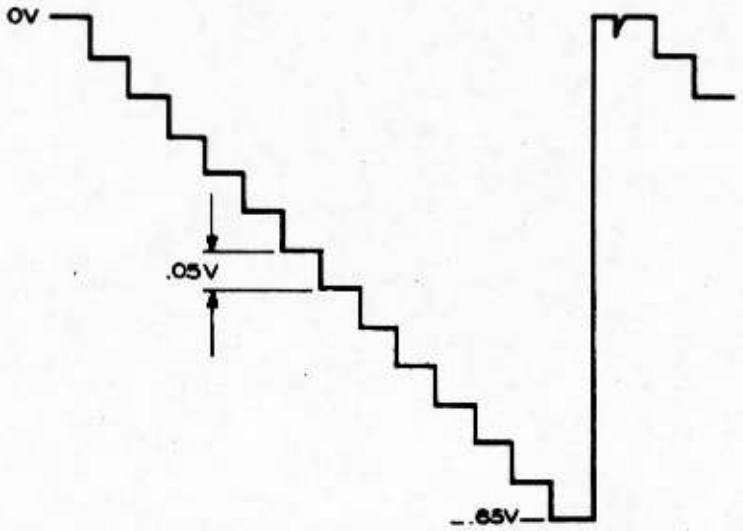
to construct a figure 8. Segment 13 is used to construct the decimal point. Segment 14, if it were actually drawn on the scope, would be in the same place as segment 7, but if it were drawn in addition to segment 7, then that segment would be brighter than the rest of the segments, so segment 14 isn't drawn in the construction of a digit, but it is drawn for a negative sign. Segments 4, 5, and 12, shown by dotted lines are not drawn on the CRT face at all. They are there because

of certain timing situations, and it is easier to leave the CRT blanked than to go to the trouble of eliminating them.

So far only the figure 8 has been discussed, but by blanking one or more of the segments, other digits can be constructed. If segment 7 is blanked, a 0 is constructed. Blanking segments 0 and 3 creates a digit 2, and so on. It should; however, be realized and remembered that the beam is ALWAYS deflected as shown in figure 1. BLANKING determines what digit is displayed.

THE HORIZONTAL STAIRCASE GENERATOR

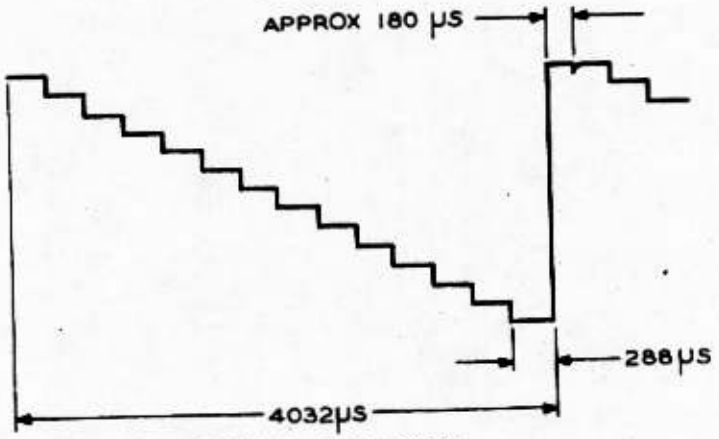
This generator produces the waveform which positions the 13 digits and the sign on the scope horizontally. The display circuitry is so arranged that 0 volts output from the staircase generator will position the digit in the extreme right position. The greater the amplitude of the output of the staircase generator, the farther from the right hand position the digit will be displaced. Given that, 1) for the sign position (C1), the amplitude of the staircase output is 0 volts, and that, 2) for the least significant digit (C2) the amplitude is .05V, and that, 3) the digits are equidistant apart, then the output signal of the staircase has 14 steps or voltage levels with the amplitude of the first step (C1) at 0 volts, the amplitude of the second step at -.05 volts, and increasing by increments of .05 volts until the final step (C14) which is at -.65 volts. The actual waveform of the output signal with respect to voltage levels is thusly:



HORIZONTAL STAIRCASE WAVEFORM

Each step is produced by charging a capacitor to -.05 volts and then not discharging it. The voltage across the capacitor is coupled to the output circuitry by an emitter follower with a very high input impedence to avoid loading the circuit and thereby create sagging within each step. After the capacitor has been charged to the desired level for C14 (about -.65 volts) the staircase circuit must be reset. This is done by shorting the capacitor to ground by turning on a transistor that is connected across the capacitor.

The horizontal staircase generator produces the voltage levels that ultimately position the 13 digits and the sign on the display tube. To do this requires 14 separate, distinct levels. Since each character (digit) time is 288 u sec, it follows that each voltage level is 288 u sec long. If there are 14 steps of 288 u sec each, then the overall staircase waveform is 14 x 288 x 10^{-6} sec or about 4.03 milliseconds long. The waveform, with respect to time, will look something like this:



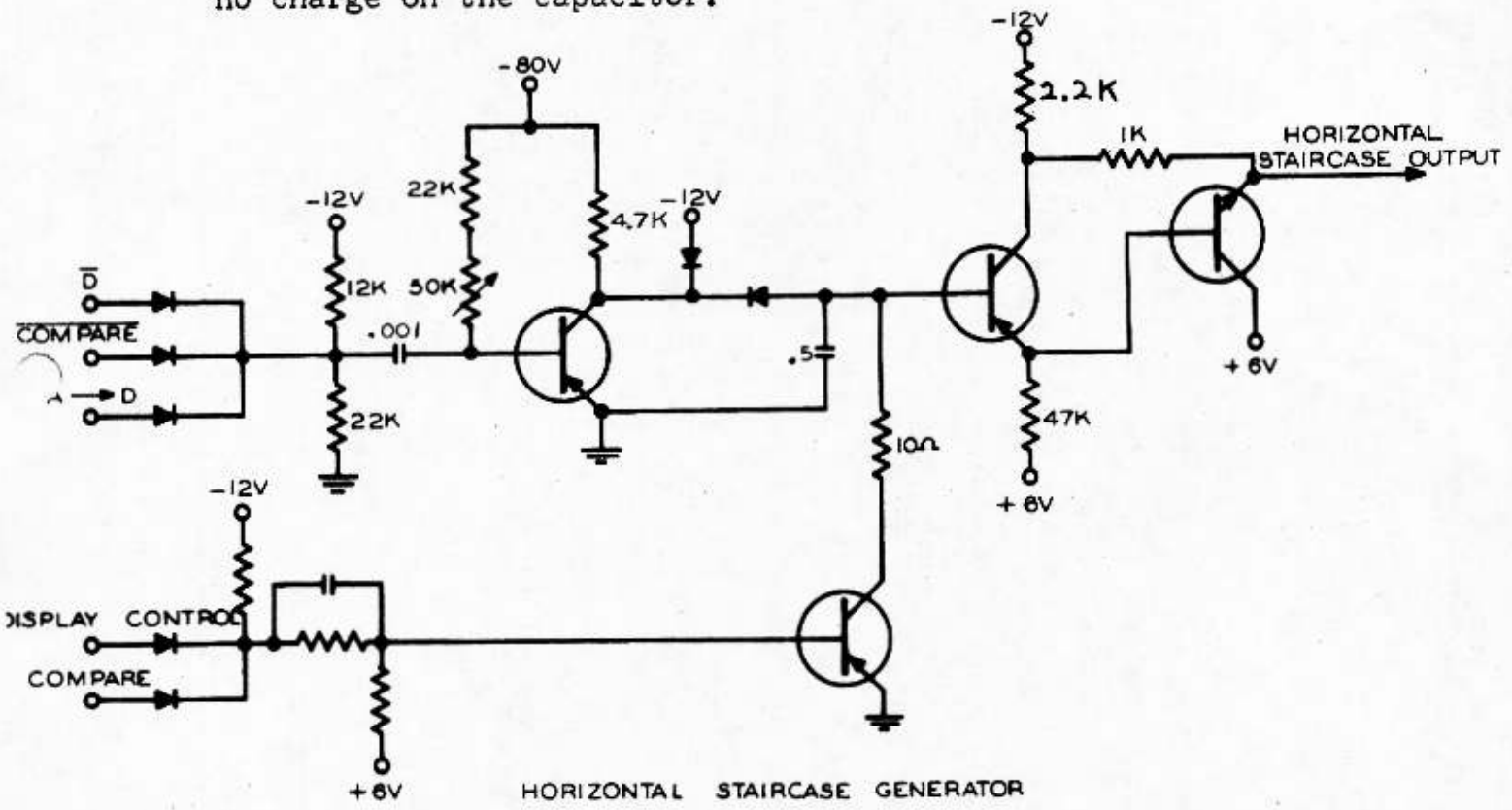
HORIZONTAL STAIRCASE WAVEFORM

The difference in potential between any two adjoining steps is proportional to the spacing between the two characters (or

digits) assigned to those two voltage levels.

This staircase waveform is produced by charging a capacitor and not allowing it to discharge. The overall circuit is pretty complex, but a component by component analysis renders it quite easily understandable. The input to the staircase generator is via a three input positive OR gate. The output of the OR gate is a 24 u sec negative pulse every 288 u sec. The output of the OR gate is connected to a voltage divider consisting of a 12K and a 22K. The 12K is connected to -12V; the 22K is connected to ground. When any input to the OR gate is 0 volts, that diode conducts and clamps the point between the two resistors to 0 volts. When all three inputs are at -12 volts, the diodes are back-biased, and the voltage divider output is -7.75 volts. All three inputs will be at -12 volts for 24 u sec. Then, one input will return to 0 volts, and the output of the voltage divider circuit goes to 0 volts. The output of the voltage divider is connected to a .001 u f capacitor. The other side of the capacitor is connected to the base of a transistor. Also connected to the base of the transistor is a 50K potientiometer and a 22K in series to -80 volts. When the output of the OR gate and voltage divider combination is 0 volts, the left side of the capacitor is tied to this 0 volts. The base-emitter junction of the transistor is forward biased because the emitter is grounded, and the base is connected to -80 volts through the 50K pot and the 22K. The first consideration of this circuit will be with the 50K pot adjusted for minimum resistance. Because the emitter-base junction is forward biased, the base current will be $-80/22 \times 10^3 = (-80/22) \times 10^{-3}$ which equals 3.6 milliamps. This is sufficient to clamp the right side of

the 100P capacitor connected to this base to 0 volts (actually about -.2 volts, negligible here). Since both sides of the capacitor are at 0 volts, the capacitor has no charge. The transistor is on and in saturation. Its collector is at 0 volts. When the output of the OR gate voltage divider combination goes to -7.75 volts the left side of the capacitor also goes from 0 volts to -7.75 volts. Therefore, the right side of the capacitor tries to go to -7.75 volts because there was no charge on the capacitor.



HORIZONTAL STAIRCASE GENERATOR

This increases the emitter-base current of the transistor and tries to turn the transistor on harder. Alas, it's already in saturation. The transistor stays in saturation, and the .001 capacitor is charged with -7.75 volts on its left side, and 0 volts on its right side. During the time immediately preceeding the change . . . . . .

of the input signal from 0 volts to -7.75 volts, the transistor was in saturation, and its collector was clamped to 0 volts. When the input changed from 0 volts to -7.75 volts the transistor stayed in saturation. Now, at the end of the 24 u sec that the input signal is at -7.75 volts, the transistor is STILL in saturation, and the .001 uf capacitor is charged to -7.75 volts. Now, after this 21 u sec one of the inputs to the OR gate goes to 0 volts. This puts 0 volts on the left side of the capacitor. This is a 7.75 volt change in a positive direction. The right side of the capacitor also must go 7.75 volts in a positive direction. The right side of the capacitor was at 0 volts. 0 volts +7.75 volts equals +7.75 volts. This positive voltage back biases the emitter-base junction of the transistor and turns it off. The collector does NOT rise to -80 volts. Neither will the base stay at plus 7.75 volts. The capacitor begins to charge toward -80 volts through the 50K pot and the 22K. As soon as the base voltage (base voltage equals charge on the capacitor) goes more negative than 0 volts, the transistor will turn on, and its collector will go to 0 volts. The length of time the transistor stays OFF is determined by the length of time it takes the.001u capacitor to charge from plus 7.75 volts to -.2 volts. This length of time is determined by the R.C. time constant of the capacitor and its charge resistance (the 50K pot plus the 22K, but the 50K pot has been adjusted to 0 ohms). The formula for finding the length of time (T) that the transistor will be off may be derived from the familiar formula below.

$$Ei = Ea(1-e^{\frac{-T}{RC}})$$

$$(1-e^{\frac{-T}{RC}}) = Ei/Ea$$

$$-e^{\frac{-T}{RC}} = (Ei/Ea)-1$$

$$e^{\frac{-T}{RC}} = 1 - (Ei/Ea)$$

$$-T/RC = \log_e (1-Ei/Ea)$$

$$-T = \log_e (1-Ei/Ea) \times RC$$

Given That:

RC = 22K x 100P = 22 u sec

Ei = 7.95 volts *

Ea = 87.75 volts**

$$-T = \log_e (1-Ei/Ea) \times RC$$

$$= \log_e (1-7.95/87.75) \times 22 \times 10^{-6}$$

$$= \log_e (1-.0907) \times 22 \times 10^{-6}$$

$$-T = \log_e (.9093) \times 22 \times 10^{-6}$$

$$= -.0952 \times 22 \times 10^{-6}$$

$$-T = -2.09 \text{ u sec}$$

$$T = 2.09 \text{ u sec}$$

if the 50K pot is set to 0 ohms. If it is set for 50 K ohms then

* The transistor will turn on at -.2 volts on the base. Plus 7.75 volts, now exists there. Plus 7.75-(-.2) equals plus 7.95 volts.

** Although -80 volts is applied, the capacitor is charged to plus 7.75 volts, so must be considered a source also. These sources subtract.

$$-T = -.0952 \times 72 \times 10^{-6}$$

$$T = 6.85 \text{ u sec}$$

Hence, the limits of the transistor off time are 2.09 u sec and 6.85 u sec. The collector of the transistor is connected to -80 volts through a 4.7K resistor. The cathodes of two diodes are also connected to the collector of the transistor. One diode goes to -12 volts to clamp the collector to -12 volts. This diode is back biased as long as the collector voltage is less than -12 volts, but if the collector voltage starts to exceed -12 volts, the diode becomes forward biased and clamps the collector to -12 volts. This is to protect the transistor which is good for only 30 volts. The other diode is connected to a .5u capacitor. The other side of the capacitor is connected directly to ground.

Assuming the capacitor to be completely discharged, the capacitor will not charge as long as the staircase step control transistor is on. When the transistor turns off, the u5 capacitor begins to charge from ground, up through the capacitor, through the diode, which is forward biased, through the 4.7K to -80 volts. Note that the capacitor sees -80 volts as the charge potential, not -12 volts. The -12 volts is connected to the collector through the diode which is normally back biased. The capacitor will charge as long as the staircase control transistor remains off; therefore, by varying the off time of the transistor, the charge time of the capacitor is varied. The longer the transistor charges, the greater will be the voltage across its plates when it stops charging.

The RC time constant of the charge circuit is $.5 \times 10^{-6} \times 4.7 \times 10^{3} = 2.35$ milliseconds. If the staircase control transistor

is off for the minimum time of 2.1 u sec then the amount of charge on the u5 capacitor after 2.1 u sec of charging is found by the now familiar formula.

$$Ei = Ea(1-e^{\frac{-T}{RC}})$$

$$Ei = -80(1-e^{\frac{-2.1}{2350}})$$

$$= -80(1-e^{-.00089})$$

$$= -80(1-.9996)$$

$$= -80(.00037)$$

$$= -.03 \text{ volts}$$

Given that:

Ei = Instantaneous voltage

Ea = -80 volts

e = epsilon or 2.72

T = 2.1 u sec

RC = 2.35 milliseconds or 2350 u sec

Ei = -.03V with the staircase control transistor off the minimum time of 2.1 u sec. If the transistor is off the maximum time of 6.85 u sec then

$$Ei = -80(1-e^{\frac{-6.85}{2350}})$$

$$= -80(1-e^{-.00292})$$

$$= -80(1-.9971)$$

$$= -80(.0029)$$

$$= -.233 \text{ volts}$$

Ei = -.233 volts with the staircase control transistor set for maximum off time (6.85 u sec). Thus, the limits of the change in charge across the capacitor for a charge period are -.03 volts and - .233 volts.

If it is assumed that the off time of the staircase control transistor (or the charge time of the capacitor) is set for minimum for purposes of illustration, and the capacitor is

completely discharged, then during the first charge period) the capacitor will charge to -.03 volts. When the transistor turns back on, the charge time of the capacitor will be terminated as explained, but the capacitor will not discharge. The diode in the charge path is now insufficiently forward biased because about -.1 volt (emitter-collector voltage drop) is on the cathode and -.03 volts on the anode. This is well under the breakover voltage of the diode, hence it will not conduct. The capacitor is connected to the collector of the reset transistor through a 10 ohm resistor, but this transistor is biased off at this time. The capacitor is also connected to the base of an emitter follower, but the emitter resistor is 47K, so the input impedence to the emitter follower stage is Beta times 47K. If the Beta of the stage is 40 then the input impedence is 47K x 40 which equals 1.9 megohms, and the time constant of this discharge path is $1.9 \times 10^{6} \times .5 \times 10^{-6}$ or 950 milliseconds. Since there are 288 u sec between capacitor charge times, the capacitor can discharge for 288 u sec after each charge. 288 u sec is .0003 times one time constant. The amount of charge the capacitor loses during .0003 time constants can be considered negligible in this circuit. Suffice it to say that the capacitor does not discharge during the 288 u sec the staircase control transistor is on. When the transistor turns off once again for 2.1 u sec, the capacitor will once again charge to -.03 volts, but in addition to the -.03 volts that it didn't lose during the 288 u sec on time of the transistor. -.03 volts plus -.03 volts equals -.06 volts. This, then, is the charge across the capacitor after the second charge period. The charges are cumulative. So, after 13 charge periods, the charge across

the capacitor will be 13 times -.03 volts or -.39 volts. The capacitor is charged 13 times to establish 14 levels because 0 volts is considered the first level. After the 13th charge period, the capacitor maintains its -.39 volt charge for 288 u sec. At the end of the 288 u sec, the staircase reset transistor turns on. This shorts our the .5u capacitor through a 10 ohm resistor to reset the circuit and bring the charge of the capacitor back to 0 volts. The 10 ohm resistor is to limit the reset transistor collector current to a safe value.

The emitter follower previously discussed as a very high impedence discharge path of the capacitor during operation is the means of picking off the signal from the capacitor to apply it to the horizontal deflection amplifier.

This circuit has two purposes. 1) It must provide a high degree of isolation. 2) It must provide a high degree of current amplification. These two emitter follower stages are D.C. coupled to reduce unnecessary signal loss. For this reason, an NPN transistor is used in the second stage. This transistor also provides the current amplification necessary to drive the output load. The first stage is a transistor with a 2.2K from the collector to -12 volts and a 47K from the emitter to +6 volts. The output is taken off the emitter. For practical analysis, the inherent loss in the emitter follower will be considered negligible. Therefore, if the signal at the base is 0 volts, the signal at the emitter is also 0 volts. This means that there is 6 volts dropped across the 47K; hence the current through the first emitter follower stage is .1275 milliamps. Then the collector voltage should be $(.1275 \times 10^{-3} \times 2.2 \times 10^{3}) - 12 = (.28 \text{ volts}) - 12 \text{ volts}$ or

-11.72 volts. However, only -3.65 volts is actually measured on the collector of the first emitter follower. The reason will become apparent shortly. 0 volts on the emitter of the first stage means 0 volts on the base of the second stage. It is an emitter follower, too, so there will be 0 volts on the emitter of that transistor also. The output is taken at this point, so with 0 volts in, and 0 volts out, all is well. Notice how the emitter of the NPN transistor is returned to -12 volts. Of what resistors is the second stage emitter resistance composed? It is composed of a 1K and the SAME 2K2 that is the collector resistor of the first stage. If 3K2 is the emitter resistance for the second stage, and one side of the voltage divider (that is, the 2K2 and the 1K in series) is connected to -12 volts, and the other side is 0 volts (the output voltage is 0 volts), then the voltage dropped across the 2K2 resistor is $12 \times 2.2 \times 10^3$ - 8.35 volts. The voltage on the collector of the first stage, then is 8.35-12 or -3.65 volts (not -11.72 volts as would be supposed by considering only the collector current of the first stage). The purpose of this is to reduce the collector-base leakage current which might affect the voltage level on the u5 capacitor. (This leakage current would cause the voltage on the capacitor to increase in a negative direction, not sag as might at first be supposed.) All in all, the horizontal staircase generator is a well thought out, stable circuit which should give little trouble in the field, and should be easy to trouble-shoot when trouble does develop.

Display Matrix

The display matrix looks forboding and complicated, but matrix theory is quite easily understood. Consider Figure 1; obviously this is nothing more than three negative AND gates which feed a negative OR gate. Look at the logic of it all! If A and B and C are present, that will yield X. If D and E and F are present, that will yield Y. If G and H and J are present that will yield Z.

If X or Y or Z are present, So will be produced.

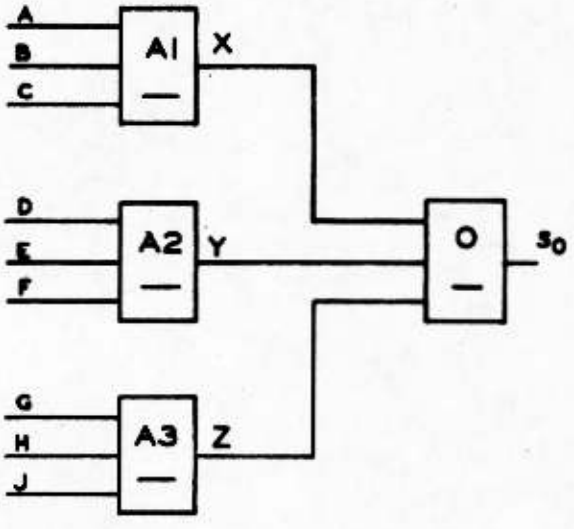


Figure 1

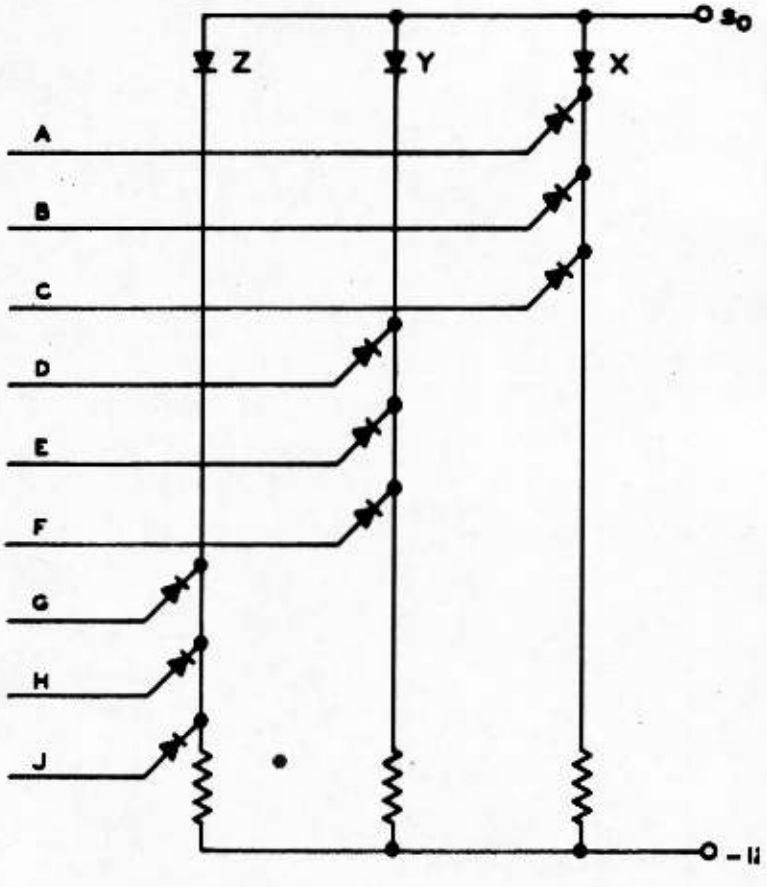


Figure 2

To get So, all the signals at the first AND gate must be

2

present, or all the signals at the second AND gate, or all the signals at the third AND gate. That is pretty easy to understand. There is nothing complex about it at all. Yet Figure 1 is a diode matrix. Figure 2 shows it schematically. Assume that So is the blanking signal, and that the CRT will be blanked anytime So is low. Then, the CRT will be blanked when A and B and C, or D and E and F, or G and H and J are low.

To take a purely hypothetical case, suppose that A and B go low only when it is desired to display a zero. Suppose further that C goes low only when segment 7 is being drawn on the CRT. Then, X will go low when it is desired to display a zero and segment 7 is being drawn on the CRT. When X goes low, So goes low and segment 7 is blanked.

This is, of course, only an example, but examine figure 3 for a moment. This is a portion of the actual display matrix. Only one AND gate is shown for simplicity. The only time D1 and D5 are both negative is when there is a digit 0 in the D counter to be displayed. The only time $\overline{R4}$ and $\overline{D}$ are both negative is when segment 7 is being displayed. When all four of these signals are negative, segment 7 will be blanked.

The rest of the display matrix works the same way as described above except that there are different inputs to blank different segments.

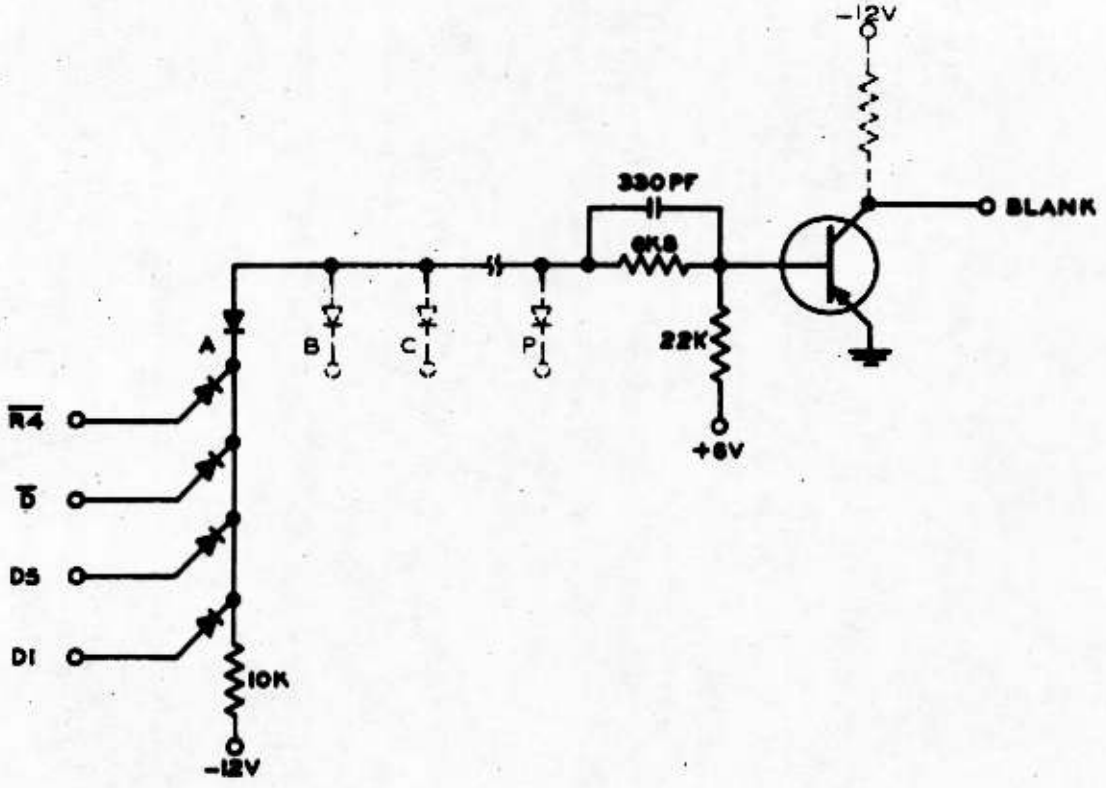
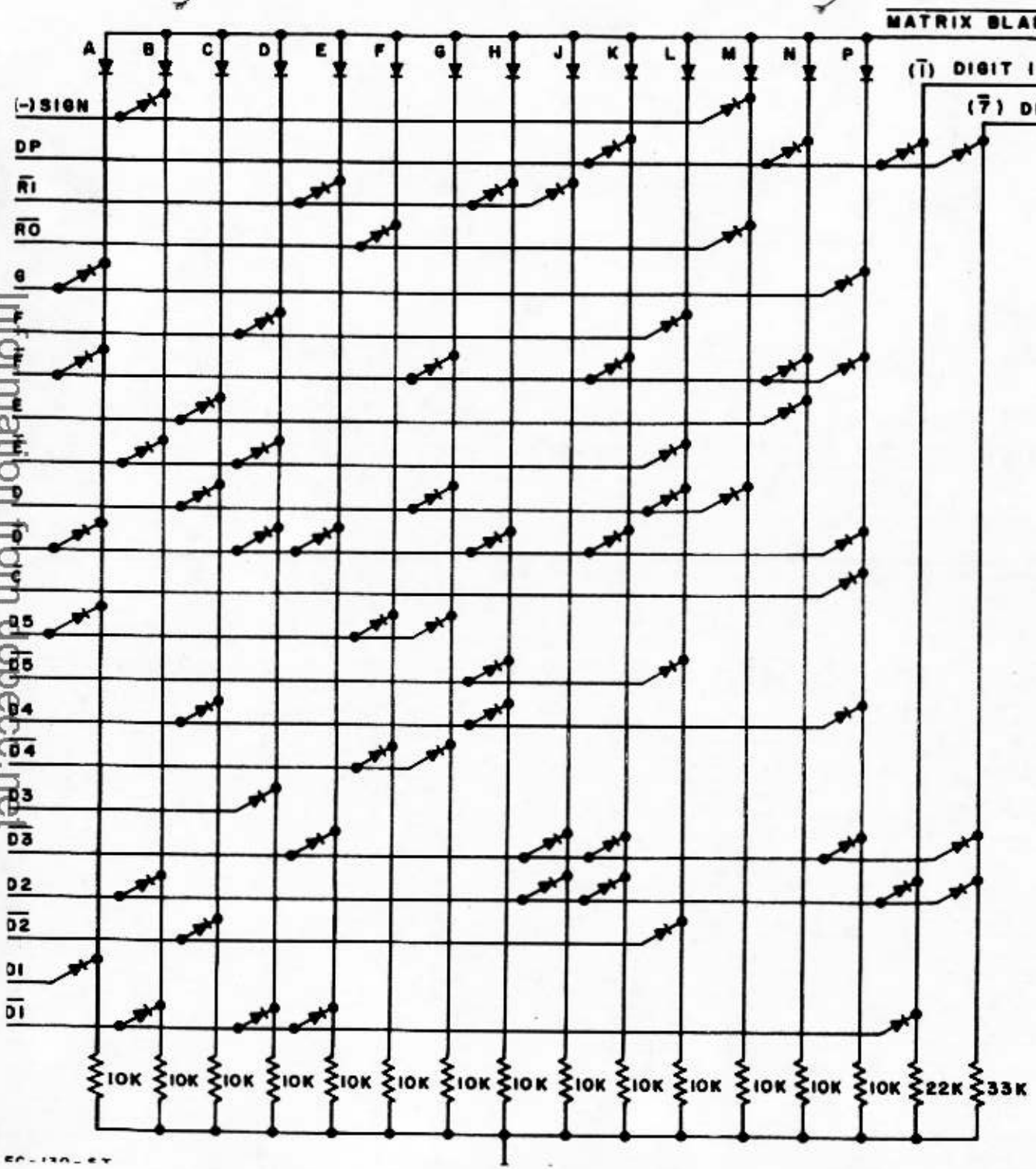
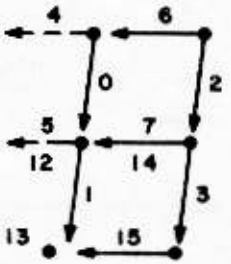


Figure 3



DIGIT CONST.



SEGMENT TRUTH TABLE

	TIMING FF'S				
SEG	D	E	F	G	REG
0	0	0	0	0	R1
1	1	0	0	0	"
2	0	1	0	0	R2
3	1	1	0	0	"
4	0	0	1	0	R3
5	1	0	1	0	"
6	0	1	1	0	R4
7	1	1	1	0	"
12	0	0	1	1	R5
13	1	0	1	1	"
14	0	1	1	1	RMD
15	1	1	1	1	"

MATRIX FUNCTION

BUS	BLOCKS SEG	AFFECTS DIGIT
A	7	0
B	2,3,6,7,14,15	1
C	0	2,3
D	3	1,2
E	1	3,4,5
F	14,15	4
G	6	4
H	1	9
J	0,1	7
K	7,15	7
L	2	5,6
M	14	-SIGN
N	4,5,12,13	D.P.
P	7	MOD. 3

Compare

The purpose of the signal, COMPARE, is to indicate that the information that the display circuit is looking for COMPARES with the information that is in the A Counter. The signal COMPARE is high for one R time ie 48us. By definition the signal $\overline{\text{COMPARE}}$ will be low at the same time. In order to use this sought after information that is in the A Counter the signal $\overline{\text{COMPARE}}$ is used to generate an A $\longrightarrow$ D shift at B15. While the data is in the D Counter it is decoded by the display matrix and the number is displayed on the C.R.T. The information remains in the D Counter for 288us.

Together with other signals the signals COMPARE and $\overline{\text{COMPARE}}$ also control the Display Control Flip-Flop, and the horizontal staircase generator.

As an example, follow the gating for displaying register one. Refer to the list of, Information To Be Displayed, and note that the two timing signals, M and N are low for this condition; therefore, $\overline{M}$ and $\overline{N}$ will be high for this example and their corresponding gates will be blocked.

The signal $\overline{G}$ will be low for each Rs and Rmd, and the signal $\overline{\text{COMPARE}}$ will be high.

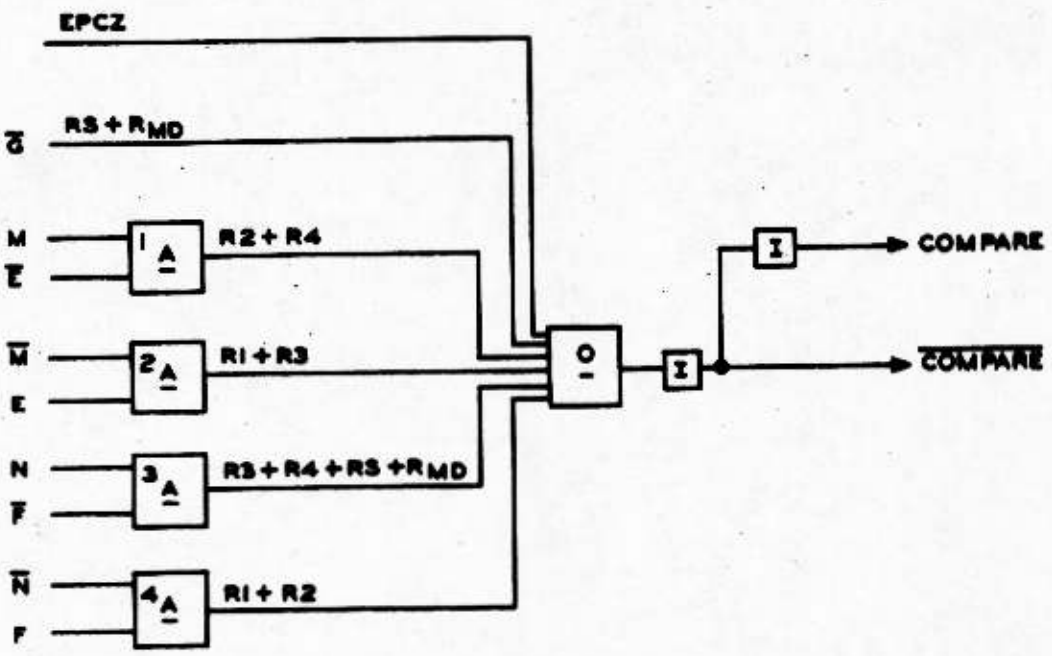
AND gate (1) will have a negative output each time the signal $\overline{E}$ is negative. Referring to the Information Available List shows that $\overline{E}$ goes negative each R2 and R4 time; consequently, the signal $\overline{\text{COMPARE}}$ will go high each R2 and R4 time.

Similarly, AND gate (3) will make $\overline{\text{COMPARE}}$ high each R3, R4, RS and Rmd times. The functions of this gate and the signal $\overline{G}$ overlap for RS and Rmd but this is of no consequence.

The combined inputs to the Negative OR cause the signal $\overline{\text{COMPARE}}$ to be high at every R time Except R1, which is the condition necessary to display register one.

The same technique can be used to develop COMPARE for R2, R3 and R4.

Development of the Compare Signal



Information to be Displayed	Information Available
M & N low for R1	E low during R1 & R3
$\overline{M}$ & N low for R2	$\overline{E}$ low during R2 & R4
M & $\overline{N}$ low for R3	$\overline{F}$ low during R3, R4, RS, Rmd
$\overline{M}$ & $\overline{N}$ low for R4	F low during R1 & R2
	$\overline{G}$ low during RS & Rmd

By definition, any negative input to the Negative OR gate will make $\overline{\text{COMPARE}}$ high which indicates NOT COMPARE. It then follows that any time that there is no negative input to the OR gate the signal $\overline{\text{COMPARE}}$ is low and COMPARE is high. This indicates that the information to be displayed compares with the information available in the "A" counter.