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# A Five Stage Chopper Stabilized Instrumentation Amplifier Using Feedforward Compensation

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## Abstract

A programmable gain chopper stabilized instrumentation amplifier is presented. It uses a fifth order amplifier architecture with simulated open loop gain of 200dB. It is the first reported silicon implementation of an amplifier using multipath feedforward compensation. The instrumentation amplifier achieves noise density of 7nV/sqrt(Hz) and THD of -110dB with 14mW from a single 5V supply. It is implemented in 0.6μm CMOS and has an active area of $4mm^{2}$.

## Introduction

To minimize power in a low noise, low distortion amplifier it is necessary to examine fundamental design methodologies and trade-offs. Thermal noise in the input stage is fundamentally linked to bias current requirements. All other stages are not noise-relevant and can theoretically be operated at low power. However, compensation schemes such as Miller Compensation or Nested Miller Compensation require significant transconductance in the output stage which can result in increased power consumption.

Moreover, it is desirable to use a class AB output stage to minimize quiescent power, but the nonlinear transfer function of such a stage can produce distortion components if open loop gain is insufficient.

Traditional single dominant pole operational amplifiers have a fixed relation between unity gain bandwidth and gain-bandwidth product in the band given by the -20dB/dec roll-off of the gain vs. frequency. A given open loop gain requirement (150dB as derived from 30dB of closed loop gain plus 120dB to guarantee good THD with large nonlinearity in the output stage) over a certain signal band (800Hz) will lead to enormous or impossible unity gain bandwidth values (24 GHz). Single dominant pole compensation is used in almost all contemporary amplifiers.

## Amplifier Architecture

Multipath feedforward compensation [1] allows high loop gain in the signal band without requiring a large unity-gain bandwidth. Such a conditionally stable circuit can have a large drop in loop gain between the signal band and the unity-gain crossover. The phase lag dips below 180 degrees, but returns to less than 120 degrees at unity gain crossover. A Bode plot of the open loop transfer function comparing the unity gain requirement for a conditionally stable 5 stage amplifier compared with a single integrator model is shown in figure 1. It is obvious that the 5 stage amp achieves a given gain requirement in the band with significantly lower unity gain bandwidth, thus allowing the use of low power circuitry throughout the opamp. The Bode plot shows the DC gain of the amplifier as 200dB. Parasitic effects will likely limit the actual DC gain.

No silicon implementation of an amplifier based on multipath feedforward compensation have been reported. The architecture to achieve this transfer function is shown in figure 2. Five integrators are connected in a cascade. At low frequencies, in the signal band, all integrators are contributing to the open loop gain. In this band the phase lag may be as much as 450 degrees. In the transition region, the integrators get bypassed one after another, thus rolling back the phase lag to smaller values. At unity gain only the widest bandwidth integrator (I5) is in the path and the phase lag is below 180 degrees, thus satisfying the Nyquist stability criterion.

The widest bandwidth integrator (I5) has 5MHz bandwidth. The second widest integrator (I2) has 100kHz bandwidth. The input stage (I1) has 20kHz bandwidth, I3 has 30kHz, I4 has 60kHz.


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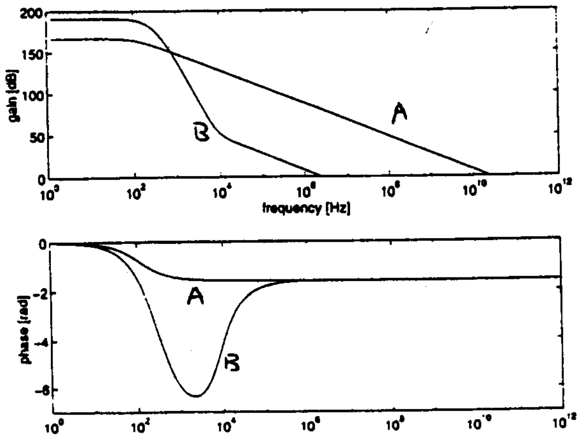


Fig 1: Open loop transfer function: comparison of single integrator (A) to 5 stage feedforward compensated amplifier (B)

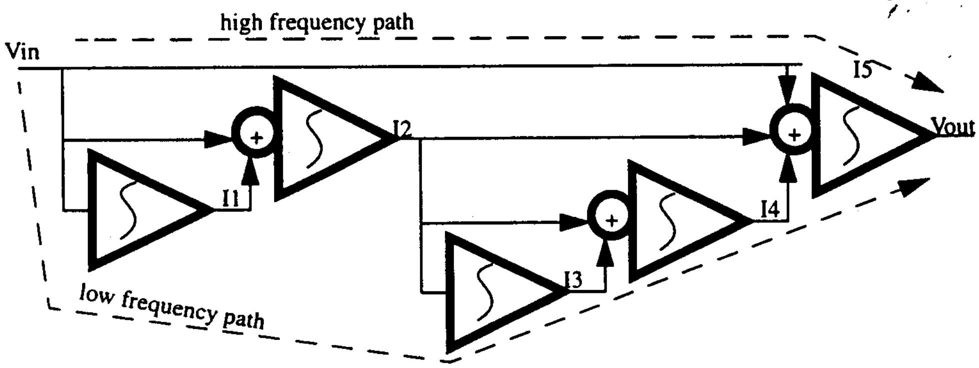


Fig 2: Architecture of amplifier: cascade of 5 integrators with bypass paths around low bandwidth integrators.

### Large Signal Stability Considerations

A conditionally stable amplifier does require additional consideration of start-up, large transients and saturation recovery. This is addressed in the amplifier as follows: Using differential pairs and current summation one can implement a summer that has the following characteristic of controlled saturation (fig. 3). A large signal on vin2 can not saturate the amplifier. It will only cause an offset in input vin1 in a closed loop configuration. On the other hand a large input on vin1 will always saturate the amplifier due to Itail2 < Itail1. This controlled saturation in the summing stages allows the high frequency path to not be disturbed when lower frequency integrators are saturated. If the high frequency path is saturated, it will block signal propagation from the lower bandwidth integrators.

Using this technique, all possible operating points of the circuit will satisfy the Nyquist stability criterion, leading to stable large signal settling. A large signal step response is shown in figure 4. It shows fast initial settling followed by small signal settling behavior that is slow due to low frequency pole zero doublets present in the closed loop transfer function of the amplifier.

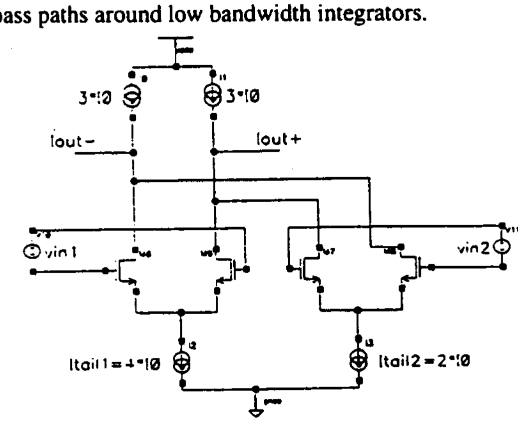


Fig 3: Summer with controlled saturation behavior

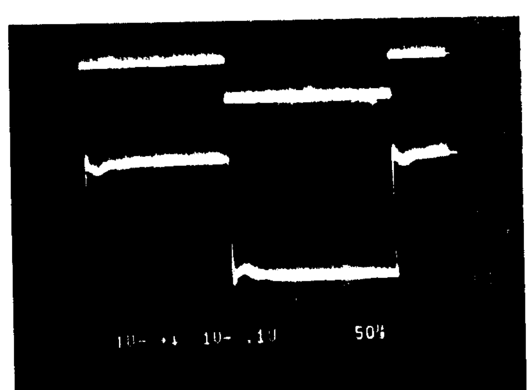

Fig 4: Large Signal Settling behavior (Gain 30dB) top: input, bottom: output. frequency:2500Hz

## Circuit Design

The input stage determines the noise and distortion performance of the opamp. 50% of the total opamp power is consumed in this stage to minimize the thermal noise. It is a single stage folded cascode design.

Chopper stabilization is used in the input stage (I1) to remove offset and 1/f noise. The chop frequency is 512kHz. This leads to a flat noise spectrum with 7 nV/sqrt(Hz) noise density from 0.1Hz to 1kHz. Since the chopped stage is in the signal path only for low frequencies up to 20kHz, filters stages at the output are used to suppress chopping artifacts. As a result there are no large chop artifacts visible in the output waveform.

The low time-constant of the input stage of about 20 kHz is realized in the following manner: Capacitor size limitations require the input stage to have 2.5 MHz bandwidth. By following this stage with a cascade of attenuators with a total attenuation of 1/128 the low time-constant can be realized without unreasonable device sizes. A circuit diagram of I1 is shown in figure 5.

All intermediate integrators have very relaxed requirements for noise or bandwidth. They are implemented as single stage transconductors with capacitive loads. Throughout the amplifier fully differential circuits are used.

The output integrator is a two stage Miller compensated class AB circuit designed for power efficiency. It is operated at low current levels because there are no stringent linearity constraints and only moderate bandwidth requirements. It is based on a design by Op't Eynde [2]. In its application the circuit drives a load consisting of 2kΩ feedback resistor and an anti-alias filter of 500 Ω, 20 nF.

This two opamp instrumentation amplifier configuration does not remove the common mode voltage. It is designed to drive a fully differential analog to digital converter that has high common mode rejection (figure 6).

## Summary of Results

| | |
|---|---|
| noise density 0.1 to 1000Hz | 7nV/sqrt(Hz) |
| THD | -110dB |
| Unity gain bandwidth | >5MHz |
| Offset voltage | <2μV |
| power consumption | 14mW |
| gain range | 0 to 30dB |
| CMRR | >120dB |
| Input range | 0.9 to 3.1V |

The measured noise and distortion spectra are shown in figures 7 and 8. A photograph of the amplifier is shown in figure 9.

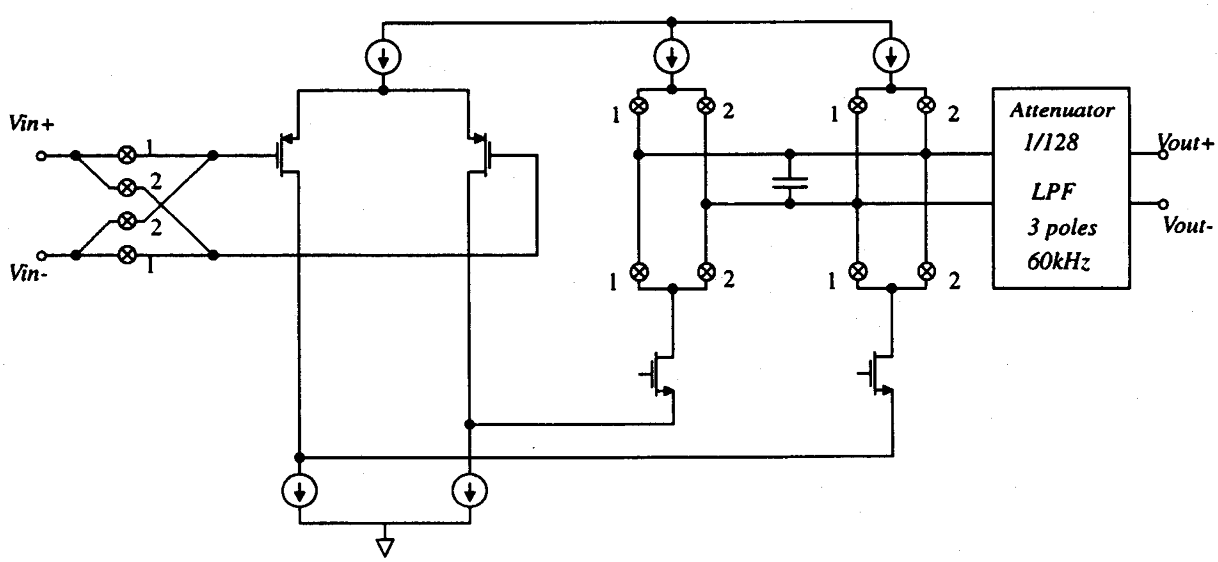


Fig 5: Circuit diagram of Input stage I1

  

## Conclusion

In this paper we have presented a five stage amplifier design using multipath feedforward compensation. The architecture allows high gain over the low frequency band of interest while using a low power class AB output stage that has a bandwidth of only 5 MHz. Chopper stabilization is employed to reduce offsets and 1/f noise. Large signal stable operation using controlled saturation of stages is demonstrated. The measured results indicates that the multipath feedforward architecture can be an effective technique in minimizing power consumption in low noise, low distortion CMOS amplifiers applications.

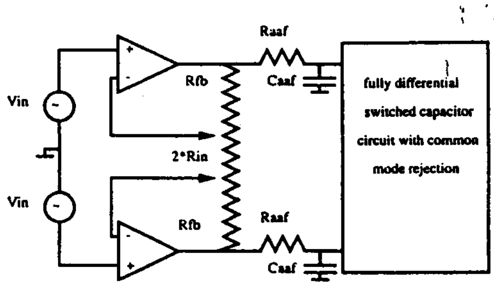


Fig 6: Application diagram of 2 opamp instrumentation amplifier

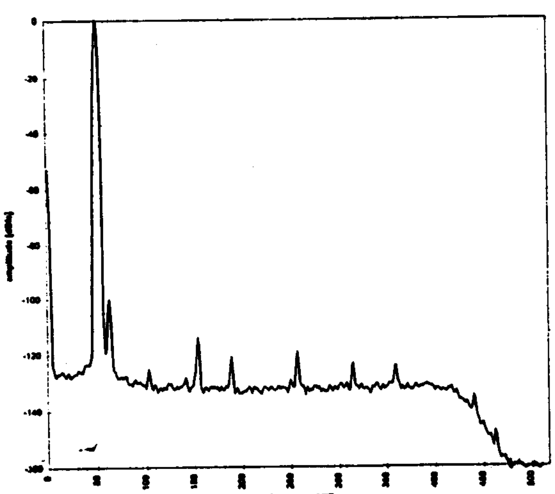

Fig 7: Output spectrum. Gain 18dB, f= 50 Hz, Vin=400mVp differential. THD=-110dB

## References

[1] R. G. H. Eschauzier, J. Huising, 'Frequency compensation techniques for low-power operational amplifiers', Kluwer Academic Publishers, Dordrecht, 1995, pp.166-173

[2] F. Op't Eynde, W. Sansen, 'Analog interfaces for digital signal processing systems' Kluwer Academic Publishers, Dordrecht, 1993, pp. 62-78

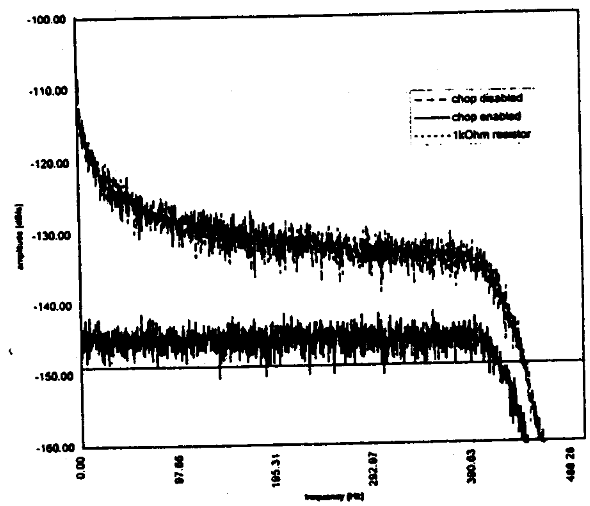


Fig. 8: Noise spectrum with and without chopping (reference line for 1kΩ equivalent resistance)

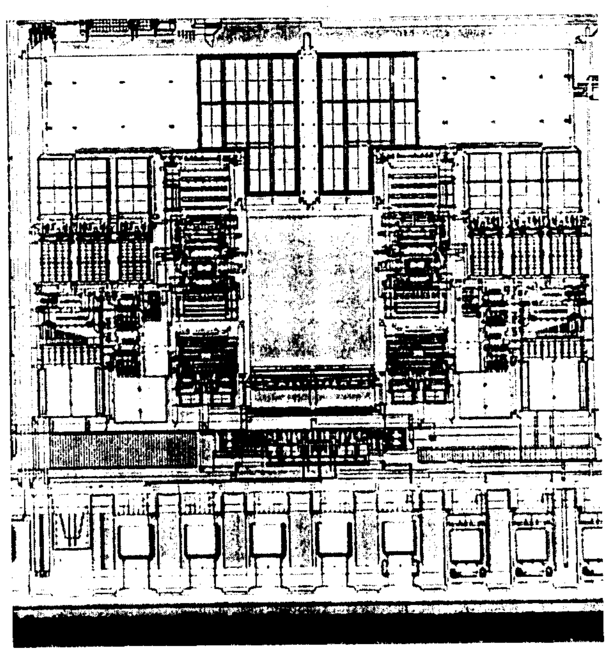

Fig 9: Photo of the instrumentation amplifier. Feedback resistor in center.