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A dedicated two layer PCB was built and assembled to test the voltage flicker noise of different chopper amplifier ICs. The chopper current noise spectrum will not be evaluated at this time. The PCB has three locations for amplifiers to be tested. Each of the three locations can support a DIP, SOIC8 or MSOP8 package. One of the three locations is wired for a dual opamp. Only one of the dual op amp channels is evaluated (pins 1, 2 and 3). The other opamp is configured for a gain of 1 and the input is grounded. Each PS input to each opamp has a 0.1ufd ceramic SMD cap and a 100ufd Aluminum Electrolytic cap to ground for bypass.

Minimizing EMI influence – reference schematic

The PCB is installed in a heavy cast bare aluminum box (no EMI Gasket). The dimensions are 220mm x 120mm x 81mm. Power comes in through two 0.05uF Bolt-in EMI filters.

Ferrite beads are used on the input and output leads to improve the performance of the feedthrough capacitors.

The output of the opamp goes to a DVM and a Digital Spectrum Analyzer (DSA). The opamp is isolated from each output port with a 1k resistor and a capacitor to ground.

The voltmeter output is filtered with a 1k MF resistor, 0.05ufd feed through cap, RF beads, 0.68ufd PP cap, and a 100 ohm resistor. The 100 ohm resistor and 0.68ufd caps filter any noise coming from the HP34420A Nano voltmeter back into the test setup. The 1k / 0.68uF filter had a 3dB corner frequency of 230 Hz to minimize chopper spikes getting to the Nano voltmeter.

The output to the DSA is filtered with a 1k MF resistor and a 0.1ufd C0G cap to ground. This forms a lowpass filter at 1.5kHz (-3dB). This should minimize chopper spikes getting into the DSA. A coax line leaves the PCB and routes through a grounded BNC connector on the lid of the enclosure. Double shielded coax (RG-142) connects the enclosure with the HP35665A spectrum analyzer.

At my location I have EMI from a 1MHz and 100MHz broadcast transmitters. In unshielded setups I can detect the transmitted modulation and when the 1MHz transmitter changes power between 1kW and 10kW at dawn and at dusk. I have detected no EMI or excess noise with this shielded setup.

Minimizing Thermal sources of noise –

The total power dissipation of the components inside the enclosure is 200mW. The voltage regulators are in TO-92 packages with long legs to minimum heat flow to the PCB.

The 10 ohm and 100k ohm gain resistors are RN73, Nichrome, Thin Film, 10ppm / deg C components. With up to 10uV of offset and x10,000 gain the output offset will be up to 100mV. A worst case

condition will be 20ppm / deg C difference in temp co between the gain setting resistors and a 2 deg C ambient change over the 24 hour test time. That will yield a thermally induced noise (from gain change) of 0.4nV RTI. This is comfortably below the 6nV noise density of the op amps. The actual temperature changes in the lab are typically less than 0.5 deg C over 24 hours and the actuall offset voltage has been less than 2uV.

Thermal EMF induced offsets are also a concern. The layout of the three locations on the PCB are the same. So far two opamps have had flicker noise free performance down to 0.001Hz at the 6nV / rt Hz level. So any thermally induces EMFs are below that level.

Testing notes –

The DC voltage from the opamps was monitored with an HP34420A 7.5 digit Nanovoltmeter. The opamps were configured for a gain of 10,000 so a 10nV noise spike is amplified to 100uV before being digitized by the DVM. The noise contribution from the DVM is negligible. The meter was configured for 100 NPLC and autozero was enabled so it took a sample every 3.3 seconds. No averaging was used in the meter. The DVM data was recorded on a PC using the GPIB data bus. At least 20,000 data points was collected for each configuration. The ambient temperature directly next to the test enclosures was measured with a HP2804A Quartz thermometer with a 0.001C resolution. The temperature and data are plotted together. The DVM data is processed with STABLE 32 to produce a Modified Allan Deviation plot of the Voltage noise spectrum.

The HP35665A DSA was configured to display noise density in Vrms / rt Hz. The noise density testing down to 0.0014Hz with over 20 samples typically took 24 hours. At higher frequencies you can collect and average hundreds of spectrum sweeps in a few minutes to reduce the random noise. At the lowest frequencies it can take over an hour for one sweep. The readings were recorded manually into a spreadsheet. Each reading was visually checked to make sure it was not a noise peak or a notch. The readings were recorded to the nearest 0.1dB. The DSA is a 2 channel device so data was collected on two opamps at the same time. The second day of testing checks the third opamp and verifies the DSA noise floor.

Initially the chopper amplifiers were configured for a 60dB gain. However the DSA flicker noise floor intruded on the test results at the lowest frequencies. The amplifiers were then reconfigured for a gain of 80dB and there is now a comfortable 4:1 margin above the DSA noise floor.

The ADA4522-1 was tested with +-2.5V and with +- 5v with basically the same results. Also a 137ua CC load was added between the ouput pin and the negative bus voltage with no change in the noise.

At the conclusion of the 1st round of testing the OPA189, ADA4522 and ADA4528 opamps were replaced and the testing was repeated. The noise density spectrums were within 1 dB of each other.