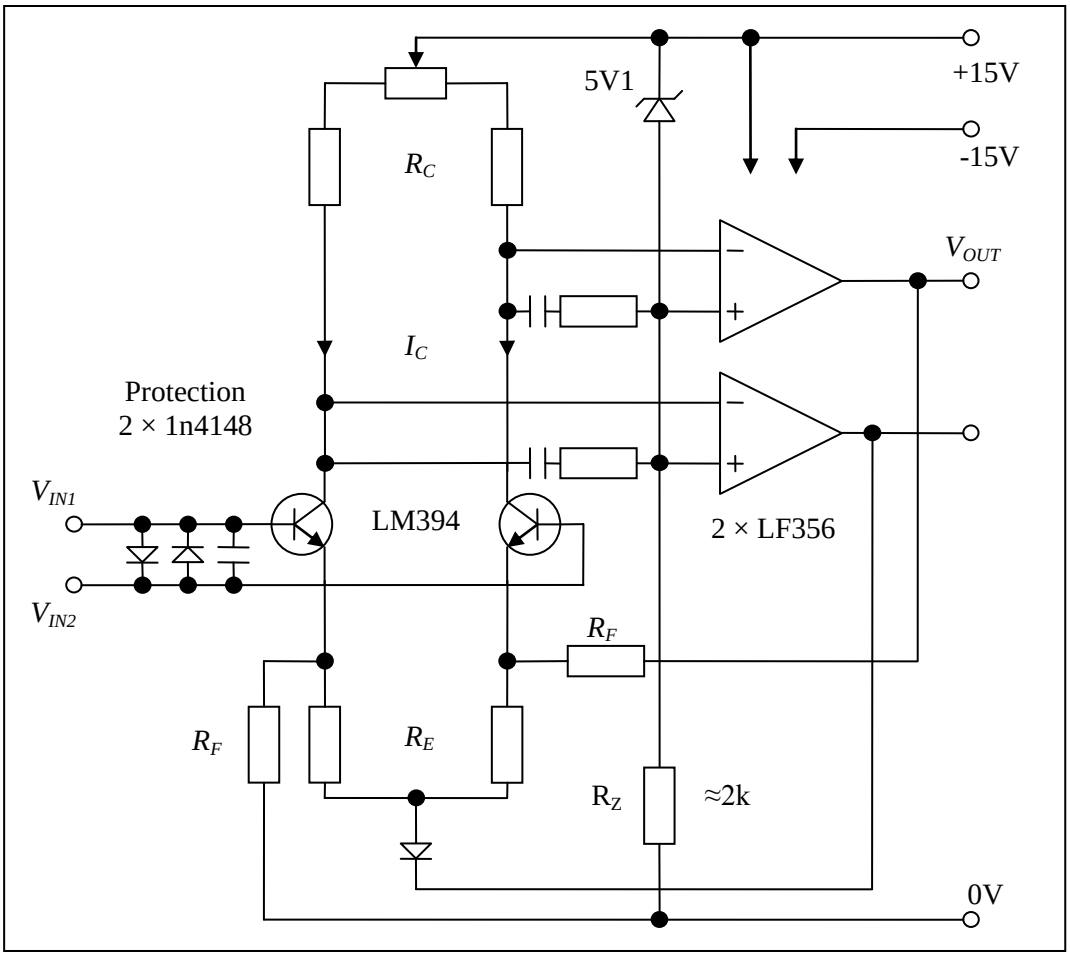


Fig. 1 Outline schematic of a low noise differential input amplifier.

The design is a little unusual – instead of the usual high gain transistor (BC109) the constant current source is implemented with an op-amp and the 5V1 zener ref. The feedback operates so that 5.1V is dropped across each R_C.

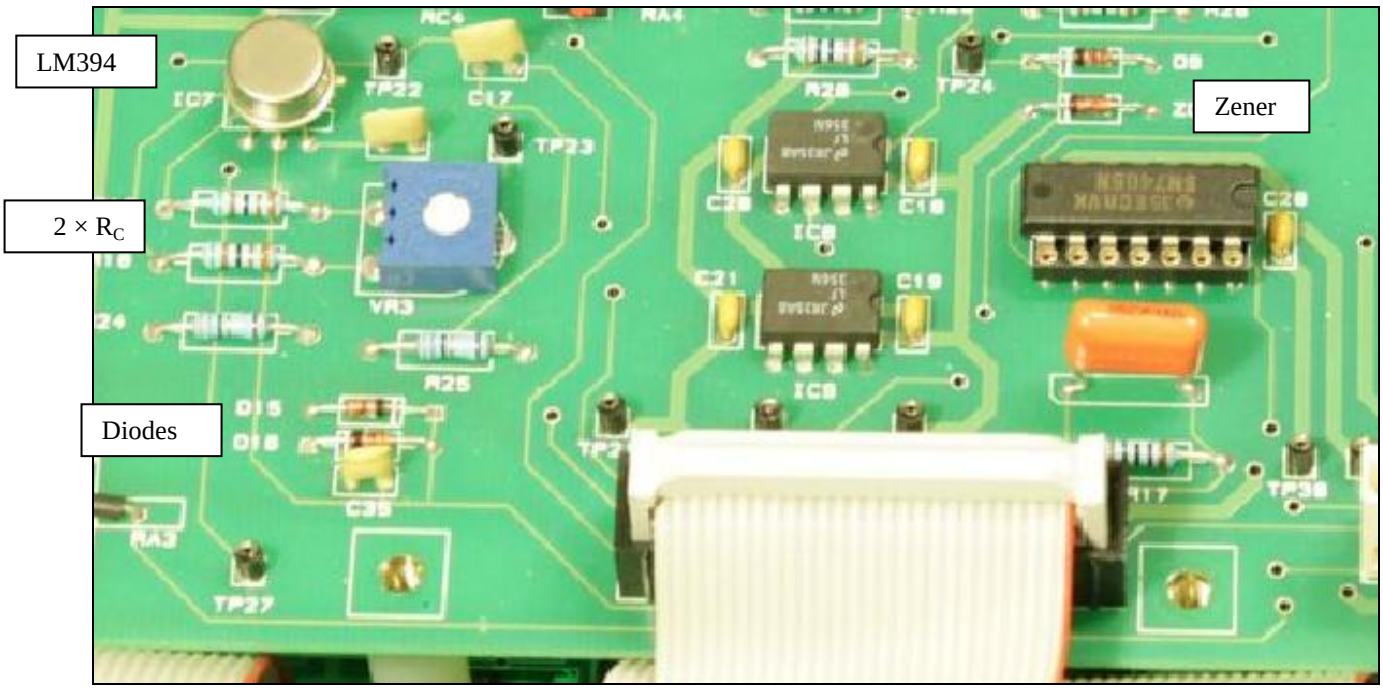


Fig. 2 I am not impressed with the PCB layout. I must have words with the lads

I can't quite make out the values of R_C. I suspect 5k1 so that each transistor runs at 1mA (low voltage noise). The trimpot is to adjust DC offset and is probably 100 or 220Ω.

R_F and R_E set the feedback factor: probably 10k and 10Ω for a gain of 1000.

For a solid reference voltage the zener needs a greedy 5mA (ish) so I guess $R_Z \approx 2k$.

The "snubber" pairs (e.g. C17 and R25) reduce the open loop gain at high frequency, reverting to first order before passing through 0dB in order to ensure closed loop stability. See part 5 monograph 2 especially section 4.4.1.

The pre-amp inputs operate at ≈0V (one is connected to the bridge virtual earth) so that common mode (and CMRR) is not critical. The main resistors can be 1% tolerance.

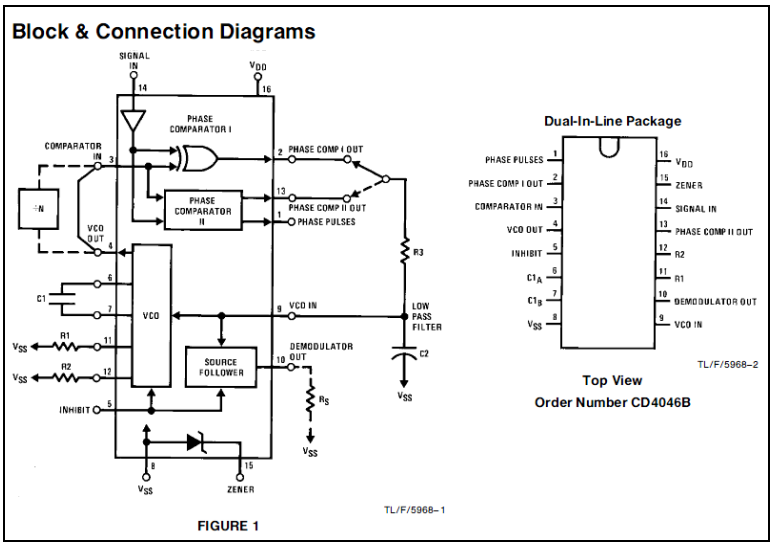
The back-back diodes protect the inputs and the small cap (C35) clobbers high frequency interference.

25Hz ripple is expected – the difference between 75Hz (operating frequency) and 50Hz or, more likely, 100Hz interference. The latter is probably due to the current pulses that charge the PSU smoothing caps (every half cycle) which, with poor wiring layout, transmits magnetic flux. Have a look at the error signal before the synchronous rectifier (before the CD4066 etc).

Also: -

1). What is the metal can IC on the corner of the main analogue PCB?

2). There are two CD4046 phase lock loop chips. Could you please check the inputs (pin 14) and outputs (pin 4). I can understand one (recovers in-phase ref for the main synchronous rectifier) but, as far as I can remember there is no quadrature servo. Also it needs only one PLL to do both (running at 300Hz and divide by 4 using CD4013).



3). I guess that the AD 7525 BCD MDAC became obsolete, hence the bodge (module) on the F300.