

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY TICPAL22V10
DEVICES TICPAL22V10
INCLUDED

ARRAY PROGRAMMING PROCEDURE:

Array FAMOS transistors are programmed by executing the following programming sequence. Each FAMOS transistor can be programmed by selecting the appropriate Inputs Line(s), (1 of 45), and Product Lines(s), (1 of 17). The levels for selecting Input Lines and Product Lines are shown in Tables 1-3 and 1-4.

- Step 1. Raise Pin 24 to 5V and Pin 13 to V_{IH} .
- Step 2. Raise Pin 1 to V_{IHH} .
- Step 3. Address the first location.
- Step 4. Place the data to be programmed on I/O pins.
- Step 5. $X = 0$
- Step 6. Program one 1.0 ms pulse by pulsing Pin 13 to a V_{IHH} level.
- Step 7. $X = X + 1$
- Step 8. If $X = 10$, then GOTO Step 10.
- Step 9. Verify the data by taking Pin 13 to V_{IL} . If incorrect, repeat Steps 6 through 8
- Step 10. Program one pulse of duration $4 * X * 1.0$ ms.
- Step 11. Reverify data. If incorrect, device fails (END).
- Step 12. Repeat Steps 4 through 11 until all addresses are programmed.
- Step 13. Verify array at 5V.
- Step 14. Lower Pin 1 to 0V.
- Step 15. Lower Pin 24 to 0V.

SECURITY FUSE PROGRAMMING PROCEDURES: (See Figure 3)

- Step 1. Raise Pin 24 to 5V.
- Step 2. Address the device per Tables 1-3 and 1-4.
- Step 3. Raise Pin 1 to a V_{IHH} .
- Step 4. Raise Pin 3 to a V_{IHH} .
- Step 5. Program the Security Fuse by pulsing Pin 13 to a V_{IHH} .

PREPARED BY B. Cole PAL24C-1.DWG		DATE 10/28/88		TEXAS INSTRUMENTS	
CHECKED BY <i>F. Sweeney</i>		DATE 12/15/88		TITLE: ALGORITHM SPECIFICATION TICPAL22V10	
ENGINEER F. Sweeney		DATE 10/28/88		PAL24010	
APPROVED BY <i>Donald B. Thomas</i>		DATE 12/15/88			
RELEASED BY		DATE 		REVISION LETTER	SIZE A
				SHEET 1 9	

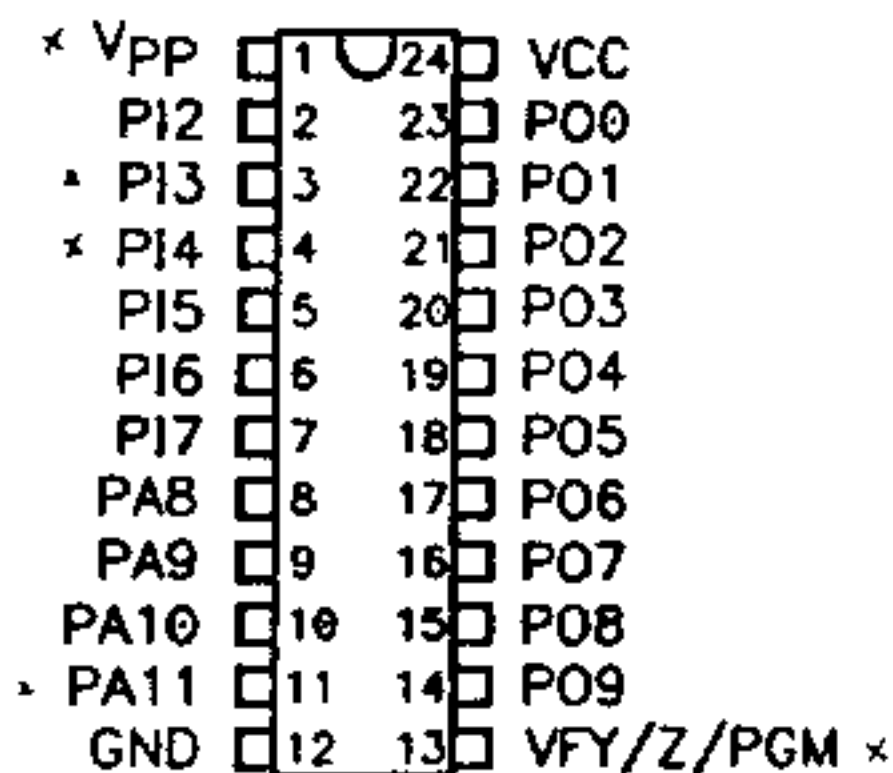
SECURITY FUSE VERIFY PROCEDURES: (See Figure 3)

- Step 1. Raise Pin 24 to 5V.
- Step 2. Raise Pin 1 to a V_{IH} .
- Step 3. Raise Pin 4 to V_{IH} .
- Step 4. Address the device per Tables 1-3 and 1-4 for Security Fuse Verify. With Pin 13 at V_{IL} , Pin 3 will act as an output under these conditions and will be a logical "0" if the Security Fuse is not programmed, and a logical "1" if the Security Fuse is programmed.

NOTE: Pin 13 should always be at V_{IH} , when changing a device address.

pin assignments in programming mode

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)

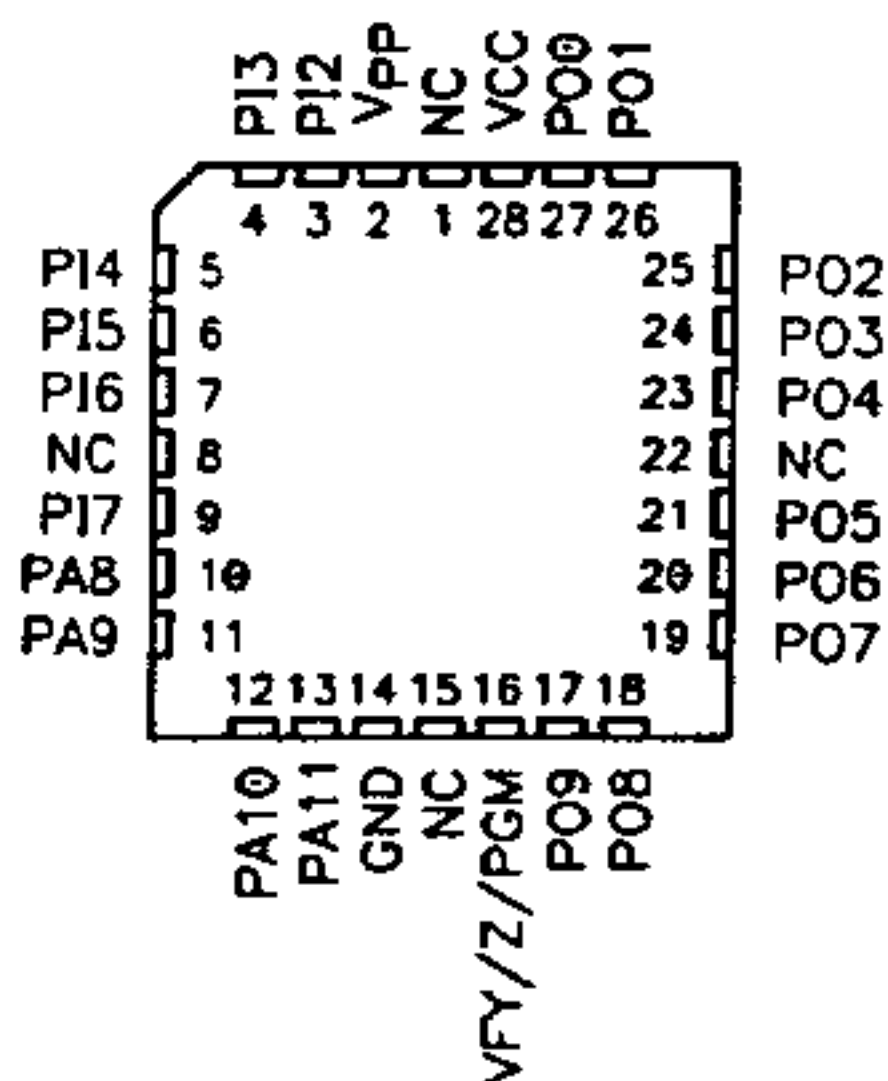


TABLE 1-2. Programming Parameters, $T_A = 25^\circ \text{C}$

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
V_{CCP}	Supply Voltage - Programming	4.75	5.00	5.25	V
V_{IHH}	Programming Voltage	13.00	13.50	14.00	V
V_{IH}	High Level Input Voltage	3.00		V_{CC}	V
V_{IL}	Low Level Input Voltage	0.00		0.40	V
V_{OH}	Voltage Out - High	2.40			V
V_{OL}	Voltage Out - Low			0.40	V
I_{pp}	Supply Current - Programming			90	mA
t_p	Delay to Programming Voltage	20			μs
t_{prime}	Programming Pulse Width	0.95		1.05	ms
t_{final}	Programming Pulse Width	3.8		42	ms
t_{dp}	Delay to Program	1			μs
t_r, t_f	V_{IHH} Rise/Fall Time	50			ns
t_{r1}, t_{f1}	V_{IHH} Rise/Fall Time PGM/VFY	20			ns
t_{as}	Address Set-up Time	1			μs
t_{ah}	Address Hold Time	1			μs
t_{hp}	Hold from Program or Verify	1			μs
t_{ds}	Data Set-up Time	1			μs
t_{dh}	Data Hold Time	1			μs
t_{scty}	Programming PW for Security	50			ms
t_{dv}	Delay from Program to Verify	2			μs
t_{vd}	Delay to Data Out			1	μs
t_{vp}	Verify Pulse Width	2			μs
t_{dz}	Verify to High Z			1	μs

TABLE 1-3, INPUT LINE ADDRESSING

INPUT LINE NUMBER	INPUT LINE NUMBER-ADDRESS PIN STATES					
	P17	P16	P15	P14	P13	P12
00	L	L	L	L	L	L
01	L	L	L	L	L	H
02	L	L	L	L	H	H
03	L	L	L	L	H	H
04	L	L	L	H	L	H
05	L	L	L	H	L	H
06	L	L	L	H	H	H
07	L	L	L	H	H	H
08	L	L	H	L	L	H
09	L	L	H	L	L	H
10	L	L	H	L	H	H
11	L	L	H	L	H	H
12	L	L	H	H	L	H
13	L	L	H	H	L	H
14	L	L	H	H	H	H
15	L	L	H	H	H	H
16	L	H	L	L	L	H
17	L	H	L	L	L	H
18	L	H	L	L	H	H
19	L	H	L	L	H	H
20	L	H	L	H	L	H
21	L	H	L	H	L	H
22	L	H	L	H	H	H
23	L	H	L	H	H	H
24	L	H	H	L	L	H
25	L	H	H	L	L	H
26	L	H	H	L	H	H
27	L	H	H	L	H	H
28	L	H	H	H	L	H
29	L	H	H	H	L	H
30	L	H	H	H	H	H
31	L	H	H	H	H	H
32	H	L	L	L	L	H
33	H	L	L	L	L	H
34	H	L	L	L	H	H
35	H	L	L	L	H	H
36	H	L	L	H	L	H
37	H	L	L	H	L	H
38	H	L	L	H	H	H
39	H	L	L	H	H	H
40	H	L	H	L	L	H
41	H	L	H	L	L	H
42	H	L	H	L	H	H
43	H	L	H	L	H	H
ARCH S0/S1	H	H	H	H	H	H
TURBO	H	H	H	H	H	H
SF PROG	L	L	L	L	H	L
SF VERIFY	L	L	L	H	OUTPUT	L

ARCH S0 - ARCHITECTURE POLARITY FUSE
 ARCH S1 - ARCHITECTURE REGISTER/LOGIC FUSE

SF - SECURITY FUSE

TABLE 1-4, PRODUCT TERM ADDRESSING

PRODUCT TERM										PRODUCT TERM SELECT ADDRESS PIN STATES			
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	PA11	PA10	PA9	PA8
0	0	0	0	0	0	0	0	0	0	L	L	L	L
1	1	1	1	1	1	1	1	1	1	L	L	L	H
2	2	2	2	2	2	2	2	2	2	L	L	H	L
3	3	3	3	3	3	3	3	3	3	L	L	H	H
4	4	4	4	4	4	4	4	4	4	L	H	L	L
5	5	5	5	5	5	5	5	5	5	L	H	L	H
6	6	6	6	6	6	6	6	6	6	L	H	H	L
7	7	7	7	7	7	7	7	7	7	L	H	H	H
	8	8	8	8	8	8	8	8		H	L	L	L
	9	9	9	9	9	9	9	9		H	L	L	H
		10	10	10	10	10	10			H	L	H	L
		11	11	11	11	11	11			H	L	H	H
			12	12	12	12				H	H	L	L
			13	13	13	13				H	H	L	H
				14	14					H	H	H	L
				15	15					H	H	H	H
OE	OE	OE	OE	OE	OE	OE	OE	OE	OE	HH	H	H	H
			AR							H	H	H	H
						SP				H	H	H	H
S0	S0	S0	S0	S0	S0	S0	S0	S0	S0	HH	L	L	L
S1	S1	S1	S1	S1	S1	S1	S1	S1	S1	HH	L	H	L
SF PROG/VERIFY										L	L	L	L
TURBO										HH	H	H	L

OE - OUTPUT ENABLE

AR - ASYNCHRONOUS RESET

SP - SYNCHRONOUS PRESET

S0 - ARCHITECTURE POLARITY FUSE

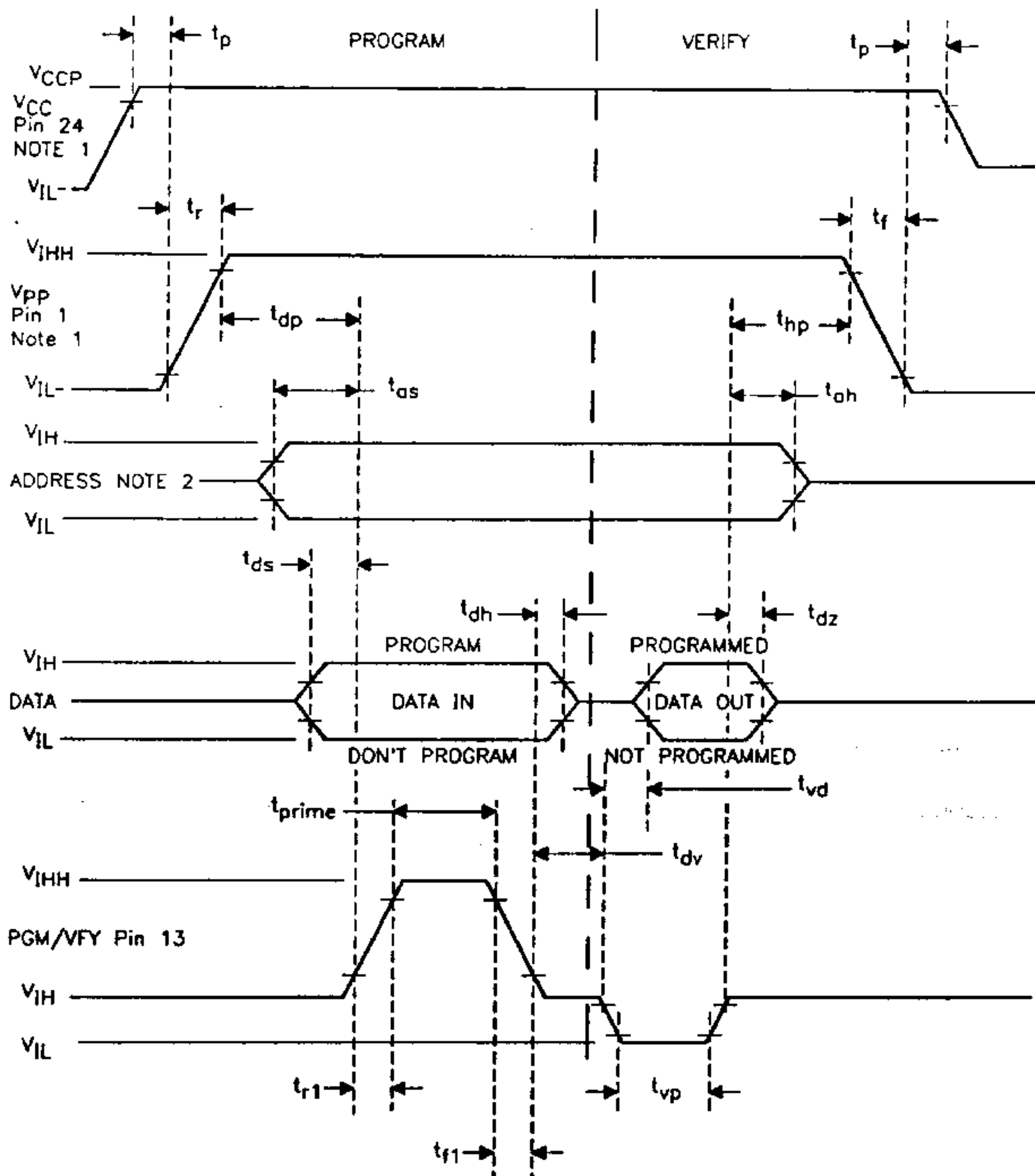
S1 - ARCHITECTURE REGISTER/LOGIC FUSE

- DATA IS PIN 20

- DATA IS PIN 17

- OUTPUT POLARITY

- OUTPUT REGISTER/LOGIC

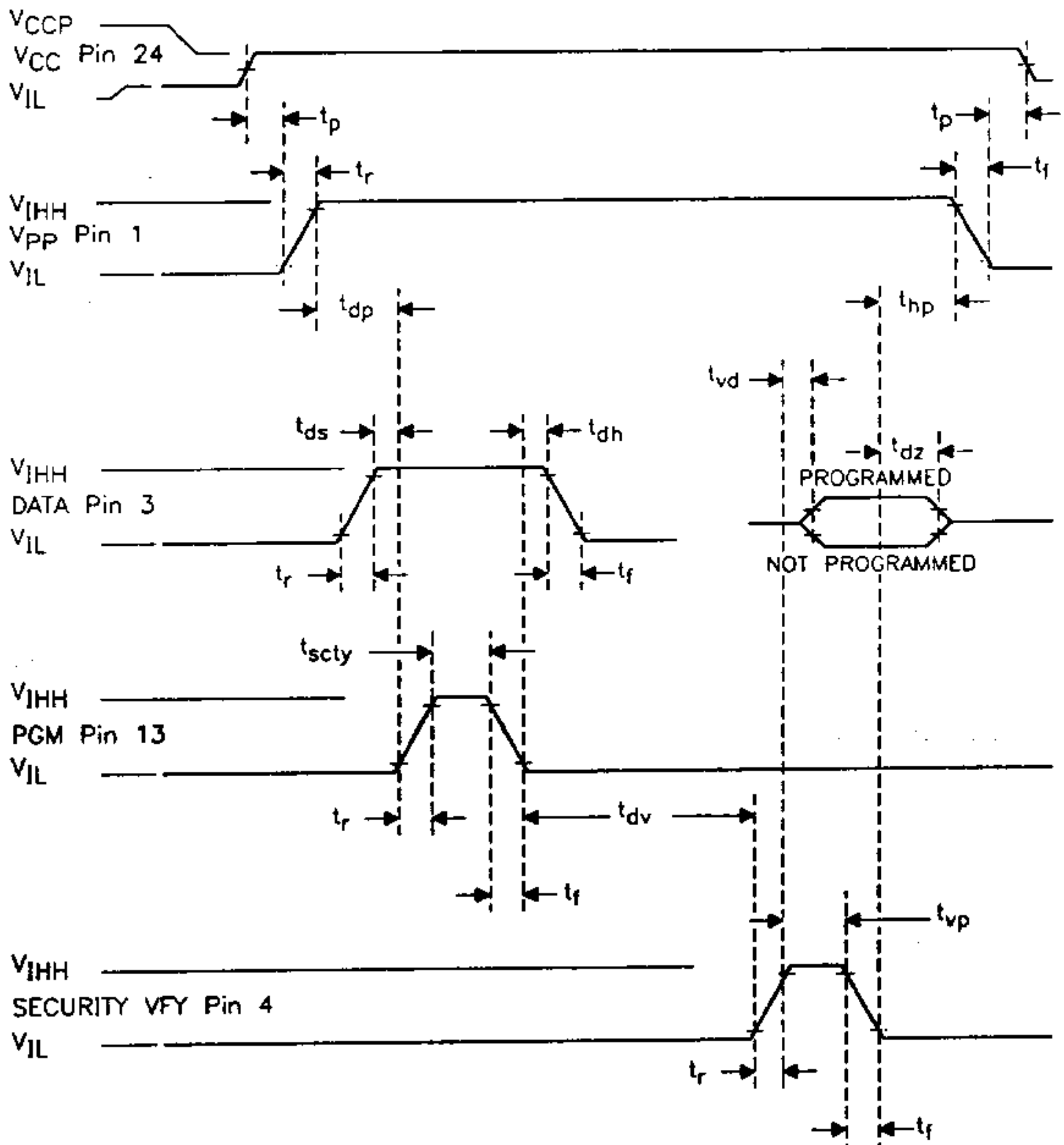


Notes:

1. Pin 1 & Pin 24 should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming OE Product Terms & Architecture bits, Pin 11 must go to V_{IHH} and satisfy t_{as} and t_{oh} .

FIGURE 3

Programming Waveforms Security Fuse



PROGRAMMING ALGORITHM TEMPLATE

SPECIFICATION NUMBER PAL24010
 DEVICE FAMILY TICPAL22V10
 INCLUDED DEVICES TICPAL22V10

PROGRAMMER INFO:

MANUFACTURER : _____ MODEL: _____ ADAPTER #: _____
 UPDATE VERSION : _____ FW/SW P/N: _____

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCCP - SUPPLY VOLTAGE - PROGRAMMING	4.75	5	5.25	V	
VIHH - PROGRAMMING VOLTAGE (PIN1)	13.0	13.5	14.0	V	
VIH - HIGH LEVEL INPUT VOLTAGE	3.0		VCC	V	
VIL - LOW LEVEL INPUT VOLTAGE			0.4	V	
VOH - VOLTAGE OUT - HIGH	2.4			V	
VOL - VOLTAGE OUT - LOW			0.4	V	
Tprime - PROGRAMMING PULSE WIDTH	0.95		1.05	MS	
Tfinal - PROGRAMMING PULSE WIDTH	3.80		42.0	MS	
tp - DELAY TO PROGRAMMING VOLTAGE (RISE)	20			US	
tp - DELAY TO PROGRAMMING VOLTAGE (FALL)	20			US	
tr - VIHH rise TIME (PIN 1)	50			NS	
trl - VIHH rise TIME (PGH/VFY)	20			NS	
tf - VIHH fall TIME (PIN 1)	50			NS	
tfl - VIHH fall TIME (PGH/VFY)	20			NS	
tdp - DELAY TO PROGRAM	1			US	
tas - ADDRESS SET-UP TIME	1			US	
tah - ADDRESS HOLD TIME	1			US	
thp - HOLD FROM PROGRAM OR VERIFY	1			US	
tds - DATA SET-UP TIME	1			US	
tdh - DATA HOLD TIME	1			US	
tdv - DELAY FROM PROGRAM TO VERIFY	2			US	
tvp - VERIFY PULSE WIDTH	2			US	

PROGRAMMING ALGORITHM TEMPLATE

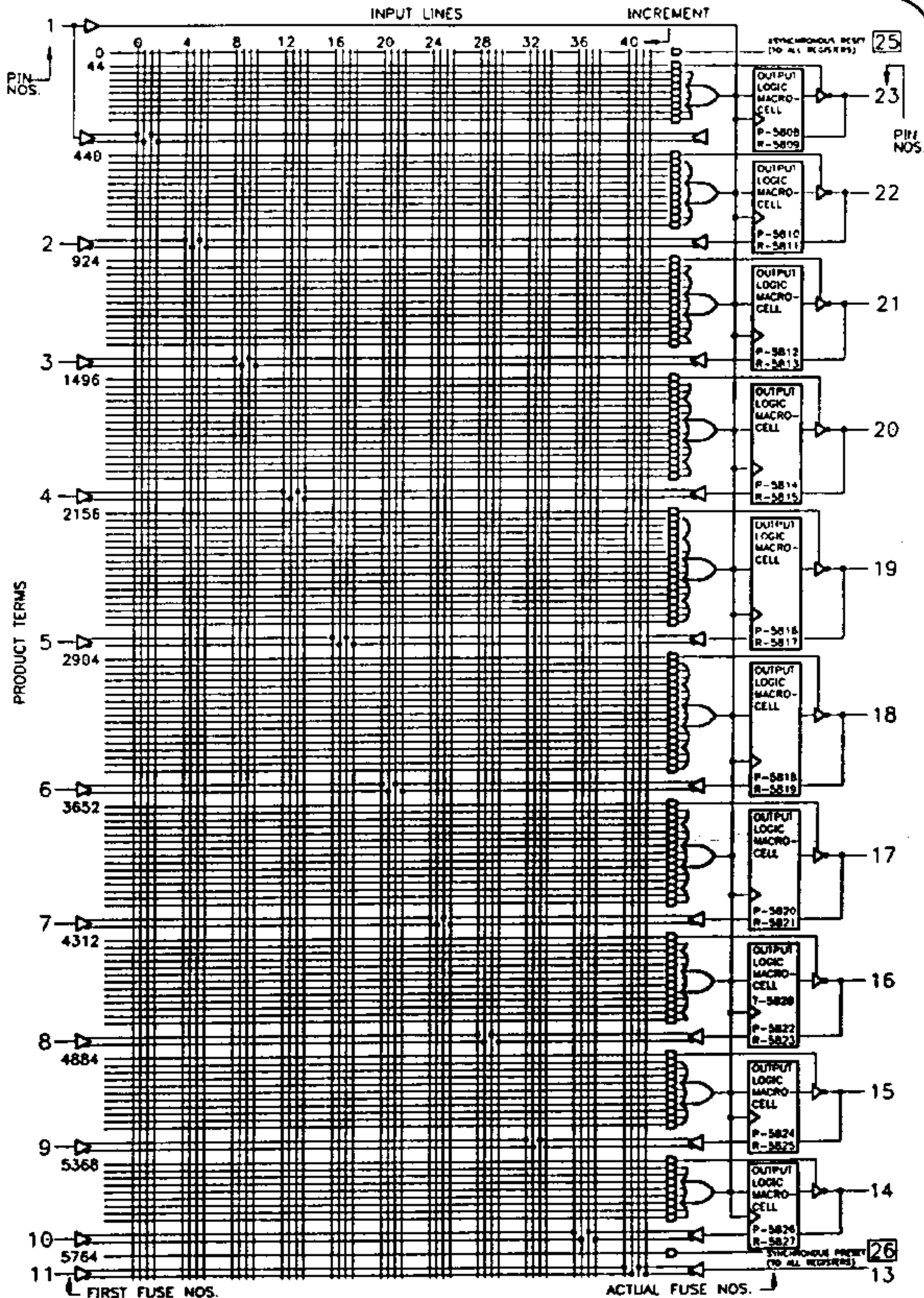
SPECIFICATION NUMBER PAL24010 ----- C O N T I N U A T I O N
 DEVICE FAMILY TICPAL22V10
 INCLUDED DEVICES TICPAL22V10

PROGRAMMER INFO:

MANUFACTURER : _____ MODEL: _____ ADAPTER #: _____
 UPDATE VERSION : _____ FW/SW P/N: _____

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCCP - SUPPLY VOLTAGE	4.75	5	5.25	V	
VIHH - PROGRAM VOLTAGE (PIN1)	13.0	13.5	14.0	V	
VIHH - PROGRAM VOLTAGE (PGM)	13.0	13.5	14.0	V	
tp - DELAY TO PROGRAMMING VOLTAGE (RISE)	20			US	
tp - DELAY TO PROGRAMMING VOLTAGE (FALL)	20			US	
tr - VIHH rise TIME (PIN 1 - SECTY)	50			NS	
tr - VIHH rise TIME (PIN 3 - SECTY)	50			NS	
tr - VIHH rise TIME (PGM - SECTY)	50			NS	
tr - VIHH rise TIME (SECURITY VFY)	50			NS	
tf - VIHH fall TIME (PIN 1 - SECTY)	50			NS	
tf - VIHH fall TIME (PIN 3 - SECTY)	50			NS	
tf - VIHH fall TIME (PGM - SECTY)	50			NS	
tf - VIHH fall TIME (SECURITY VFY)	50			NS	
tdp - DELAY TO PROGRAM (SECTY)	1			US	
thp - HOLD FROM PROGRAM OR VERIFY (SECTY)	1			US	
tds - DATA SET-UP TIME (SECTY)	1			US	
tdh - DATA HOLD TIME (SECTY)	1			US	
tacty - PROGRAMMING PW FOR SECURITY	50			MS	
tdv - DELAY FROM PROGRAM TO VERIFY	2			US	
tvp - VERIFY PULSE WIDTH	2			US	

NOTE: Inside each Macrocell, the 'P' fuse No. is the polarity fuse, and the 'R' fuse No. is the register fuse, and the 'T' fuse, in the macrocell for output 16, is the TURBO fuse.



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
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