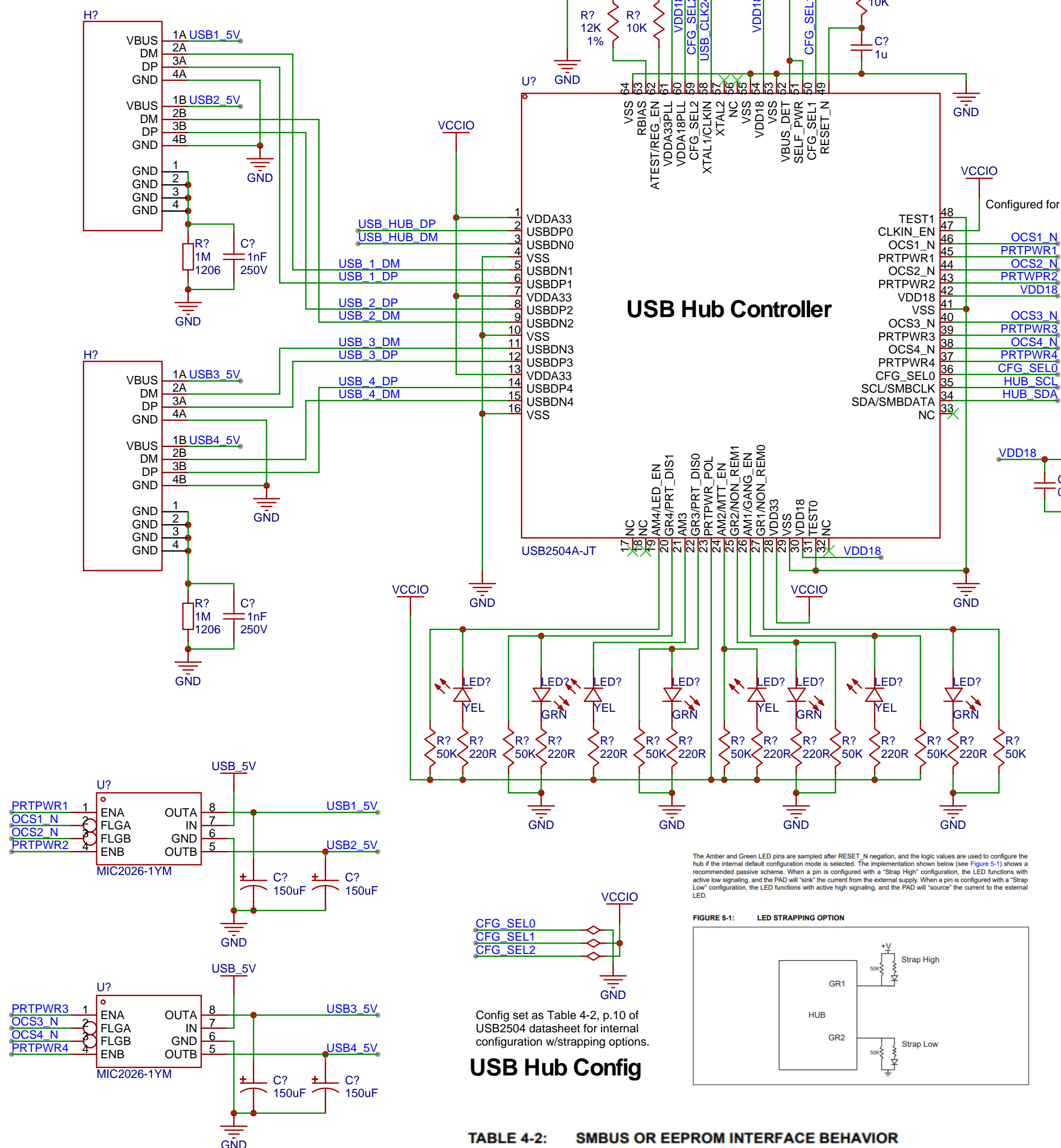
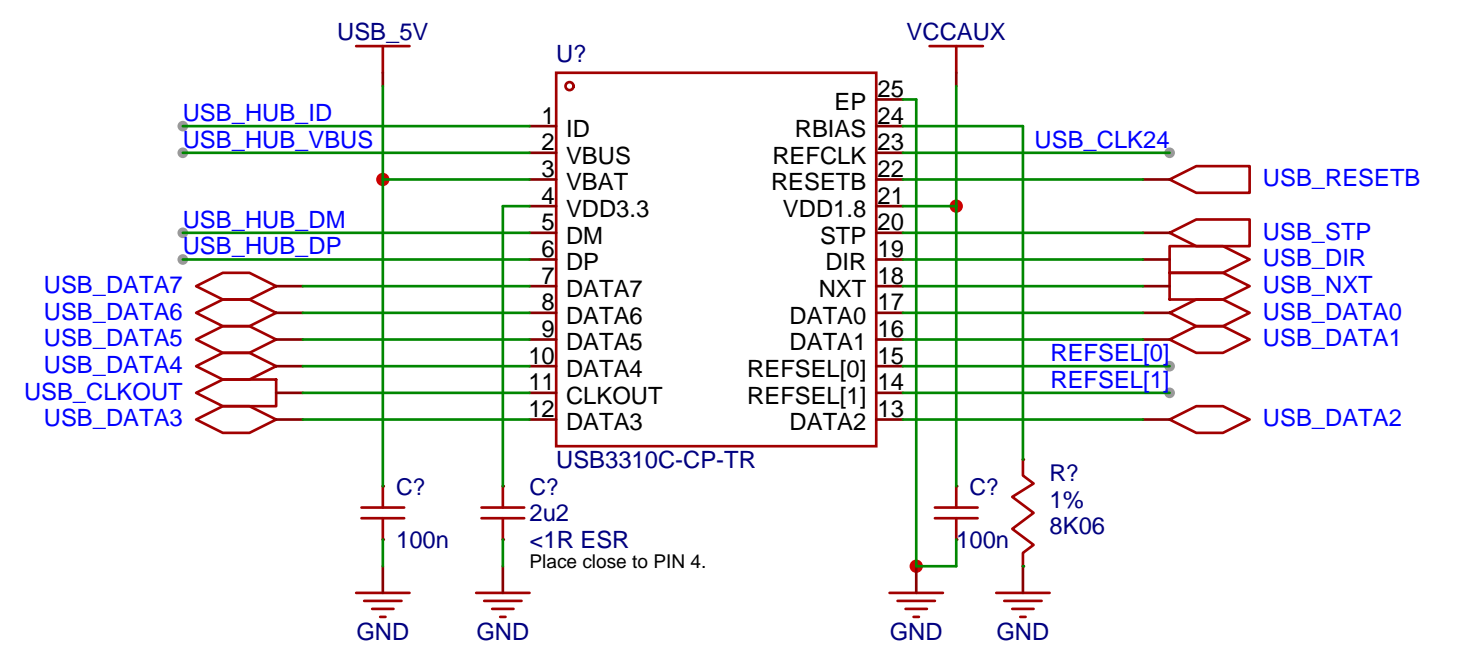


4x USB Type A Sockets

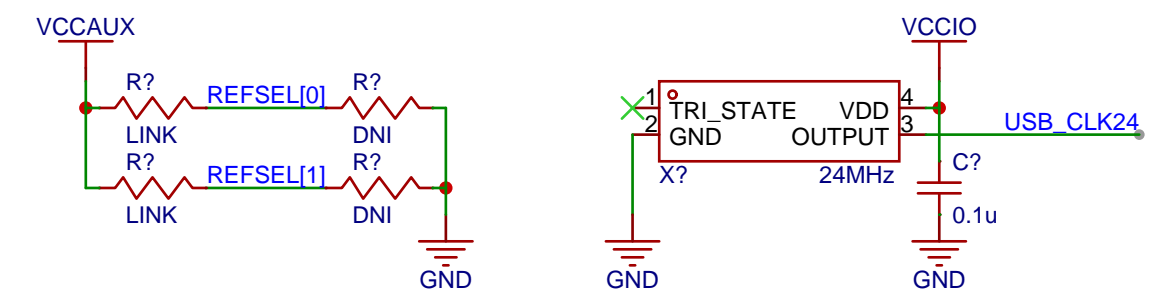


USB Connector Power Switches

TABLE 4-2: SMBUS OR EEPROM INTERFACE BEHAVIOR			
CFG_SEL2	CFG_SEL1	CFG_SEL0	SMBus or EEPROM Interface Behavior
X	0	0	Configured as an SMBus slave for external download of user-defined descriptors. SMBus slave address is 0101100
X	0	1	Configured as an SMBus slave for external download of user-defined descriptors. SMBus slave address is 0101101
0	1	0	Internal Default Configuration
1	1	0	Internal Default Configuration via strapping options.
X	1	1	2-wire (I ² C) EEPROMS are supported,



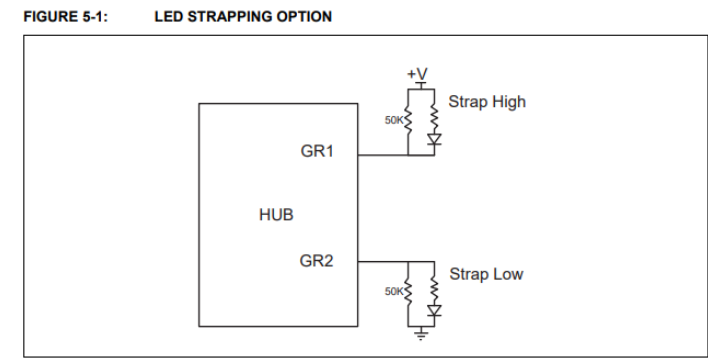
USB PHY




REFSEL		REFCLK FREQUENCY
[1]	[0]	
0	0	13 MHz
0	1	19.2 MHz
1	0	26 MHz
1	1	24 MHz

USB Clock & PHY Config

Port 4.3 Green LED & Port Disable strapping option.	GR[4:3]/PRT_DIS[1:0]	VO12	Green indicator LED for ports 4 and 3. Will be active low when LED support is enabled via EEPROM or SMBus. If the hub is configured by the internal default configuration, these pins will be sampled at RESET. N negation to determine if ports 4 & 3 will be permanently disabled. Also, the active state of the LED's will be determined as follows: PRT_DIS[1:0] = '00': All ports are enabled, GR[4] is active high, GR[3] is active high. PRT_DIS[1:0] = '01': Port 4 is disabled, GR[4] is active high, GR[3] is active low. PRT_DIS[1:0] = '10': Ports 4 & 3 are disabled, GR[4] is active low, GR[3] is active high. PRT_DIS[1:0] = '11': Ports 4, 3 & 2 are disabled, GR[4] is active low, GR[3] is active low.
Port [2:1] Green LED & Port Non-Removable strapping option.	GR[2:1]/NON_REM[1:0]	VO12	Green indicator LED for ports 2 and 1. Will be active low when LED support is enabled via EEPROM or SMBus. If the hub is configured by the internal default configuration, these pins will be sampled at RESET. N negation to determine if ports [2:1] contain permanently disabled (non-removable) devices. Also, the active state of the LED's will be determined as follows: NON_REM[1:0] = '00': All ports are non-removable, GR[2] is active high, GR[1] is active high. NON_REM[1:0] = '01': Port 1 is non-removable, GR[2] is active low, GR[1] is active low. NON_REM[1:0] = '10': Ports 1 & 2 are non-removable, GR[2] is active low, GR[1] is active low. NON_REM[1:0] = '11': Ports 1, 2, & 3 are non-removable, GR[2] is active low, GR[1] is active low.
Port 4 Amber LED & LED Enable strapping option	AM[4]/LED_EN	VO12	Amber indicator LED for port 4. Will be active low when LED support is enabled via EEPROM or SMBus. If the hub is configured by the internal default configuration, this pin will be sampled at RESET. N negation to determine if port 4 LED support is enabled or disabled. Also, the active state of the LED will be determined as follows: '1' = LED support is disabled, LED is inactive. '1' = LED support is enabled, LED is active low.
Port 3 Amber LED & Port 2 Amber LED & MTT Disable	AM[3]/AM[2]/MTT_EN	VO12	Amber indicator LED for port 3. Signal will be active low. If the hub is configured by the internal default configuration, this pin will be sampled at RESET. N negation to determine if MTT support is disabled (DIT only). Also, the active state of the LED will be determined as follows: '1' = MTT support is disabled, LED is active high. '1' = MTT support is enabled, LED is active low.
Port 1 Amber LED & Gang Power Switching and Current Sensing strapping option.	AM[1]/GANG_EN	VO12	Amber indicator LED for port 1. Will be active low when LED support is enabled via EEPROM or SMBus. If the hub is configured by the internal default configuration, this pin will be sampled at RESET. N negation to determine if downstream port power switching and current sensing are enabled or disabled. Also, the active state of the LED will be determined as follows: '1' = Port-by-port sensing & switching, LED is active high. '1' = Gangled sensing & switching, LED is active low.
Port Power Polarity strapping	PRTTPWR_POL	VO12	Port Power Polarity strapping determination for the active signal polarity of the 4-SPRTTPWR pins. While RESET_N is asserted, the logic state of this pin will (through the use of internal combinatorial logic) determine the active state of the 4-SPRTTPWR pins in order to ensure that downstream port power is not inadvertently enabled to inactive ports during a hardware reset. On the rising edge of RESET_N (see the applicable RESET_N timing table in Section 4.6.1), the logic value will be latched internally, and will retain the active signal polarity for the PRTTPWR[4:1] pins. '1' = PRTTPWR[4:1] PIN pins have an active 'high' polarity. '0' = PRTTPWR[4:1] PIN pins have an active 'low' polarity.



Schematic	XCAT-7100			Update Date	2023-03-19
				Create Date	2023-02-11
File	USB HUB			Part Number	
Drawn	nockieboy	XCAT-7100_Pro			
Reviewed					
		VER	SIZE	PAGE	9 OF 11
		V0.1	A4	EasyEDA.com	