U1.1
EP4CE10E22C8N
BANK 1
IO
IO
IO
IO,DIFFIO_L1n,(DATA1,ASDO)
IO,VREFB1N0
IO,DIFFIO_L2p,(FLASH_nCE,nCSO)
IO,DIFFIO_L4p,(DQS0L/CQ1L,DPCLK0)
IO,DIFFIO_L4n
IO,(DATA0)
1 INT_REQ
2 BEEP
3 RESET
6 ASDO
7 nCSO
10 UART_TX
11 UART_RX
13 DATA

U1.2
EP4CE10E22C8N
IO,DIFFIO_L6n
IO,DIFFIO_L8p,(DQS1L/CQ1L#,DPCLK1)
IO,VREFB2N0
IO,RUP1
IO,RDN1
IO
BANK 2
28 IEI_3v3
30
31 SD_DI
32 SD_CLK
33 SD_DO
34 A0

U1.3
EP4CE10E22C8N
BANK 3
IO,DIFFIO_B1p
IO,DIFFIO_B1n
IO,(DQS1B/CQ1B#,DPCLK2)
IO,PLL1_CLKOUTp
IO,PLL1_CLKOUTn
IO,VREFB3N0
IO,DIFFIO_B9p,(DQ1B)
IO,DIFFIO_B9n,(DQ1B)
IO,DIFFIO_B10p,(DQ1B)
IO,DIFFIO_B11p
IO,DIFFIO_B11n
38 A1
39 A2
42 A3
43 A7
44 A6
46 A5
49 A4
50 A8
51 A9
52 A10
53 A11

U1.4
EP4CE10E22C8N
BANK 4
IO,DIFFIO_B12p
IO,DIFFIO_B12n
IO,DIFFIO_B15p,(DQ1B)
IO,DIFFIO_B16p,(DQ1B)
IO,DIFFIO_B16n,(DQ1B)
IO,VREFB4N0
IO,RUP2,(DQ1B)
IO,RDN2,(DQ1B)
IO,DIFFIO_B20n,(DQS0B/CQ1B,DPCLK3)
IO
IO,DIFFIO_B21p
IO,DIFFIO_B21n
IO,DIFFIO_B22p
54 A15
55 A14
58 A13
59 A12
60 EA_DIR
64 EA_OE
65 E14
66 E15
67 E16
68 E17
69 E18
70 E19
71 E20
72 E21

U1.5
EP4CE10E22C8N
BANK 5
IO
IO
IO
IO,RUP3
IO,RDN3
IO,VREFB5N0
IO
IO,DIFFIO_R8n
IO,DIFFIO_R8p,(DQS1R/CQ1R#,DPCLK4)
IO,DIFFIO_R7n,(DEV_OE)
IO,DIFFIO_R7p,(DEV_CLRn)
73 IEO_3v3
74 PS_CLOCK
75 PS_DATA
76 B7
77 B6
80 B5
83 B4
84 B3
85 B2
86 B1
87 B0

U1.6
EP4CE10E22C8N
BANK 6
IO, DIFFIO_R4n, (INIT_DONE)
IO, DIFFIO_R4p, (CRC_ERROR)
IO
IO, DIFFIO_R3n, (nCEO)
IO, DIFFIO_R3p, (CLKUSR)
IO, (DQS0R/CQ1R,DPCLK5)
IO, VREFB6N0
IO, DIFFIO_R1n
98 G7
99 G6
100 G5
101 G4
103 G3
104 G2
105 G1
106 G0

U1.7
EP4CE10E22C8N
BANK 7
IO,DIFFIO_T20p,(DQS0T/CQ1T,DPCLK6)
IO,DIFFIO_T19p
IO,PLL2_CLKOUTn
IO,PLL2_CLKOUTp
IO,RUP4,(DQ1T)
IO,RDN4,(DQ1T)
IO,VREFB7N0
IO,DIFFIO_T16n,(DQ1T)
IO,DIFFIO_T16p
IO,DIFFIO_T13p
IO
IO,DIFFIO_T12n
IO,DIFFIO_T12p
110 R7
111 R6
112 R5
113 R4
114 R3
115 R2
119 R1
120 R0
121 Z80_INTA
124 Z80_RD
125 Z80_WR
126 Z80_MREQ
127 Z80_IORQ

U1.8
EP4CE10E22C8N
BANK 8
IO,DIFFIO_T11n
IO,DIFFIO_T11p
IO,DIFFIO_T10n,(DATA2),(DQ1T)
IO,DIFFIO_T10p,(DATA3),(DQ1T)
IO,DIFFIO_T8n,(DQ1T)
IO,VREFB8N0
IO,(DATA5),(DQ1T)
IO,(DATA6)
IO,DIFFIO_T5p
IO,DIFFIO_T2p,(DQS1T/CQ1T#,DPCLK7)
IO,DIFFIO_T1n,(DQ1T)
IO,DIFFIO_T1p,(DM1T)
128 Z80_M1
129 Z80_RES
132 D7
133 D6
135 D5
136 D4
137 D3
138 D2
141 D1
142 D0
143 245_OE
144 245_DIR

U1.9
EP4CE10E22C8N
FPGA_CLK 23
24
25
27
Z80_CLK 30
89
88
CLK1,DIFFCLK_0n
CLK2,DIFFCLK_1p
CLK3,DIFFCLK_1n
CLK4,DIFFCLK_2p
CLK5,DIFFCLK_2n
CLK6,DIFFCLK_3p
CLK7,DIFFCLK_3n

U1.10
EP4CE10E22C8N
TDI 15 TDI
TDO 20 TDO
TCK 16 TCK
TMS 18 TMS
94 MSEL0
2.5V 96 MSEL1
97 MSEL2
nCE 21 nCE
DCLK 12 DCLK
92 CONF_DONE
14 nCONFIG
9 nSTATUS
R4 10K CONF_DONE
R5 10K nCONFIG
R6 10K
3.3V
GND

U1.11
EP4CE10E22C8N
17 VCCIO1 VCCINT 5
26 VCCIO2 VCCINT 29
VCCINT 45
40 VCCIO3 VCCINT 61
47 VCCIO3 VCCINT 78
VCCINT 102
56 VCCIO4 VCCINT 116
62 VCCIO4 134
81 VCCIO5
93 VCCIO6
117 VCCIO7
122 VCCIO7
130 VCCIO8
139 VCCIO8
3.3V
1.2V
GND

U1.12
EP4CE10E22C8N
4 GND GND 79
19 GND GND 82
22 GND GND 95
27 GND GND 118
41 GND GND 123
48 GND GND 131
57 GND GND 140
63 GND
GND
GND

U1.13
EP4CE10E22C8N
35 VCCA1 GNDA1 36 GNDA1
37 VCCD_PLL1
107 VCCA2 GNDA2 108 GNDA2
109 VCCD_PLL2
FB1 180 Ohm
FB2 180 Ohm
FB3 180 Ohm
FB4 180 Ohm
C9 100nF
C10 100nF
1.2V
2.5V
GNDA1
GNDA2
GND

U2
AD1580BRTZ-R2
1 V+
2 V-
3 NC
C2 1uF
+5V
GND

U3.1
ADV7125KSTZ140
35 COMP
37 RSET
24 CLOCK
12 SYNC#
11 BLANK#
38 PSAVE#
13 VAA
29 VAA
30 VAA
36 VREF
1 GND
2 GND
14 GND
15 GND
25 GND
26 GND
39 GND
40 GND
FPGA_CLK
R1 530R
R2 1K
R3 100K
C1 100nF
C3 10nF
C4 10nF
C5 10nF
C6 10nF
C7 10nF
C8 10nF
+5V
GND

U3.2
ADV7125KSTZ140
B0 16
B1 17
B2 18
B3 19
B4 20
B5 21
B6 22
B7 23
IOB 28
IOB# 27
GND

U3.3
ADV7125KSTZ140
G0 3
G1 4
G2 5
G3 6
G4 7
G5 8
G6 9
G7 10
IOG 32
IOG# 31
GND

U3.4
ADV7125KSTZ140
R0 41
R1 42
R2 43
R3 44
R4 45
R5 46
R6 47
R7 48
IOR 34
IOR# 33
GND

R7 75
R8 75
R9 75
GND

DSUB1
VGA-001
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HSYNC
VSYNC
GND

U6
74HCT541PW,118
VS_IN
HS_IN
OE1# VCC
A0 OE2#
A1 Y0
A2 Y1
A3 Y2
A4 Y3
A5 Y4
A6 Y5
A7 Y6
GND Y7
VSYNC
HSYNC
+5V
GND

24-bit VIDEO OUT

U4
AMS1117-2.5
In GND TAB Out
C12 100nF
C13 10uF/16V
+5V
2.5V
GND

U5
AMS1117-1.2
In GND TAB Out
C14 100nF
C15 10uF/16V
+5V
1.2V
GND

H3
Header 1x3
IEI_3v3
IEO
R11 2K2
R14 3K3
+5V
GND
INTERRUPT DAISY CHAIN INTERFACE

R10 4K7
IEO_3v3
R13 1K
Q1 2N3904
IEO DRIVER
+5V
GND

3.3V
R12 10K
BEEP
R15 2K
Q2 S8550G
R16 33R
LS1
AUDIO OUT

INT_REQ
R17 1K
Q3 2N3904-MMBT
INT
INTERRUPT DRIVER

PS_CLOCK
R21 470
10K
R19 10K
R18 10K
R20 470
PS_DATA
PS2 KEYBOARD
PS2 KEYBOARD

H4
Header 1x3
UART_TX
UART_RX
SERIAL

X1
50MHz
R23 33
FPGA_CLK
C16 100nF
RESET
R22 10K
C17 100nF
CRYSTAL and RESET

Micro_SD_Card_Holder;
DATA2
CS
DI
VDD
SCLK
VSS
DO
DATA1
SD_DI
SD_CLK
SD_DO
J1
SD Card

JTAG
Header 2x5
TCK
TDO
TMS
TDI
R24 1K
R25 10K
R26 10K
AS
Header 2x5
DCLK
CONF_DONE
nCONFIG
DATA
ASDO
nCE
nCSO
R27 10K
U7
EPCS16SI8N
DATA
R28 22
DCLK
nCSO
ASDO
nCS
ASDI
JTAG and AS

U8
74LVC245APW
EA_DIR
EA14
EA15
EA16
EA17
EA18
EA19
EA20
EA21
EA_OE
E14
E15
E16
E17
E18
E19
E20
E21
A<>B

U9
74LVC373APW
A7
AQ7
AQ6
A6
AQ5
A5
AQ4
A4
A0
AQ0
AQ1
A1
A2
AQ2
AQ3
A3

U10
74LVC245APW
245_DIR
D0
D1
D2
D3
D4
D5
D6
D7
245_OE
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
A<>B

U11
74LVC373APW
A15
AQ15
AQ14
A14
A13
AQ13
AQ12
A12
A8
AQ8
AQ9
A9
A10
AQ10
AQ11
A11

U12
74LVC245APW
Z80_RES
Z80_M1
Z80_IORQ
Z80_MREQ
Z80_WR
Z80_RD
Z80_CLK
Z80_INTA
H_RESET
M1_Q
IORQ_Q
MREQ_Q
WR_Q
RD_Q
H_CLK
INTACK_Q
A<B

LEVEL CONVERTERS

H1
Header 2x20
H2
Header 2x20
AQ0
AQ1
AQ2
AQ3
AQ4
AQ5
AQ6
AQ7
AQ8
AQ9
AQ10
AQ11
AQ12
AQ13
AQ14
AQ15
H_CLK
INTACK_Q
WR_Q
RD_Q
IORQ_Q
MREQ_Q
M1_Q
H_RESET
INT
EA13
EA14
EA15
EA16
EA17
EA18
EA19
EA20
EA21
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
C41 1uF
C11 1uF
+5V
3.3V
GND
SYSTEM HEADERS

C42 100nF
C43 100nF
C44 100nF
C45 100nF
C46 100nF
C47 100nF
C18 100nF
C19 100nF
C20 100nF
C21 100nF
C22 100nF
C23 100nF
C25 100nF
C26 100nF
C27 100nF
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 100nF
C33 100nF
C34 100nF
C35 100nF
C36 100nF
C37 100nF
C38 100nF
C39 100nF
C40 100nF
C24 100nF
3.3V
1.2V
2.5V
+5V
GND
GNDA1
GNDA2

TITLE: Cyclone IV EP4CE10 GPU
REV: 1.0
Company: 10103
Sheet: 1/1
Date: 2020-01-08
Drawn By: nockieboy
EasyEDA