CYCLONE V GPU SCHEMATICS

REVISIONS

1.0 - Initial draft
1.1 - Replaced MAX5101 DAC with PCM5101A. Replaced wire-wound chokes with fixed inductors.
1.2 - Added decoupling and supply isolation for TFP410.
1.3 - Removed decoupling and supply isolation for TFP410. Added external memory.
1.4 - 10u caps and 100k pull-downs added to audio DAC output. Fixed micro-SD pullups. Corrected DDR-RAM clock pins. Variable-voltage added to U19.
1.5 - Trimpot orientation fixed. VCCA fixed to 3.3VA. Protection diodes added to PS2 port. Links added for AS x1/x4 config. VCCPGM replaced with VCCIO. TFP410 powered from VCCIO.
1.6 - Removed VGA output and TFP410, replaced with tested & verified DVI/HDMI output.

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	Date: 2020-10-20 Drawn By: nockieboy	

Cyclone V FPGA

NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design.

U1.12
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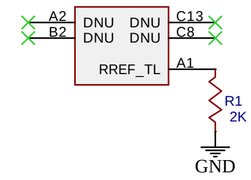

U1.1
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BANK 2A

IO,(DIFFIO_TX_L9p,DIFFOUT_L9p,DQ1L)	F4
IO,(DIFFIO_TX_L9n,DIFFOUT_L9n)	F3
IO,(DIFFIO_RX_L10p,DIFFOUT_L10p,DQ1L)	H3
IO,(DIFFIO_RX_L10n,DIFFOUT_L10n,DQ1L)	G3
IO,(DIFFIO_RX_L11p,DIFFOUT_L11p,DQS1L)	H5
IO,(DIFFIO_RX_L11n,DIFFOUT_L11n,DQSn1L)	H4
IO,(DIFFIO_TX_L12p,DIFFOUT_L12p)	F2
IO,(DIFFIO_TX_L12n,DIFFOUT_L12n,DQ1L)	E2
IO,(DIFFIO_TX_L13p,DIFFOUT_L13p,DQ1L)	G2
IO,(DIFFIO_TX_L13n,DIFFOUT_L13n,DQ1L)	G1
IO,(DIFFIO_RX_L14p,DIFFOUT_L14p,DQ1L)	J3
IO,(DIFFIO_RX_L14n,DIFFOUT_L14n,DQ1L)	J2
IO,(DIFFIO_RX_L15p,DIFFOUT_L15p)	K5
IO,(DIFFIO_RX_L15n,DIFFOUT_L15n)	K4
IO,(DIFFIO_TX_L16p,DIFFOUT_L16p,DQ1L)	J1
IO,(DIFFIO_TX_L16n,DIFFOUT_L16n,DQ1L)	H1

A1	
A2	
A8	
A6	
A10	
A9	
A3	
A0	
A5	
A4	
A13	
A12	
A15	
A14	
A11	
A7	

U1.2
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BANK 3A

IO,DATA8,(DIFFIO_RX_B1p,DIFFOUT_B1p,DQ1B)	P4
IO,DATA6,(DIFFIO_RX_B1n,DIFFOUT_B1n,DQ1B)	N4
IO,DATA7,(DIFFIO_TX_B2p,DIFFOUT_B2p,DQ1B)	P1
IO,DATA5,(DIFFIO_TX_B2n,DIFFOUT_B2n)	N1
IO,DATA12,(DIFFIO_RX_B3p,DIFFOUT_B3p,DQS1B)	L7
IO,DATA10,(DIFFIO_RX_B3n,DIFFOUT_B3n,DQSn1B)	M7
IO,DATA11,(DIFFIO_TX_B4p,DIFFOUT_B4p)	P2
IO,DATA9,(DIFFIO_TX_B4n,DIFFOUT_B4n,DQ1B)	R1
IO,CLKUSR,(DIFFIO_RX_B5p,DIFFOUT_B5p,DQ1B)	N3
IO,DATA14,(DIFFIO_RX_B5n,DIFFOUT_B5n,DQ1B)	P3
IO,DATA15,(DIFFIO_TX_B6p,DIFFOUT_B6p,DQ1B)	R2
IO,DATA13,(DIFFIO_TX_B6n,DIFFOUT_B6n,DQ1B)	T2
IO,PR_ERROR,(DIFFIO_RX_B7p,DIFFOUT_B7p)	P7
IO,PR_DONE,(DIFFIO_RX_B7n,DIFFOUT_B7n)	R6
IO,(DIFFIO_TX_B8p,DIFFOUT_B8p,DQ1B)	R4
IO,PR_READY,(DIFFIO_TX_B8n,DIFFOUT_B8n,DQ1B)	T3

E19	
E15	
E16	
E14	
EA_DIR	
EA_OE	
E17	
E20	
E18	
E21	
PS2_MCLK	
PS2_KCLK	
PS2_KDAT	
PS2_MDAT	

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BANK 6B

IO,(DIFFIO_TX_B17p,DIFFOUT_B17p,DQ2B)	T4
IO,(DIFFIO_TX_B17n,DIFFOUT_B17n)	T5
IO,(DIFFIO_RX_B18p,DIFFOUT_B18p,DQ2B)	P8
IO,(DIFFIO_RX_B18n,DIFFOUT_B18n,DQ2B)	R7
IO,(DIFFIO_RX_B19p,DIFFOUT_B19p,DQS2B)	L9
IO,(DIFFIO_RX_B19n,DIFFOUT_B19n,DQSn2B)	M8
IO,(DIFFIO_TX_B20p,DIFFOUT_B20p)	T8
IO,(DIFFIO_TX_B20n,DIFFOUT_B20n,DQ2B)	T7
IO,FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB,(DIFFIO_TX_B21p,DIFFOUT_B21p,DQ2B)	R12
IO,FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn,(DIFFIO_TX_B21n,DIFFOUT_B21n,DQ2B)	R11
IO,(DIFFIO_RX_B22p,DIFFOUT_B22p,DQ2B)	T13
IO,(DIFFIO_RX_B22n,DIFFOUT_B22n,DQ2B)	T12
IO,CLK1p,(DIFFIO_RX_B23p,DIFFOUT_B23p)	P9
IO,CLK1n,(DIFFIO_RX_B23n,DIFFOUT_B23n)	R9
IO,(DIFFIO_TX_B24p,DIFFOUT_B24p,DQ2B)	R10
IO,(DIFFIO_TX_B24n,DIFFOUT_B24n,DQ2B)	T10

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BANK 4A

IO,(DIFFIO_TX_B25p,DIFFOUT_B25p,DQ3B)	P16
IO,RZQ_0,(DIFFIO_TX_B25n,DIFFOUT_B25n)	R15
IO,(DIFFIO_RX_B26p,DIFFOUT_B26p,DQ3B)	R16
IO,(DIFFIO_RX_B26n,DIFFOUT_B26n,DQ3B)	T15
IO,(DIFFIO_RX_B27p,DIFFOUT_B27p,DQS3B)	L10
IO,(DIFFIO_RX_B27n,DIFFOUT_B27n,DQSn3B)	M10
IO,(DIFFIO_TX_B28p,DIFFOUT_B28p)	N14
IO,(DIFFIO_TX_B28n,DIFFOUT_B28n,DQ3B)	M13
IO,(DIFFIO_TX_B29p,DIFFOUT_B29p,DQ3B)	P13
IO,(DIFFIO_TX_B29n,DIFFOUT_B29n,DQ3B)	P14
IO,(DIFFIO_RX_B30p,DIFFOUT_B30p,DQ3B)	M11
IO,(DIFFIO_RX_B30n,DIFFOUT_B30n,DQ3B)	M12
IO,CLK2p,(DIFFIO_RX_B31p,DIFFOUT_B31p)	N11
IO,CLK2n,(DIFFIO_RX_B31n,DIFFOUT_B31n)	P11
IO,(DIFFIO_TX_B32p,DIFFOUT_B32p,DQ3B)	R14
IO,(DIFFIO_TX_B32n,DIFFOUT_B32n,DQ3B)	T14

P16	
R15	
R16	
T15	
L10	
Z80_INTAK	
N14	
M13	
P13	
P14	
M11	
M12	
Z80_nCLK	
P11	
R14	
T14	

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BANK 5A

IO,RZQ_1,(DIFFIO_TX_R1p,DIFFOUT_R1p,DQ1R)	N15
IO,PR_REQUEST,(DIFFIO_TX_R1n,DIFFOUT_R1n,DQ1R)	N16
IO,INIT_DONE,(DIFFIO_RX_R2p,DIFFOUT_R2p)	L13
IO,CRC_ERROR,(DIFFIO_RX_R2n,DIFFOUT_R2n)	K14
IO,nCEO,(DIFFIO_TX_R3p,DIFFOUT_R3p,DQ1R)	H16
IO,CvP_CONFDONE,(DIFFIO_TX_R3n,DIFFOUT_R3n,DQ1R)	J16
IO,(DIFFIO_RX_R4p,DIFFOUT_R4p,DQ1R)	L14
IO,(DIFFIO_RX_R4n,DIFFOUT_R4n,DQ1R)	L15
IO,DEV_OE,(DIFFIO_TX_R5p,DIFFOUT_R5p)	G15
IO,DEV_CLRn,(DIFFIO_TX_R5n,DIFFOUT_R5n,DQ1R)	G16
IO,(DIFFIO_RX_R6p,DIFFOUT_R6p,DQS1R)	K12
IO,(DIFFIO_RX_R6n,DIFFOUT_R6n,DQSn1R)	J12
IO,(DIFFIO_TX_R7p,DIFFOUT_R7p,DQ1R)	J14
IO,(DIFFIO_TX_R7n,DIFFOUT_R7n)	H15
IO,(DIFFIO_RX_R8p,DIFFOUT_R8p,DQ1R)	K15
IO,(DIFFIO_RX_R8n,DIFFOUT_R8n,DQ1R)	K16

Z80_nRD	
Z80_nWR	
Z80_nM1	
D7	
D1	
D4	
Z80_nMREQ	
Z80_nIORQ	
245_OE	
245_DIR	
Z80_nRES	
D2	
D3	
D0	
D6	
D5	

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BANK 5B

IO,CLK6p,(DIFFIO_RX_R9p,DIFFOUT_R9p)	F12
IO,CLK6n,(DIFFIO_RX_R9n,DIFFOUT_R9n)	G12
IO,(DIFFIO_TX_R10p,DIFFOUT_R10p,DQ2R)	E16
IO,(DIFFIO_TX_R10n,DIFFOUT_R10n,DQ2R)	D16
IO,(DIFFIO_RX_R11p,DIFFOUT_R11p,DQ2R)	E12
IO,(DIFFIO_RX_R11n,DIFFOUT_R11n,DQ2R)	D13
IO,FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB,(DIFFIO_TX_R12p,DIFFOUT_R12p,DQ2R)	B16
IO,FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn,(DIFFIO_TX_R12n,DIFFOUT_R12n,DQ2R)	C16
IO,(DIFFIO_RX_R13p,DIFFOUT_R13p,DQS2R)	H13
IO,(DIFFIO_RX_R13n,DIFFOUT_R13n,DQSn2R)	G13
IO,(DIFFIO_TX_R14p,DIFFOUT_R14p)	B15
IO,(DIFFIO_TX_R14n,DIFFOUT_R14n,DQ2R)	C15
IO,(DIFFIO_RX_R15p,DIFFOUT_R15p,DQ2R)	F14
IO,(DIFFIO_RX_R15n,DIFFOUT_R15n,DQ2R)	F15
IO,(DIFFIO_TX_R16p,DIFFOUT_R16p,DQ2R)	D14
IO,(DIFFIO_TX_R16n,DIFFOUT_R16n)	E15

DDR1_CSn	
DDR2_CSn	
DDR_D7	
DDR_D1	
DDR_D2	
DDR_D4	
DDR_CK+	
DDR_CK-	
DDR_RWDS	
DDR_RST	
DDR_D0	
DDR_D5	
DDR_D6	
DDR_D3	

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BANK 7A

IO,CLK10p,(DIFFIO_RX_T17p,DIFFOUT_T17p)	F11
IO,CLK10n,(DIFFIO_RX_T17n,DIFFOUT_T17n)	F10
IO,(DIFFIO_TX_T18p,DIFFOUT_T18p,DQ1T)	A15
IO,(DIFFIO_TX_T18n,DIFFOUT_T18n,DQ1T)	A14
IO,(DIFFIO_RX_T19p,DIFFOUT_T19p,DQ1T)	D11
IO,(DIFFIO_RX_T19n,DIFFOUT_T19n,DQ1T)	C11
IO,(DIFFIO_TX_T20p,DIFFOUT_T20p,DQ1T)	A13
IO,(DIFFIO_TX_T20n,DIFFOUT_T20n,DQ1T)	A12
IO,(DIFFIO_RX_T21p,DIFFOUT_T21p,DQS1T)	E10
IO,(DIFFIO_RX_T21n,DIFFOUT_T21n,DQSn1T)	E9
IO,(DIFFIO_TX_T22p,DIFFOUT_T22p)	B12
IO,(DIFFIO_TX_T22n,DIFFOUT_T22n,DQ1T)	B11
IO,(DIFFIO_RX_T23p,DIFFOUT_T23p,DQ1T)	C10
IO,(DIFFIO_RX_T23n,DIFFOUT_T23n,DQ1T)	C9
IO,(DIFFIO_TX_T24p,DIFFOUT_T24p,DQ1T)	B10
IO,RZQ_2,(DIFFIO_TX_T24n,DIFFOUT_T24n)	A10

CLKUSR	
A_LRCK	
A_DIN	
A_BCK	

U1.8
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BANK 8A

IO,CLK9p,(DIFFIO_RX_T25p,DIFFOUT_T25p)	F8
IO,CLK9n,(DIFFIO_RX_T25n,DIFFOUT_T25n)	F7
IO,(DIFFIO_TX_T26p,DIFFOUT_T26p,DQ2T)	A8
IO,(DIFFIO_TX_T26n,DIFFOUT_T26n,DQ2T)	A9
IO,(DIFFIO_RX_T27p,DIFFOUT_T27p,DQ2T)	B8
IO,(DIFFIO_RX_T27n,DIFFOUT_T27n,DQ2T)	A7
IO,FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB,(DIFFIO_TX_T28p,DIFFOUT_T28p,DQ2T)	A5
IO,FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn,(DIFFIO_TX_T28n,DIFFOUT_T28n,DQ2T)	A4
IO,(DIFFIO_RX_T29p,DIFFOUT_T29p,DQS2T)	D8
IO,(DIFFIO_RX_T29n,DIFFOUT_T29n,DQSn2T)	D7
IO,(DIFFIO_TX_T30p,DIFFOUT_T30p)	B3
IO,(DIFFIO_TX_T30n,DIFFOUT_T30n,DQ2T)	A3
IO,(DIFFIO_RX_T31p,DIFFOUT_T31p,DQ2T)	B7
IO,(DIFFIO_RX_T31n,DIFFOUT_T31n,DQ2T)	B6
IO,(DIFFIO_TX_T32p,DIFFOUT_T32p,DQ2T)	C3
IO,(DIFFIO_TX_T32n,DIFFOUT_T32n)	C4

PC_RTS	
PC_RXD	
PC_TXD	
UART_RX	
PC_CTS	
SD_D0	
SD_CLK	
UART_TX	
SD_D3	
IOR	
SD_D1	
SD_D2	
SD_CMD	
IOB	
IOG	

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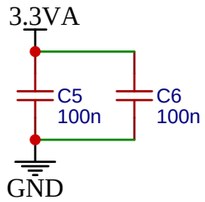
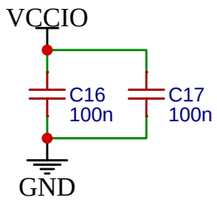
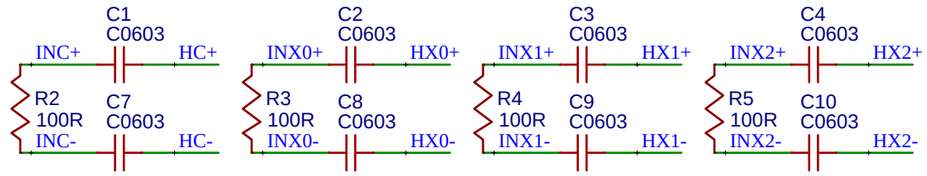
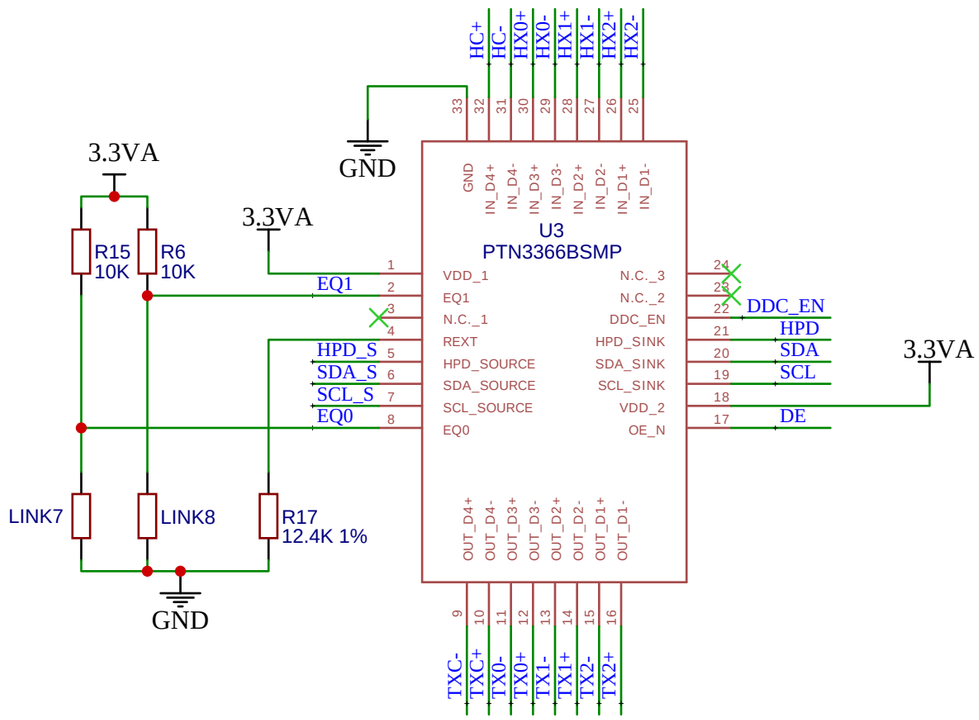
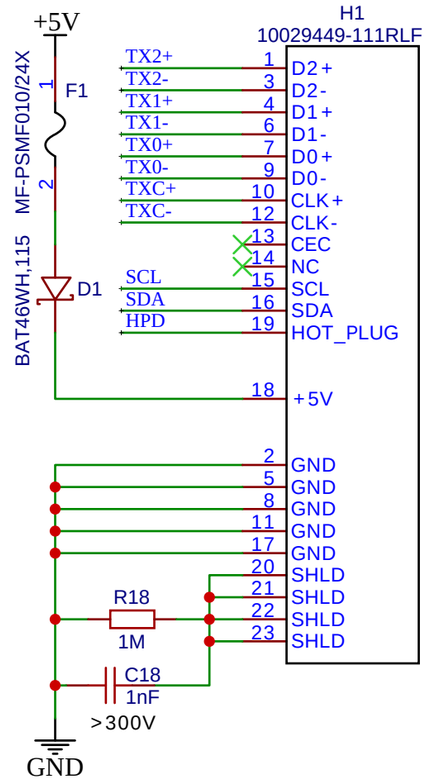
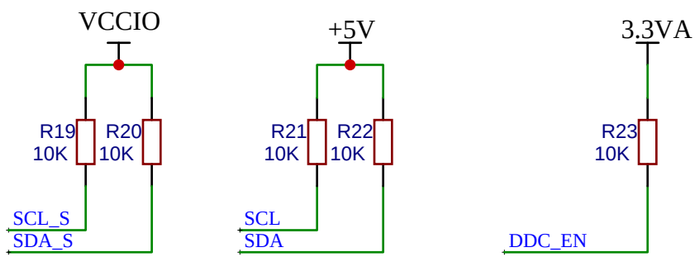








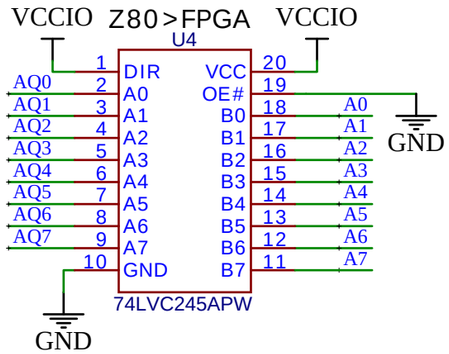


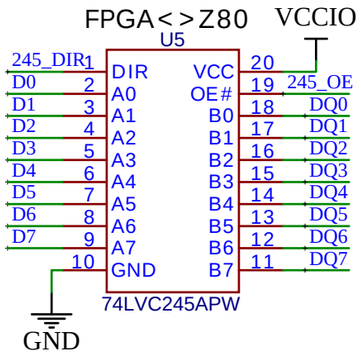


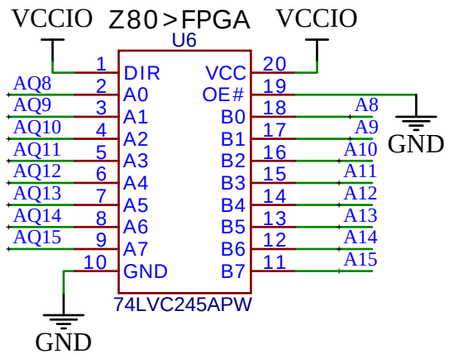
EQ0	EQ1	Equalization 3 Gbit/s
GND	GND	0 dB
Vdd	GND	2 dB
GND	Vdd	4 dB
Vdd	Vdd	6 dB

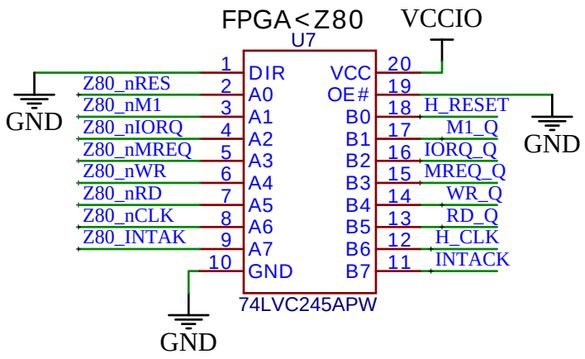
TITLE: DVI Output		REV: 1.6
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-11-13 Drawn By: nockieboy	

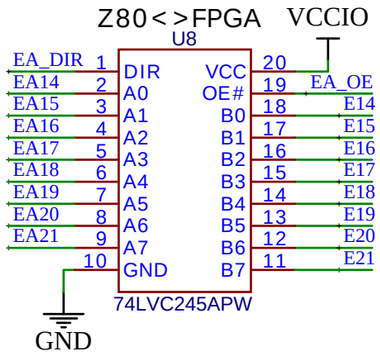
5V<->3.3V SYSTEM BUS CONVERTERS

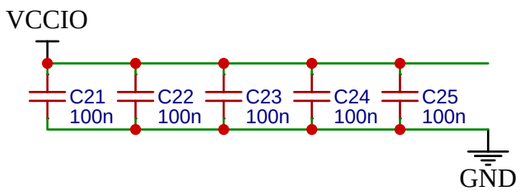


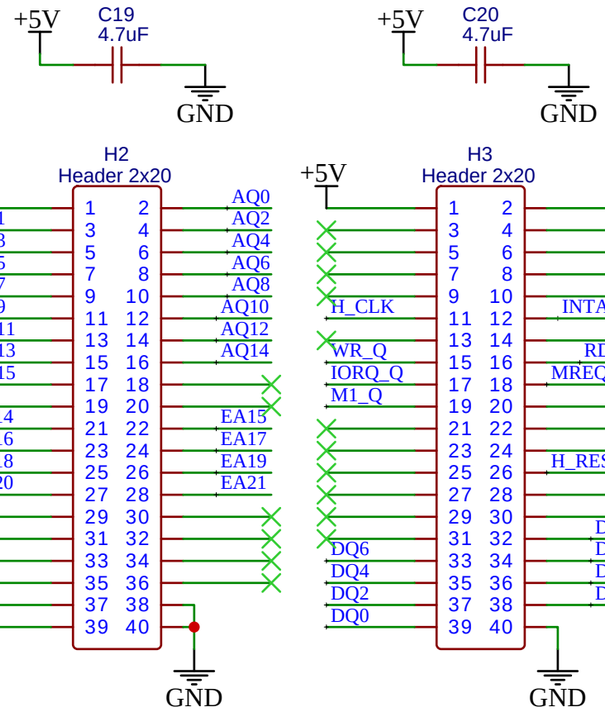












SYSTEM BUS HEADERS

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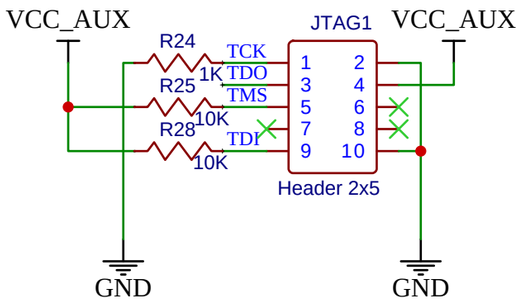
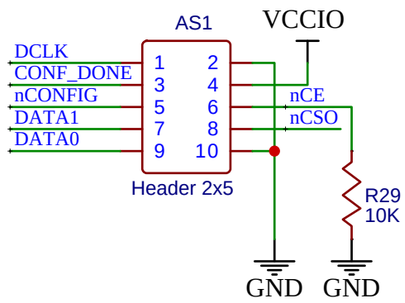
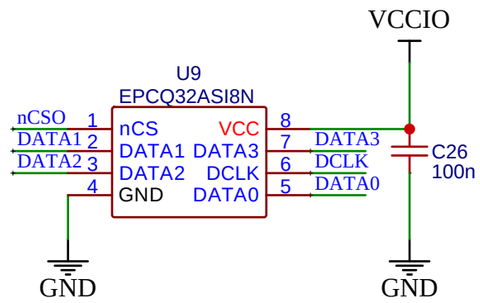
CLOCK & FPGA CONFIGURATION



JTAG HEADER

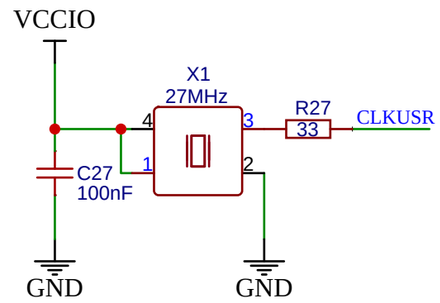


AS HEADER

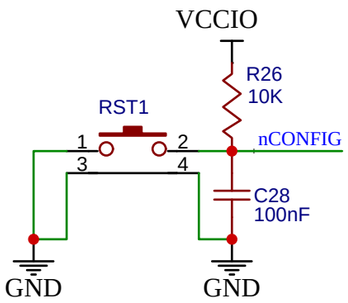


CONFIG EEPROM

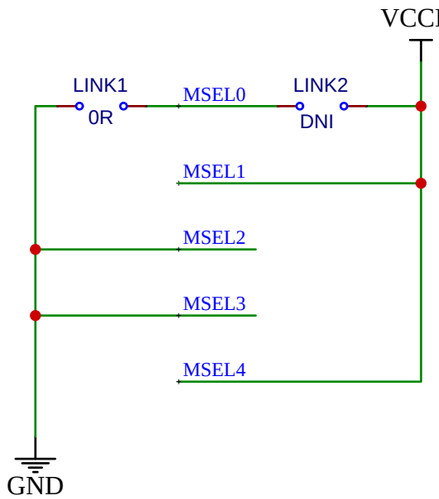
* Minimum 32Mbit EEPROM required for 21Mbit image

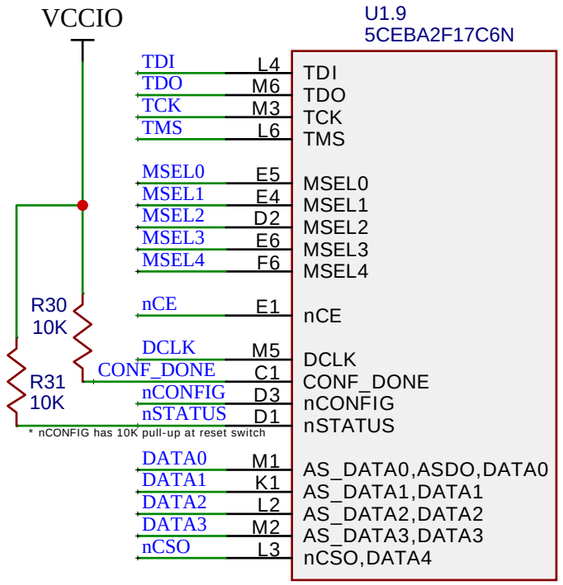


27 MHz CLOCK



FPGA RESET





AS FAST (x4) 10010 configuration @ 3.3V with J2 pins 1-2 connected.
AS STANDARD (x1) 10011 configuration @ 3.3V with J2 pins 2-3 connected.

'MSEL Pin Settings' 7-2 in Cyclone V Device Handbook Volume 1: Device Interfaces and Integration

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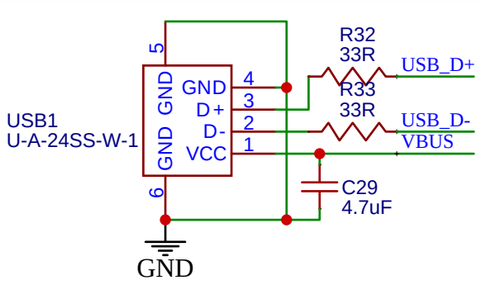
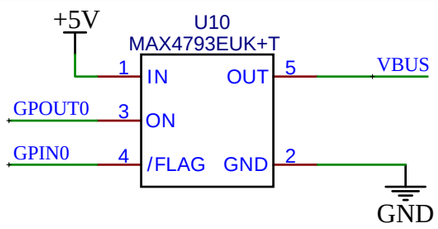
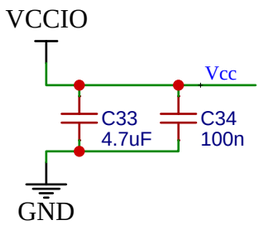
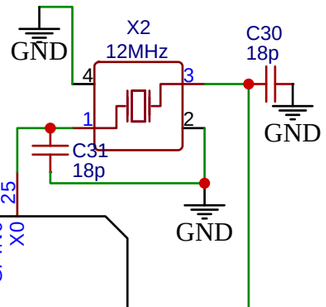
	Date: 2020-06-25 Drawn By: nockieboy	

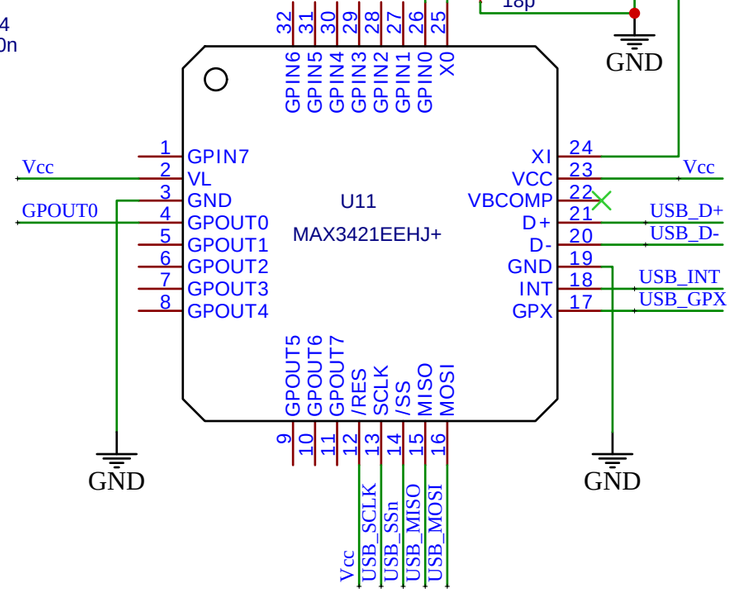
PERIPHERALS

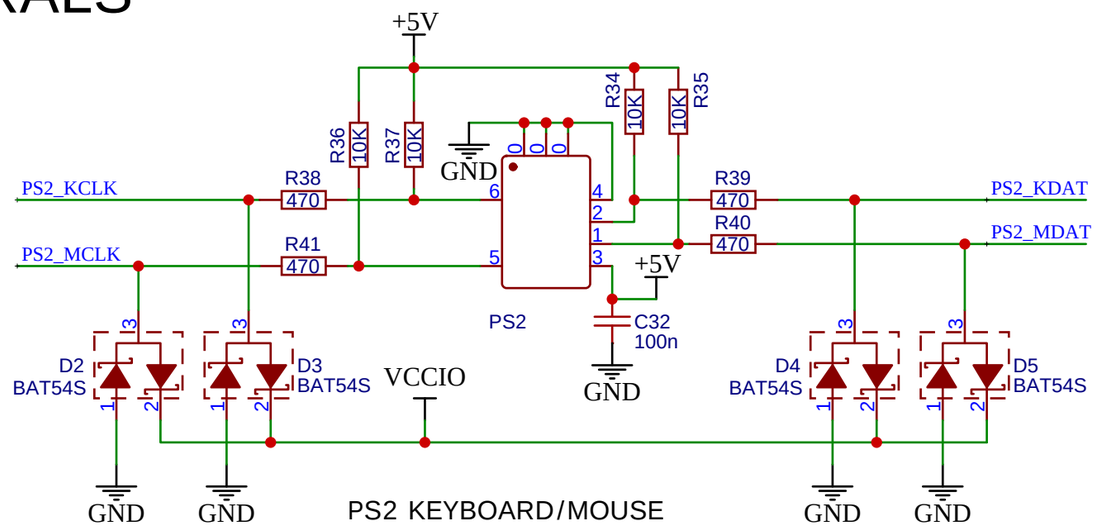


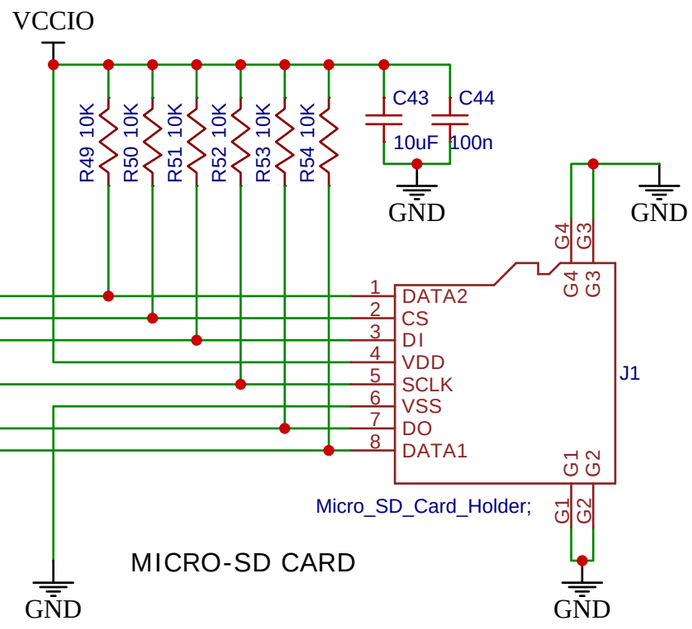


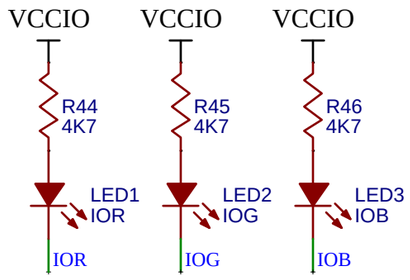


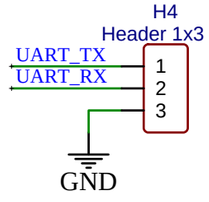


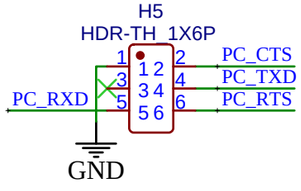












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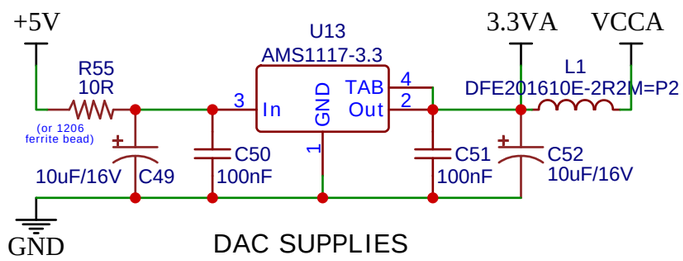
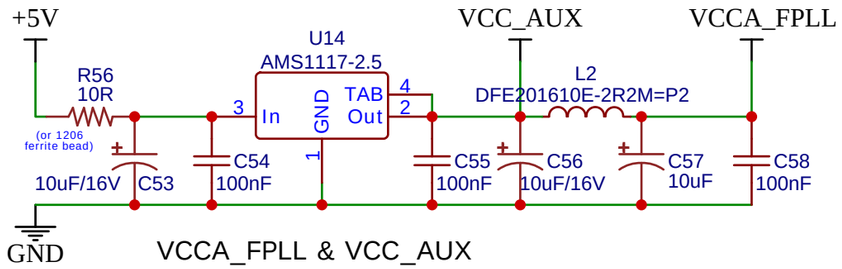
POWER SUPPLIES

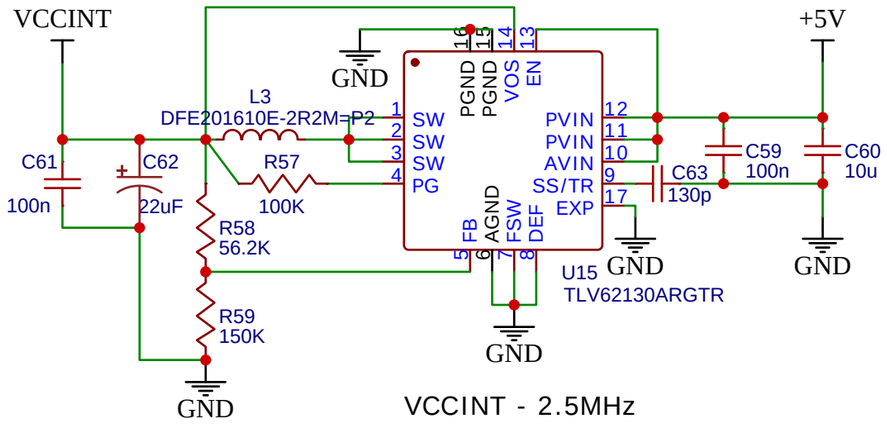


DAC SUPPLIES

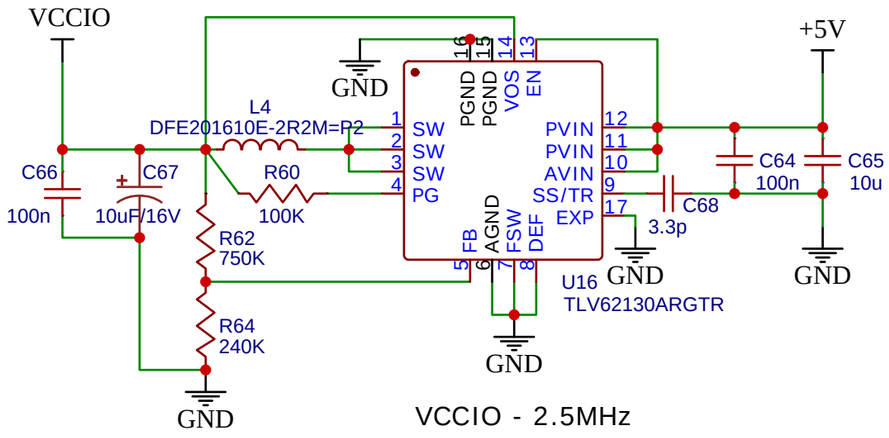


VCCA_FPLL & VCC_AUX

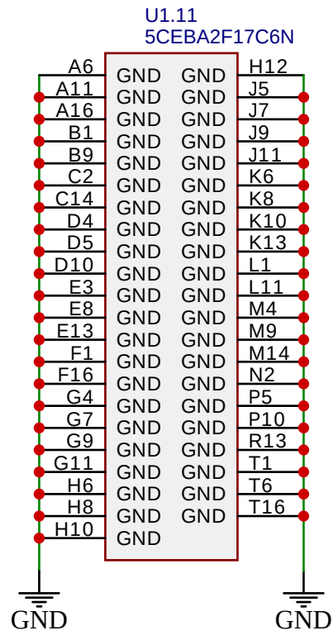
DESIGN NOTE: All 10uF/22uF components are SMD 3216 tantalum caps.

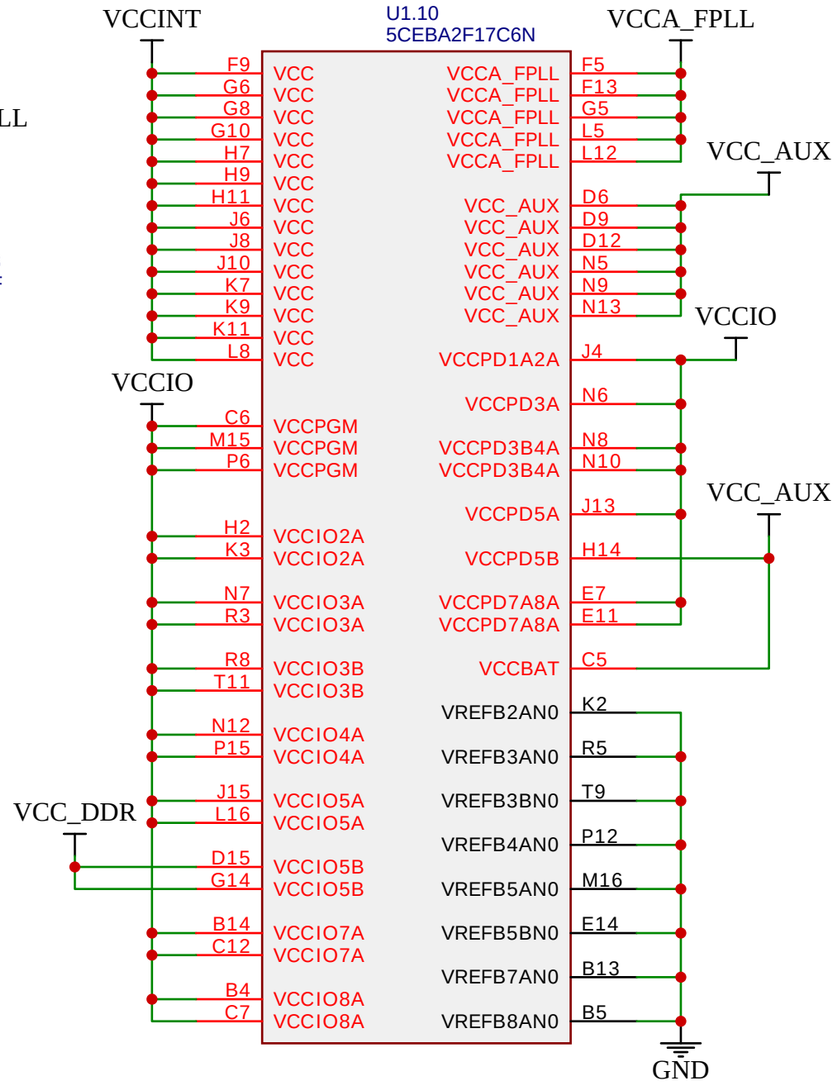


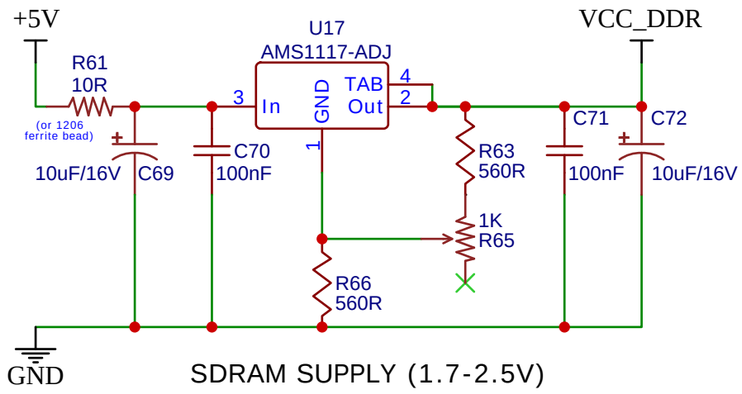
VCCINT - 2.5MHz



VCCIO - 2.5MHz







SDRAM SUPPLY (1.7-2.5V)

Supplies:
- U13 - 3.3V supply (3.3VA, VCCA)
- U14 - 2.5V supply (VCCA_FPLL, VCC_AUX)
- U15 - 1.1V supply (VCCINT)
- U16 - 3.3V supply (VCCIO)
- U19 - 1.8-2.5V supply (VCC_DDR)

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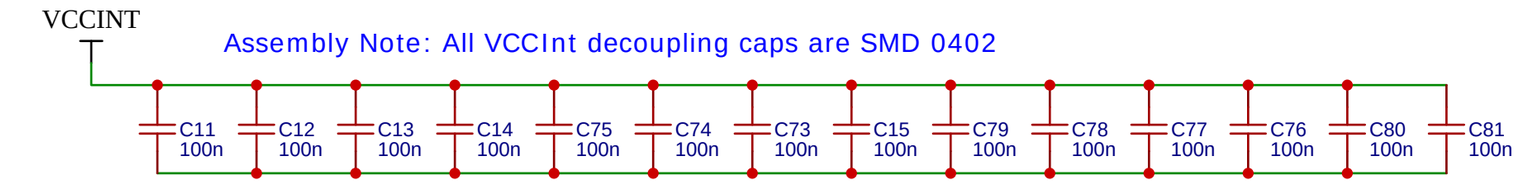
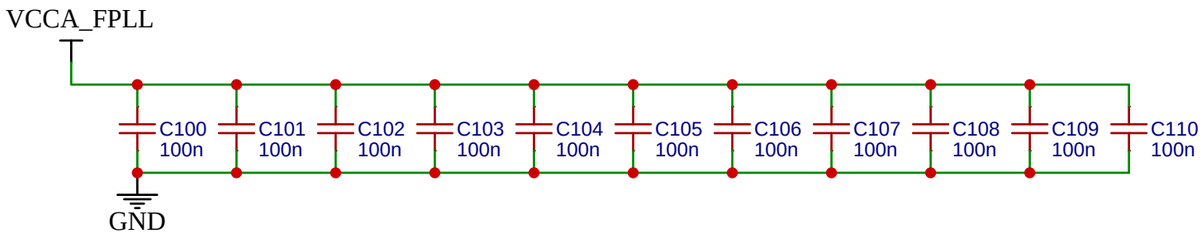
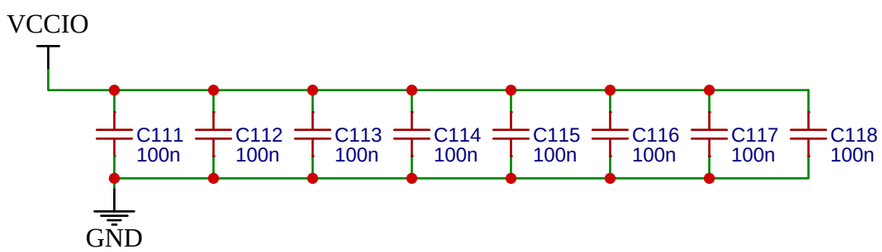
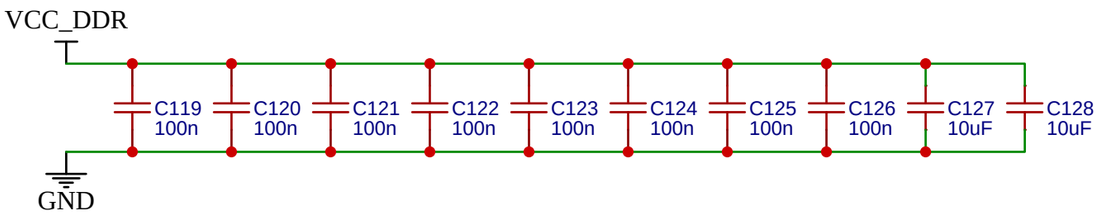
FPGA DECOUPLING

Note: Place capacitors near FPGA pins



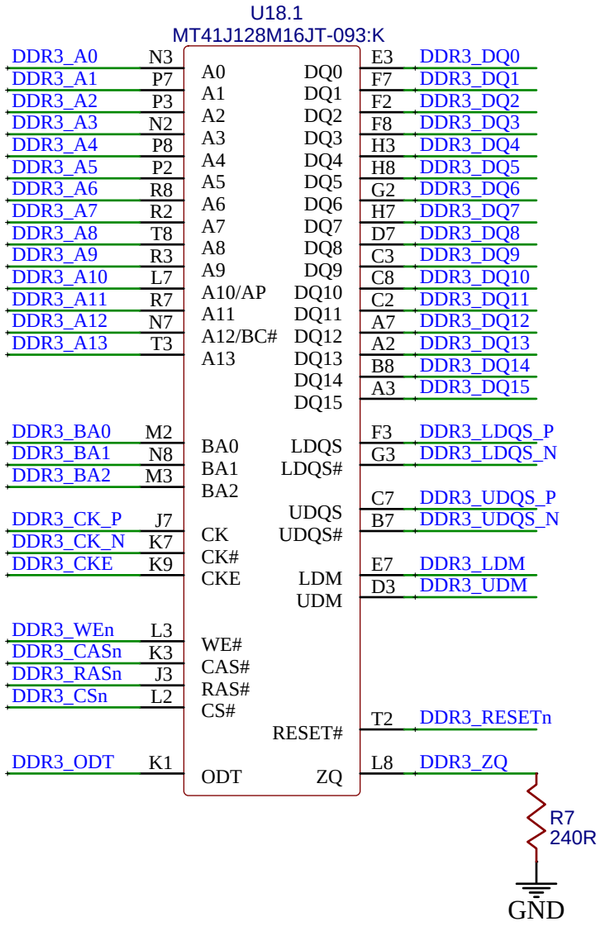


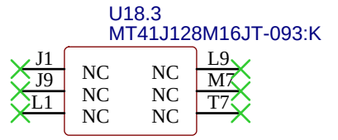


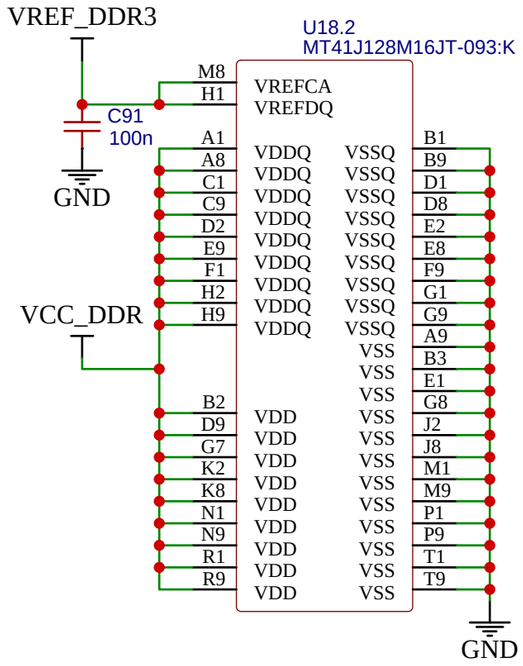


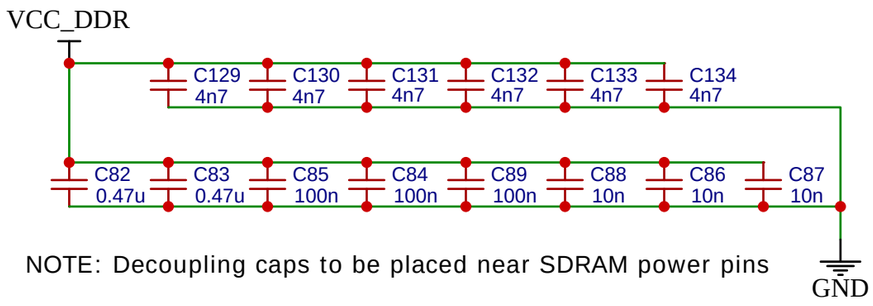
TITLE: Cyclone V GPU		REV: 1.6
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-10-20 Drawn By: nockieboy	

FPGA EXTERNAL MEMORY









NOTE: Decoupling caps to be placed near SDRAM power pins

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