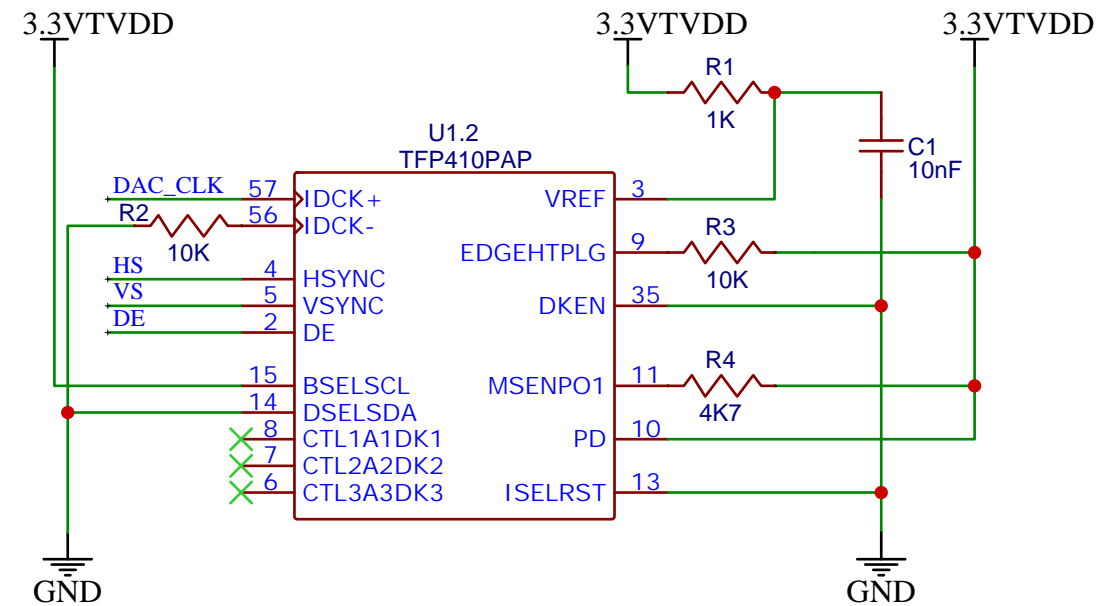
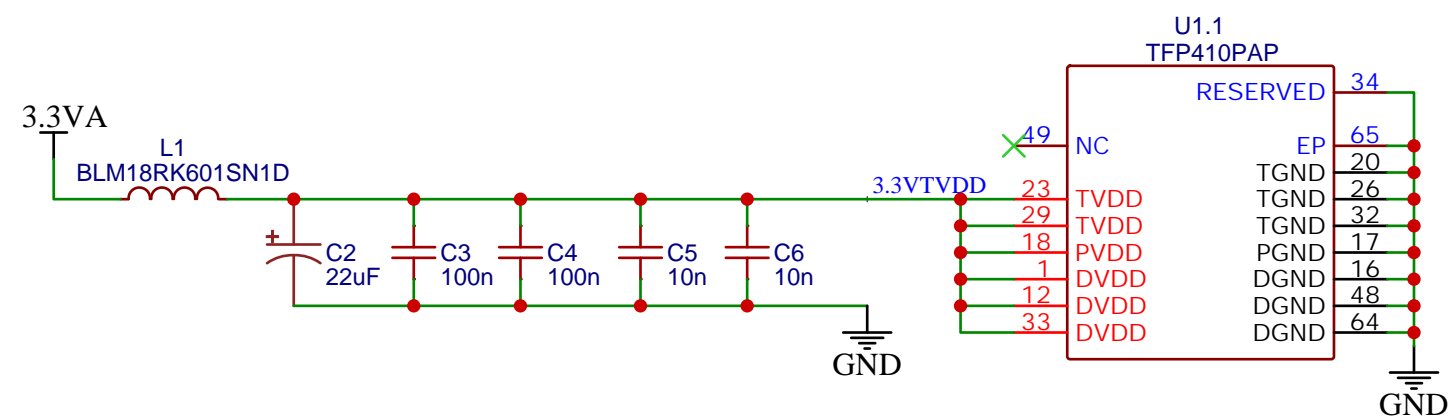


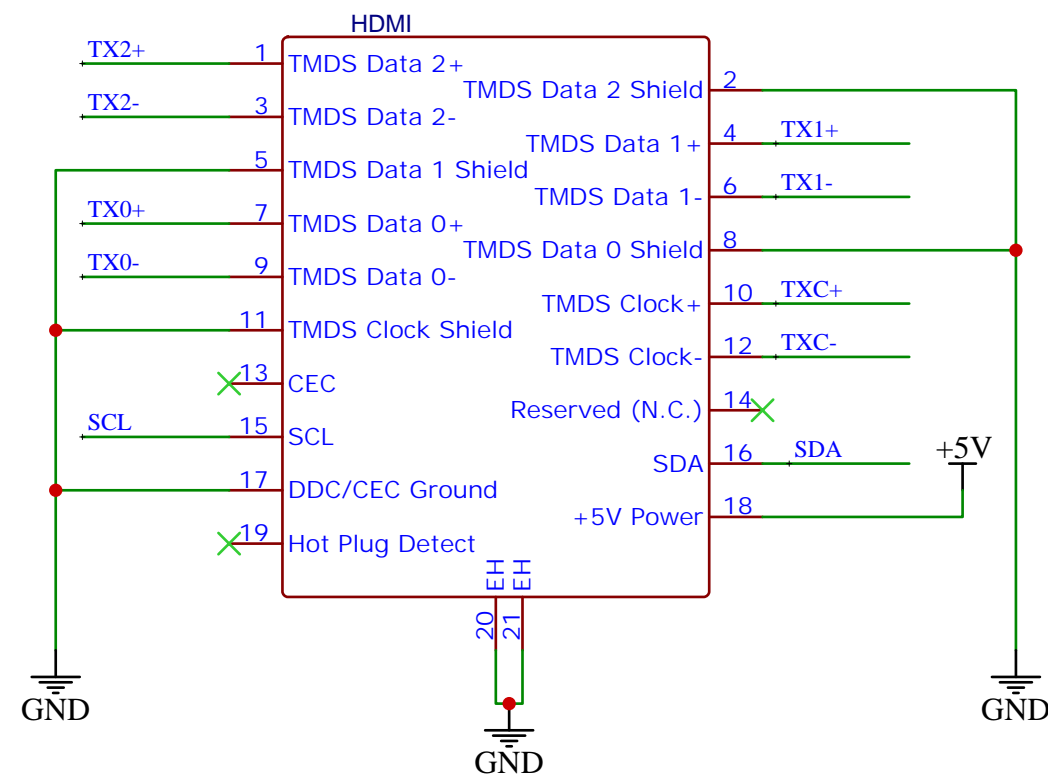
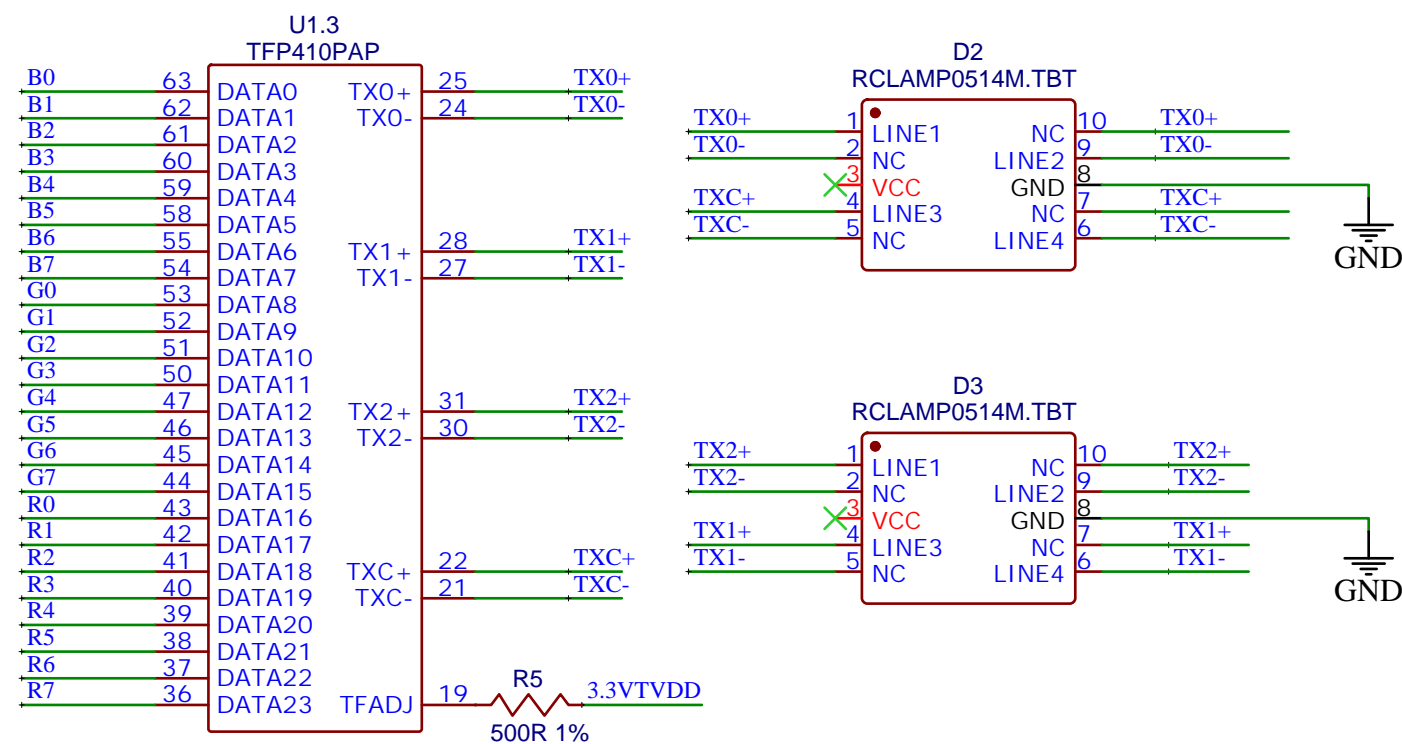
# CYCLONE V GPU SCHEMATICS

PAGE	CONTENT
1.	INDEX
2.	DVI OUTPUT
3.	VGA OUTPUT
4.	5V TO 3.3V BUS CONVERSION
5.	CLOCK & FPGA CONFIGURATION
6.	FPGA CONNECTIONS
7.	GPU BOARD PERIPHERALS
8.	POWER SUPPLIES
9.	DECOUPLING

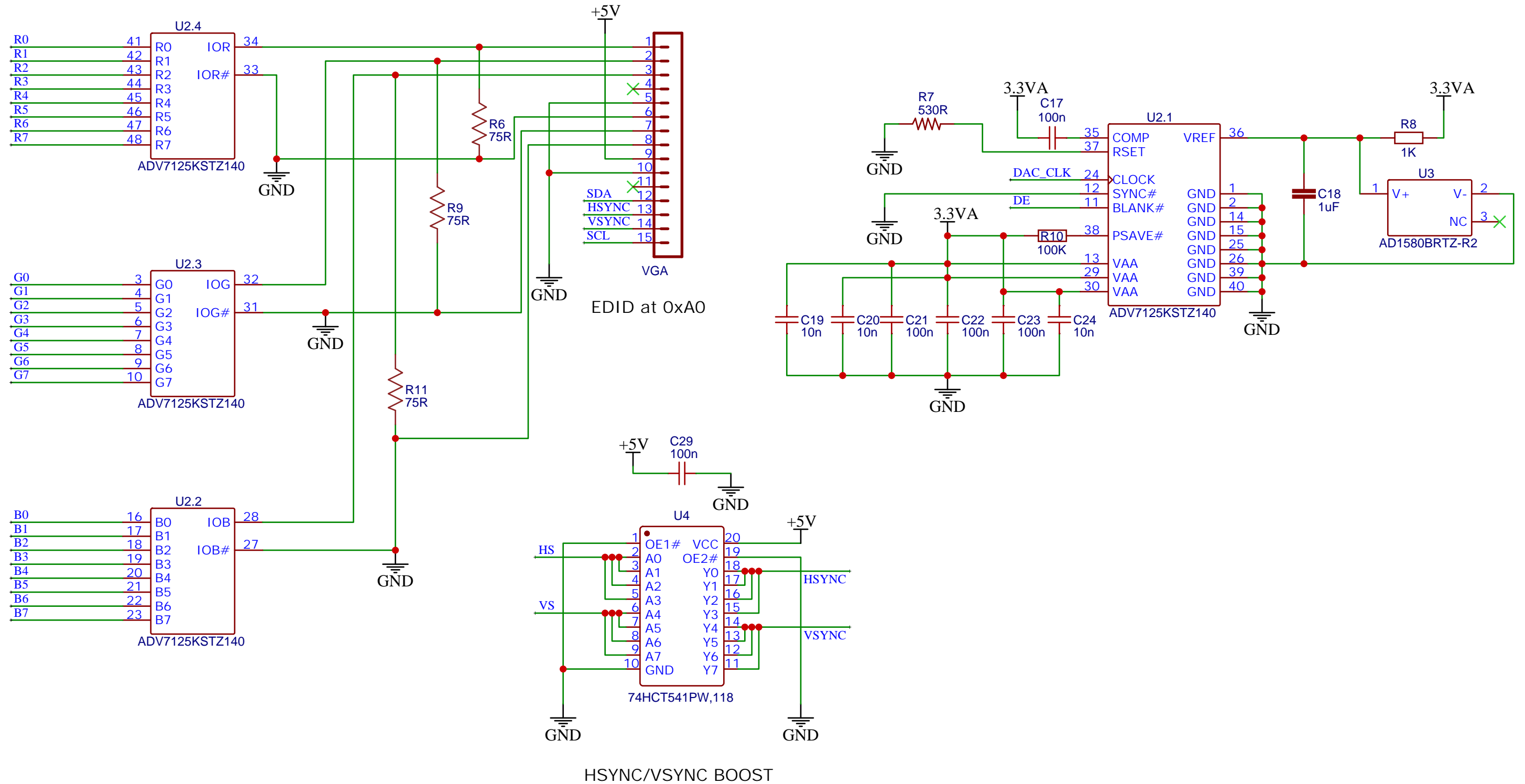
# 24-bit DVI VIDEO OUTPUT



Width 24-bit Latch Mode Single-edge Edge Rising Clock Mode Single-ended

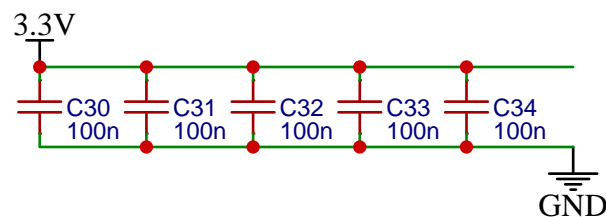
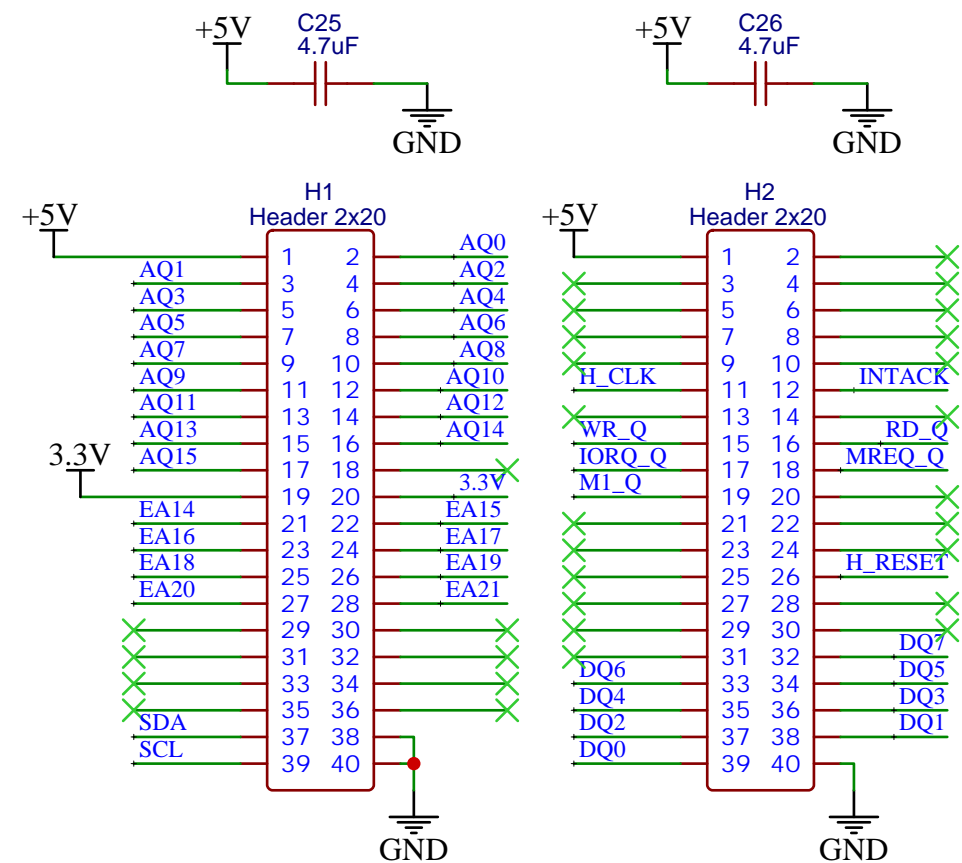
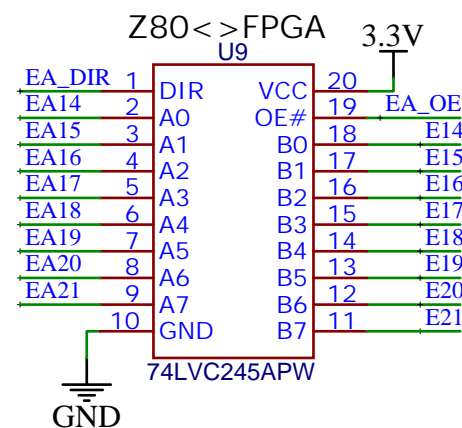
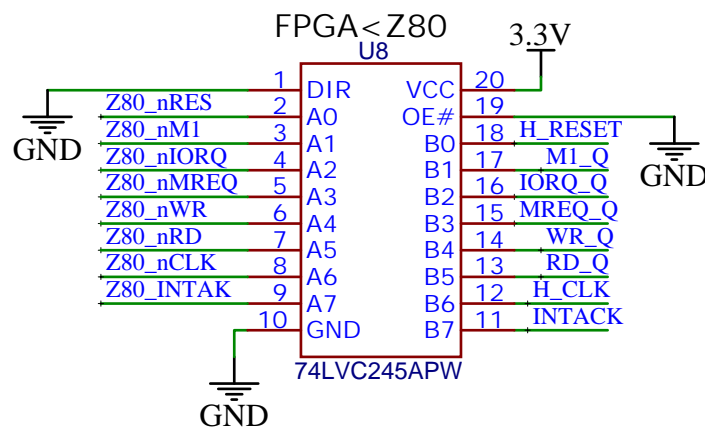
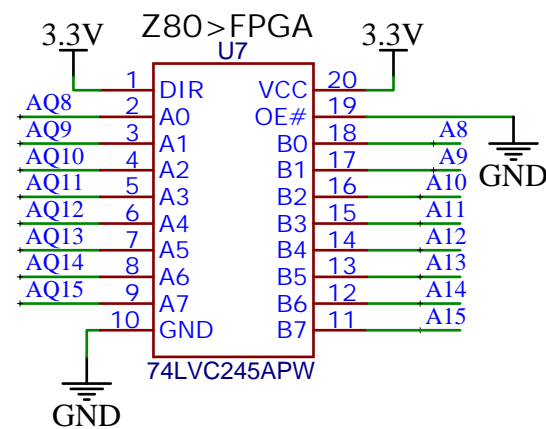
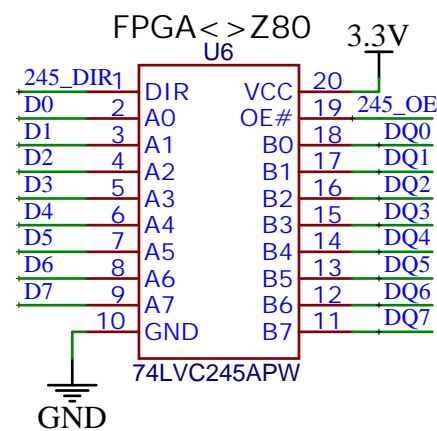
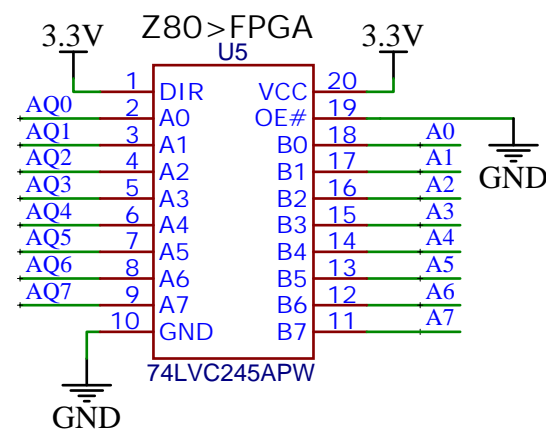


# 24-bit VGA VIDEO OUTPUT

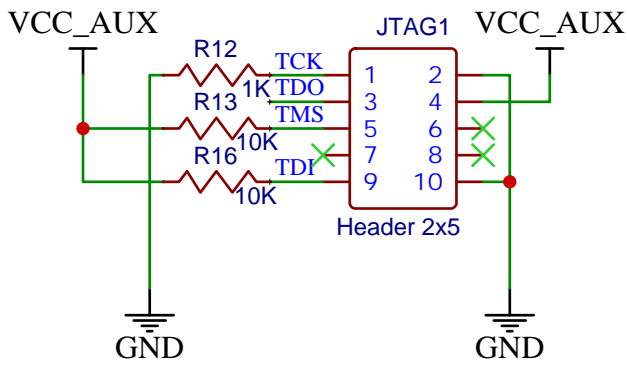


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EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-08-23	Drawn By: nockieboy

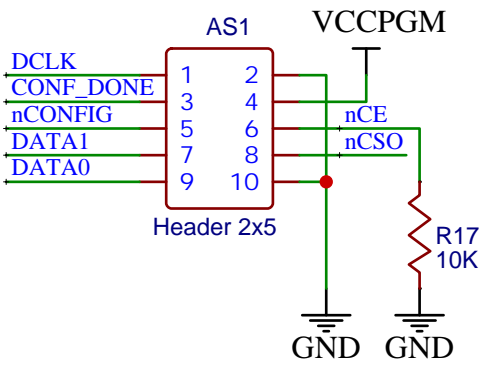
# 5V<->3.3V SYSTEM BUS CONVERTERS



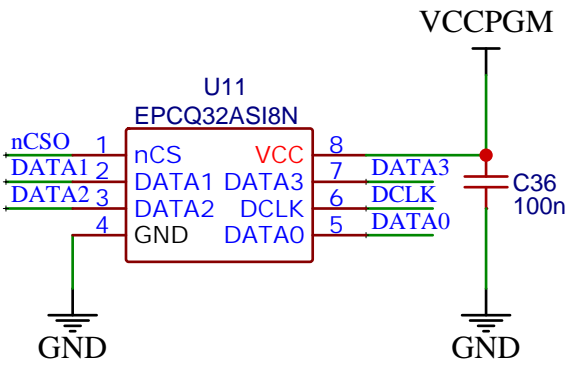
# CLOCK & FPGA CONFIGURATION



JTAG HEADER

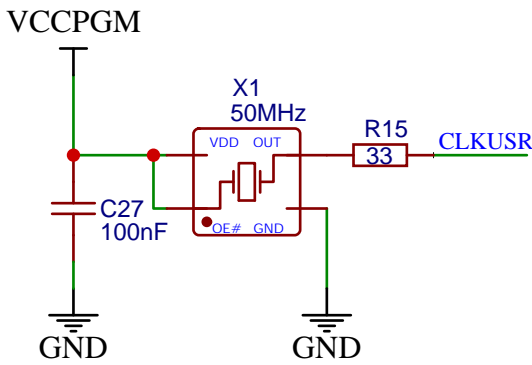


AS HEADER

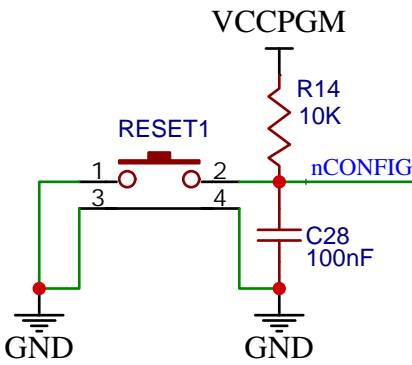


CONFIG EEPROM

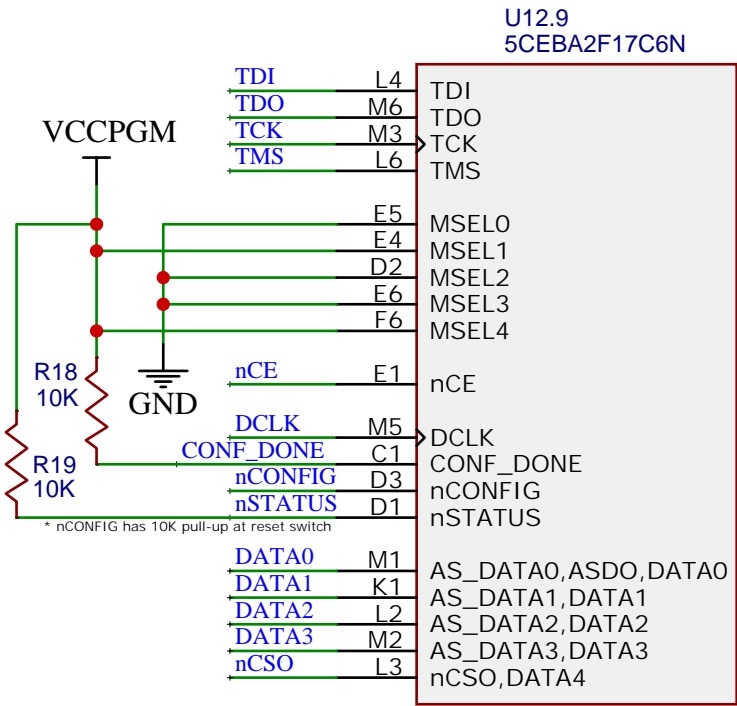
\* Minimum 32Mbit EEPROM required for 21Mbit image



50 MHz CLOCK



FPGA RESET

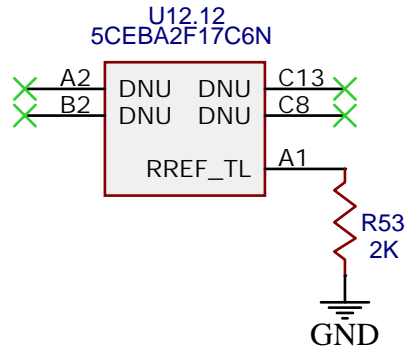
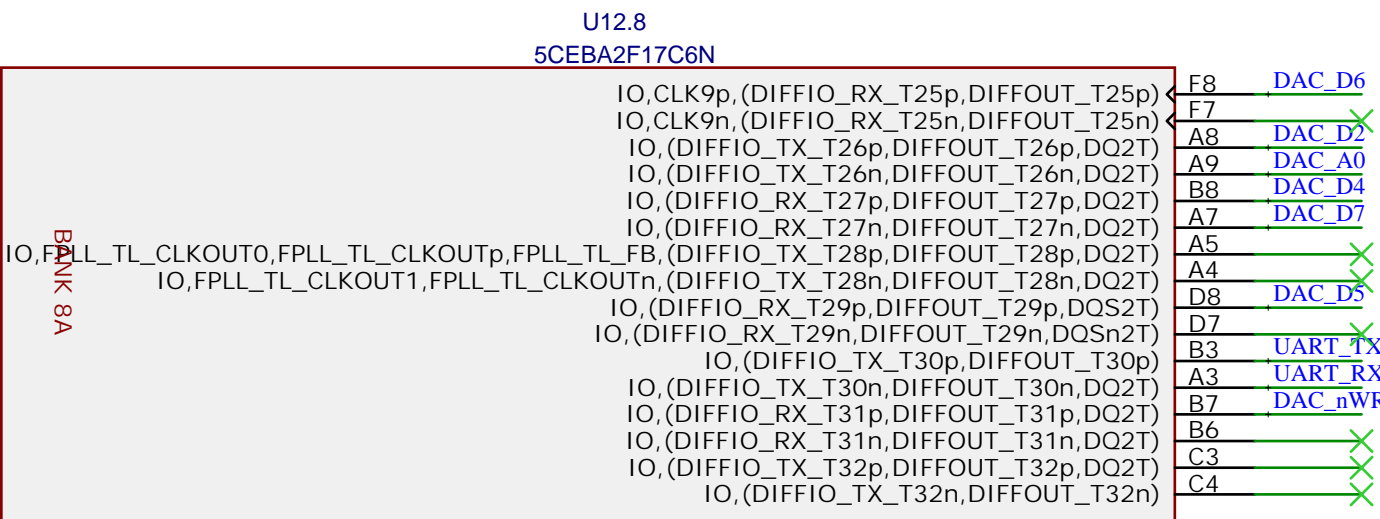
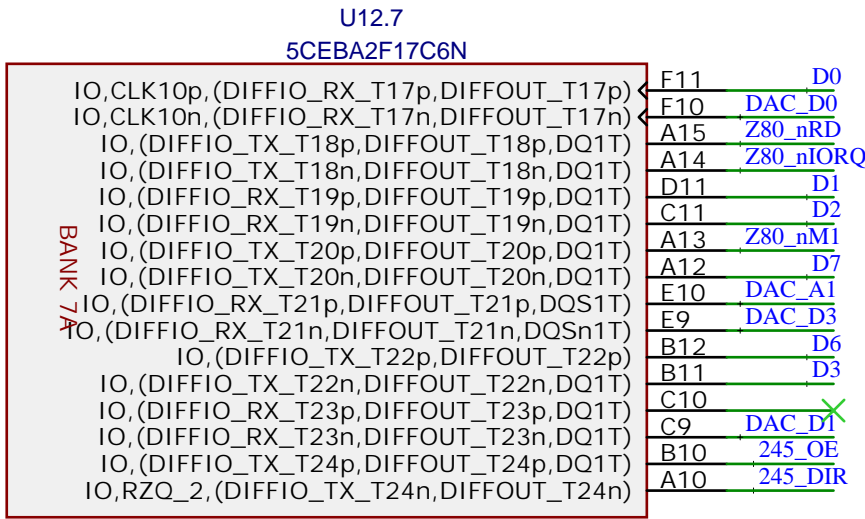
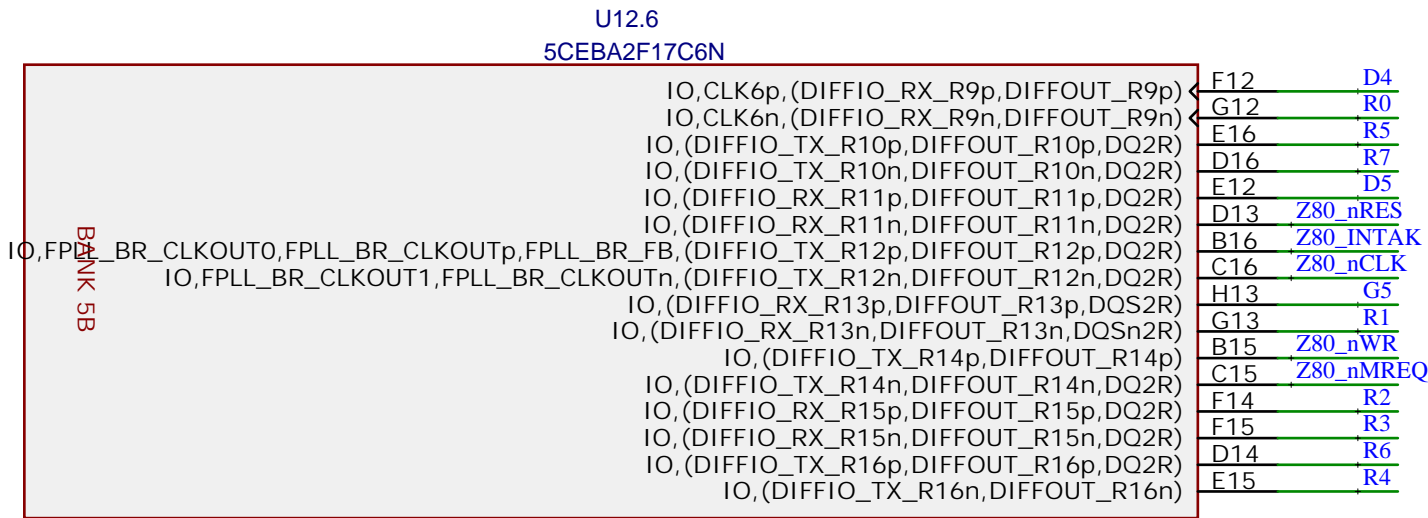
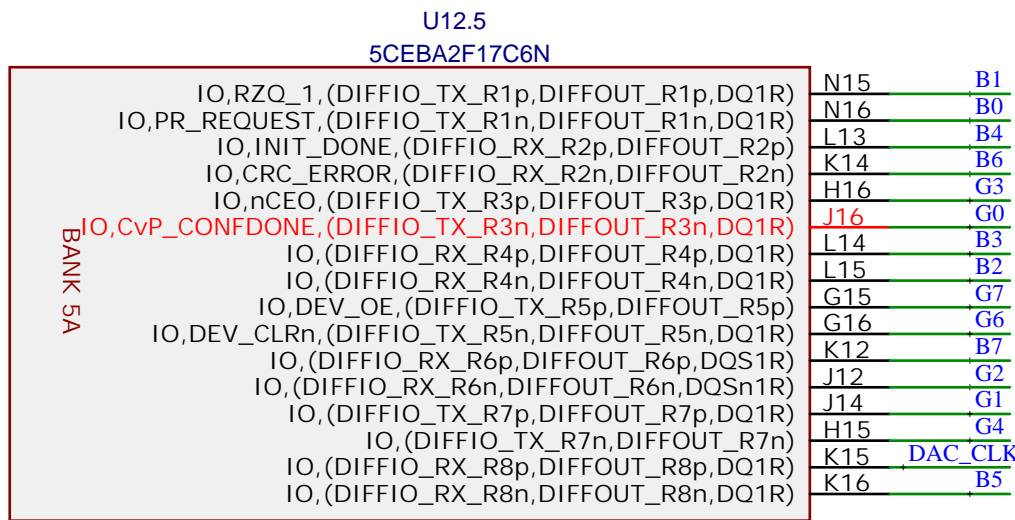
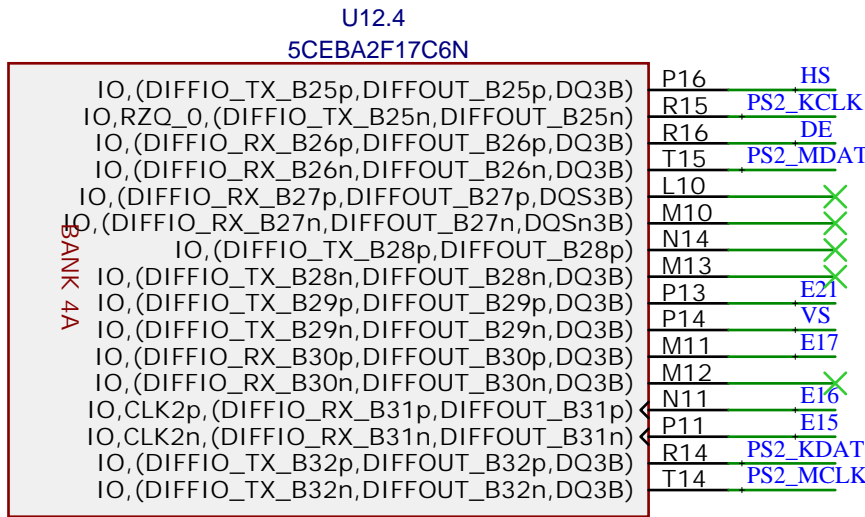
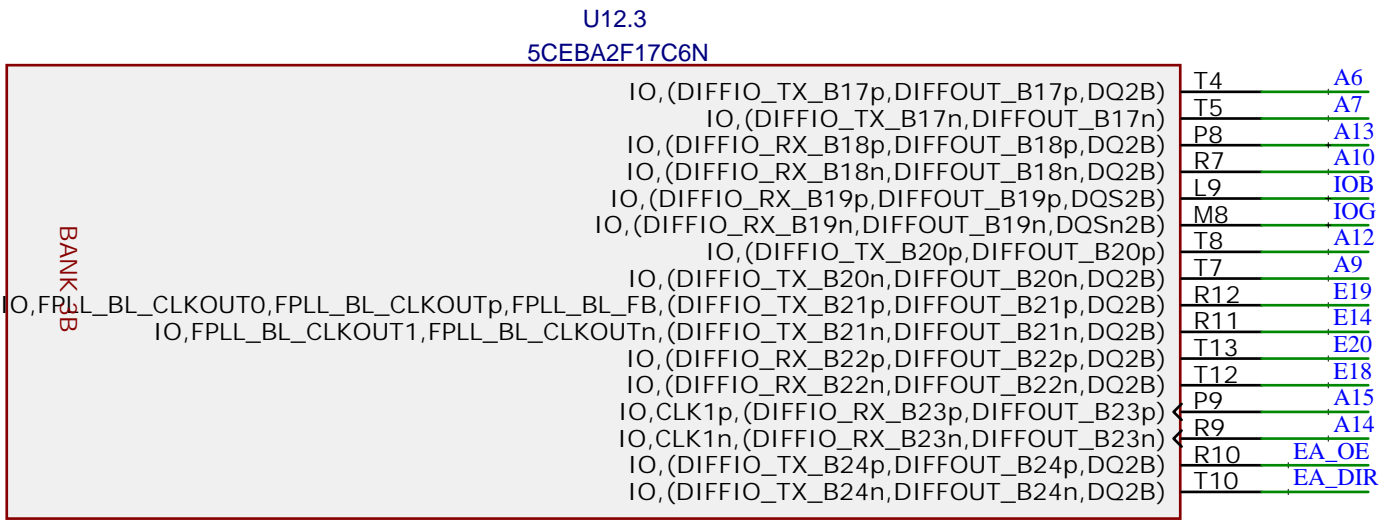
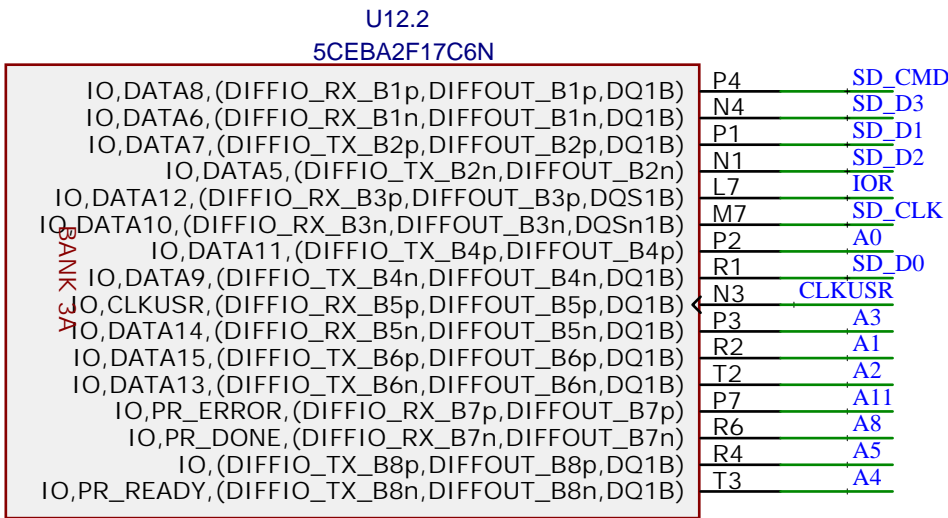
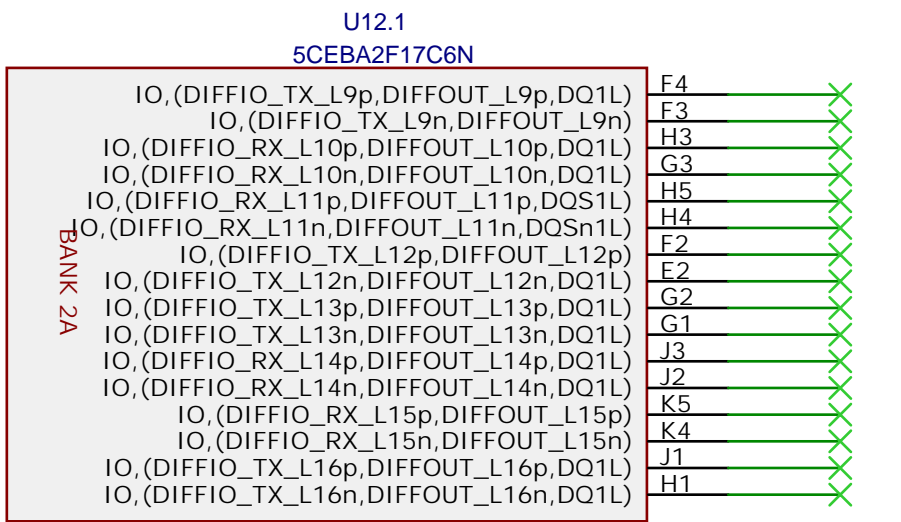


AS FAST (x4) 10010 configuration @ 3.3V

\*MSEL Pin Settings\* 7-2 in Cyclone V Device Handbook Volume 1: Device Interfaces and Integration

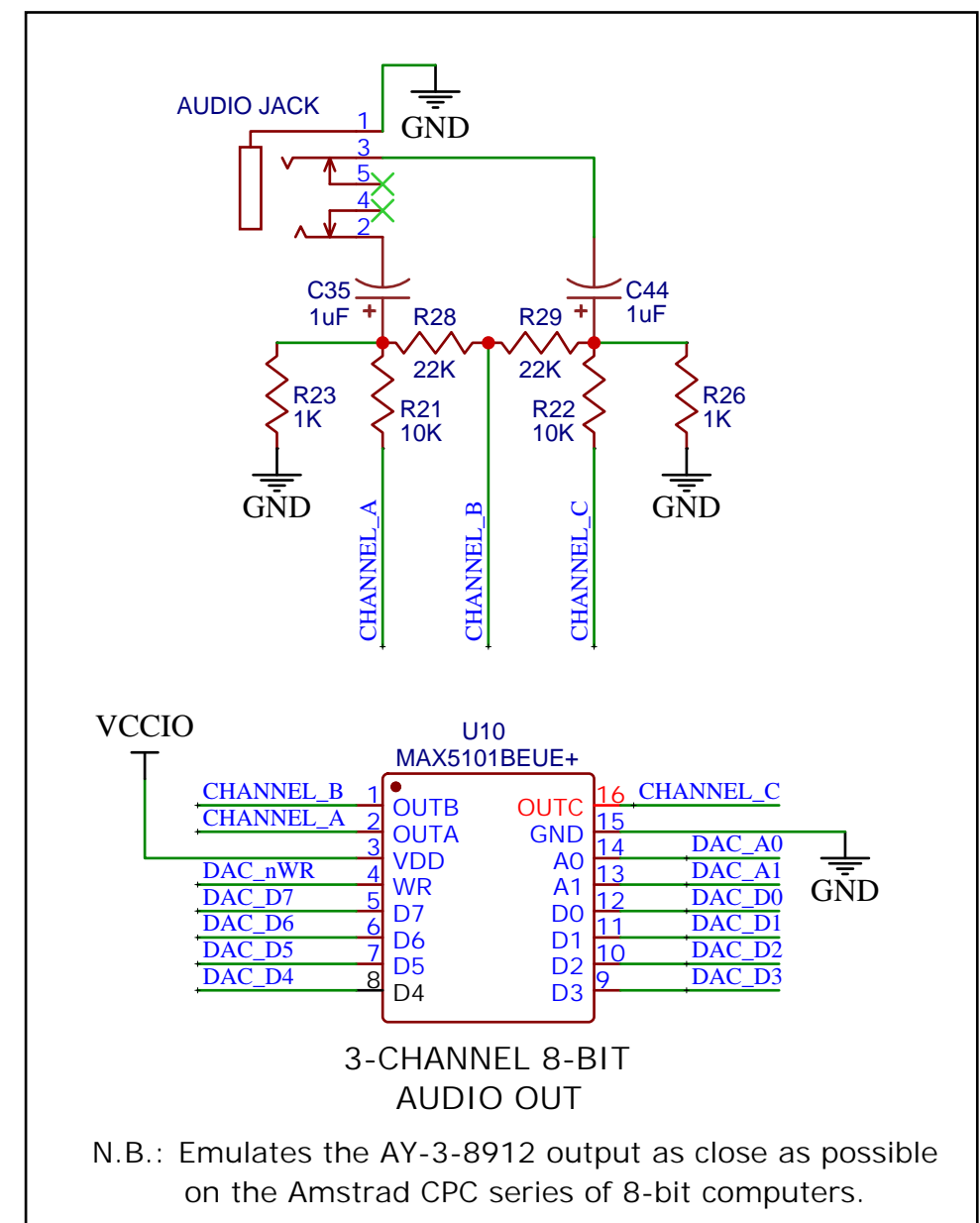
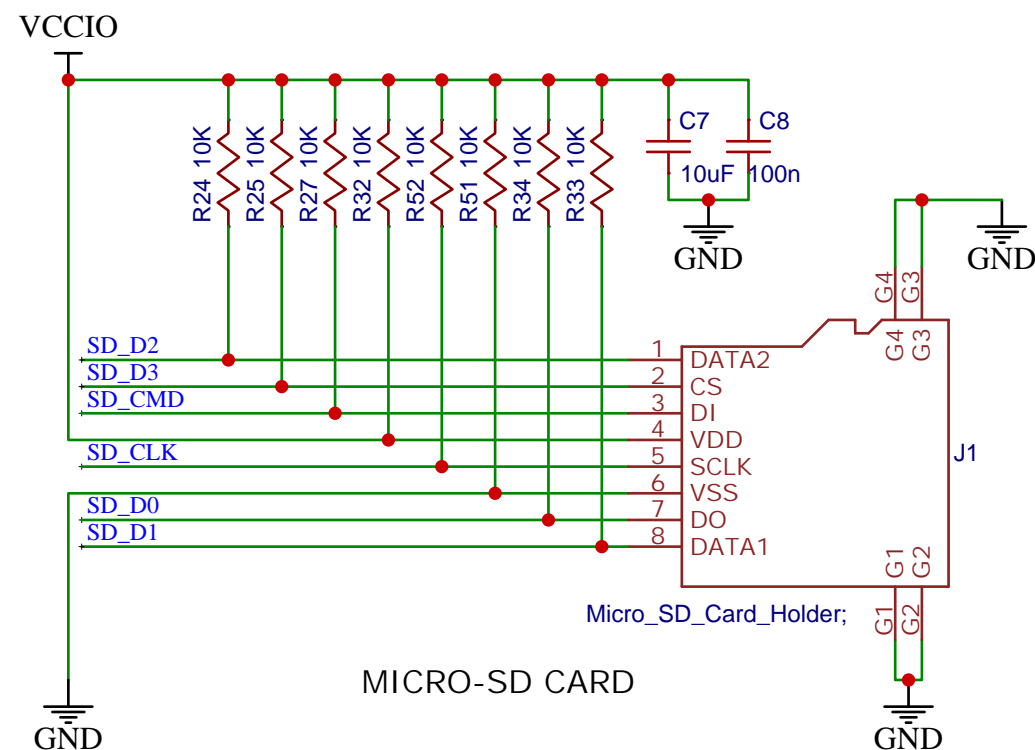
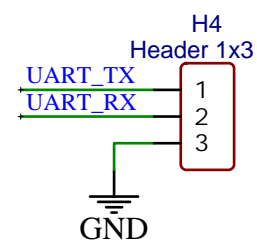
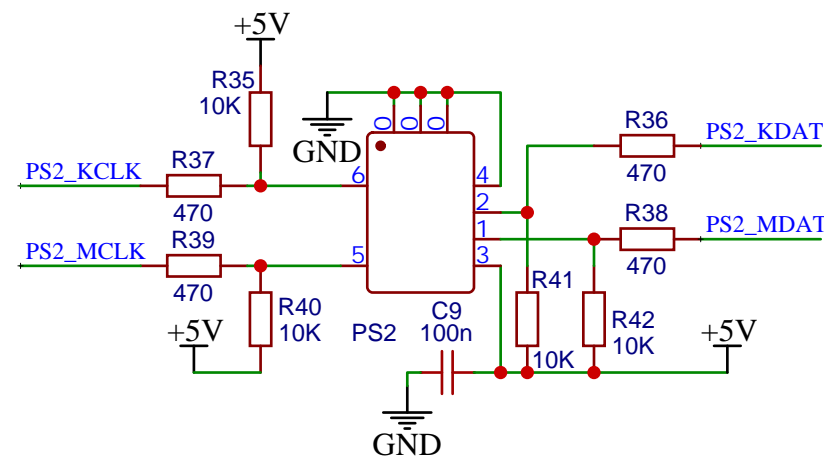
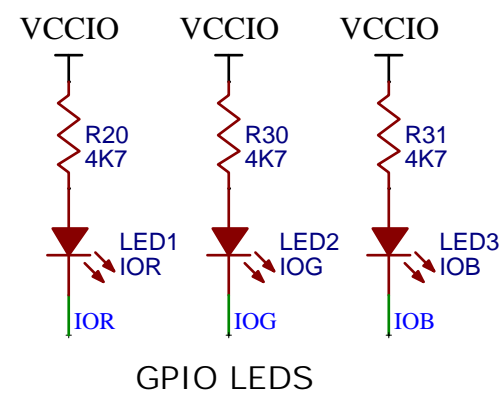
# Cyclone V FPGA

NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design.

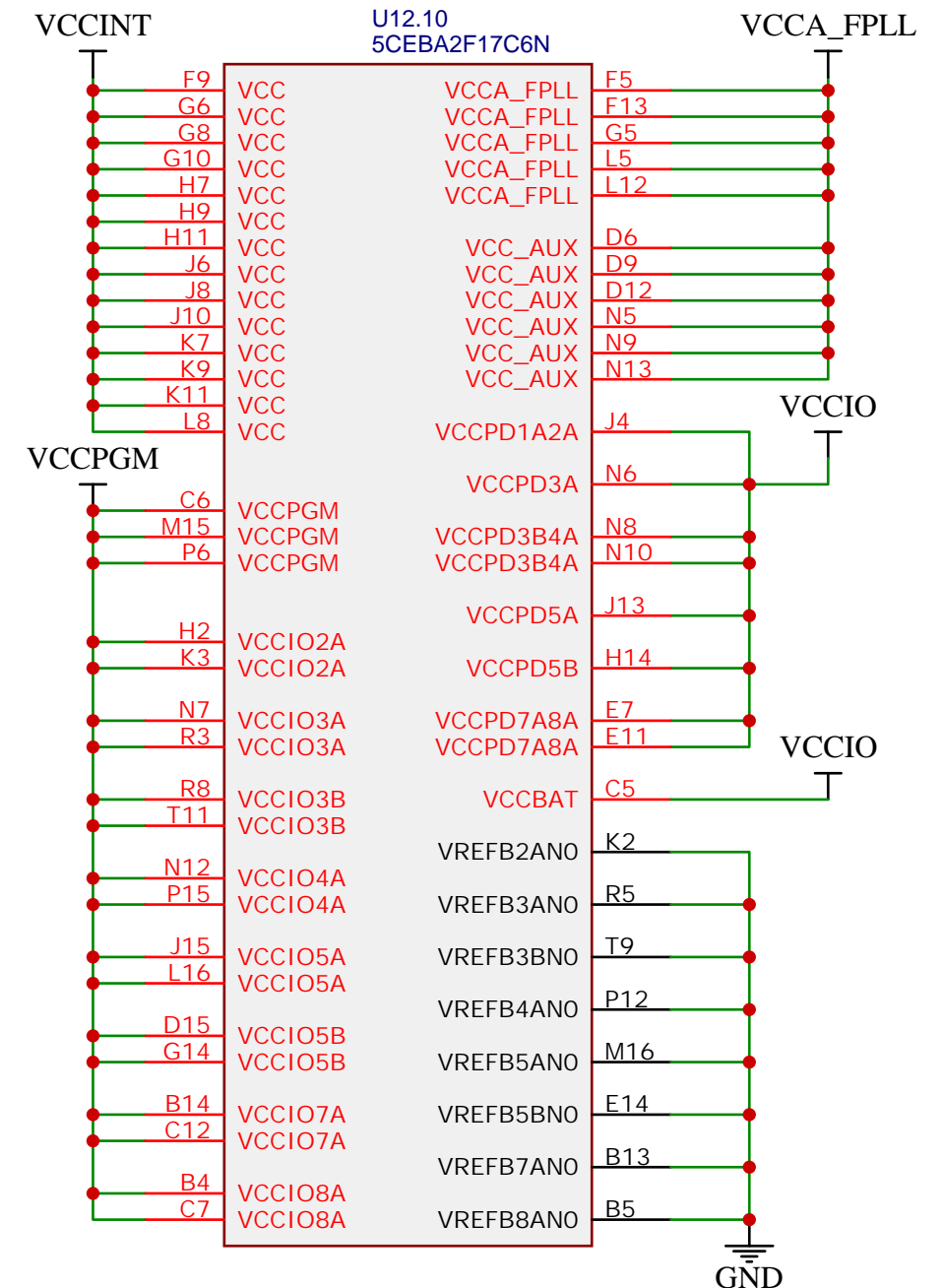
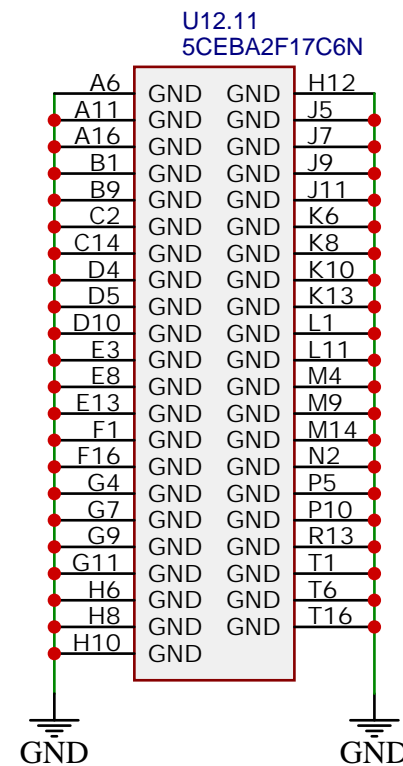
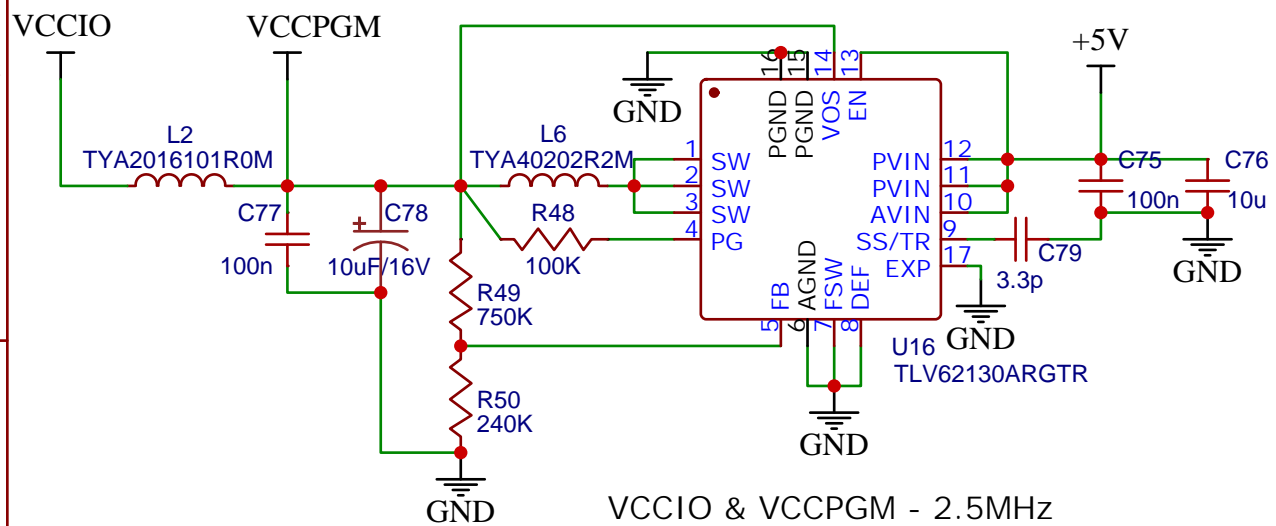
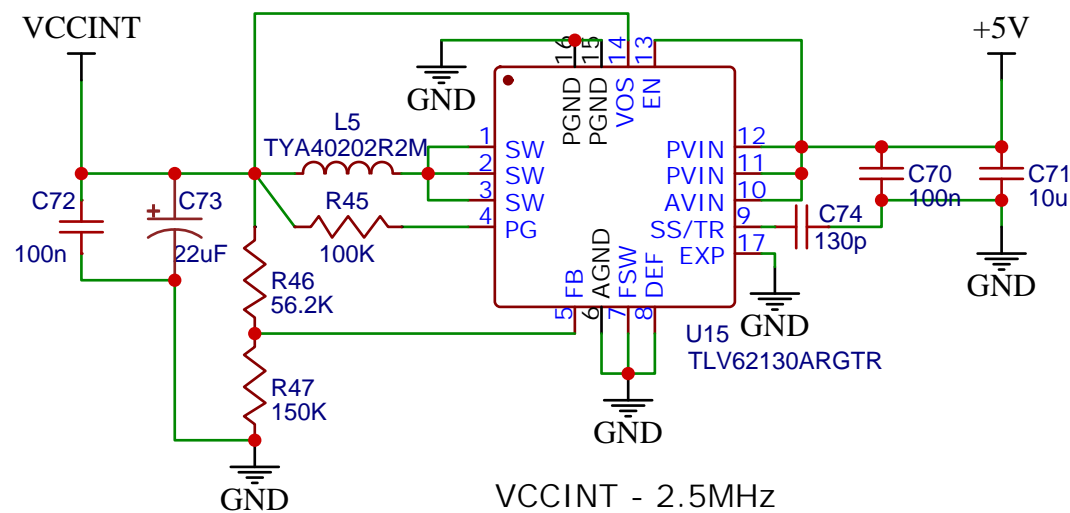
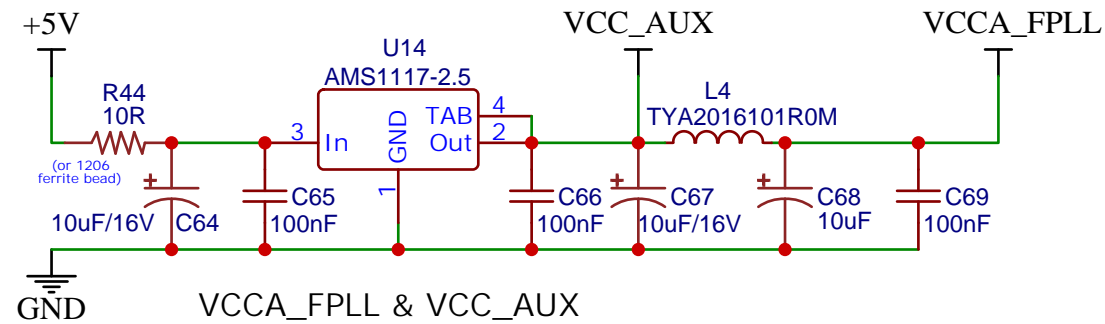
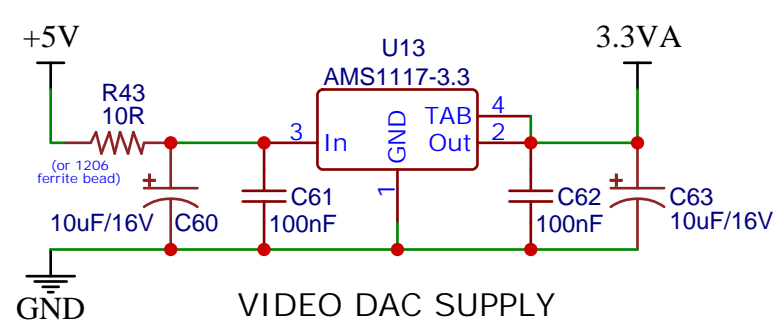




# PERIPHERALS



# POWER SUPPLIES

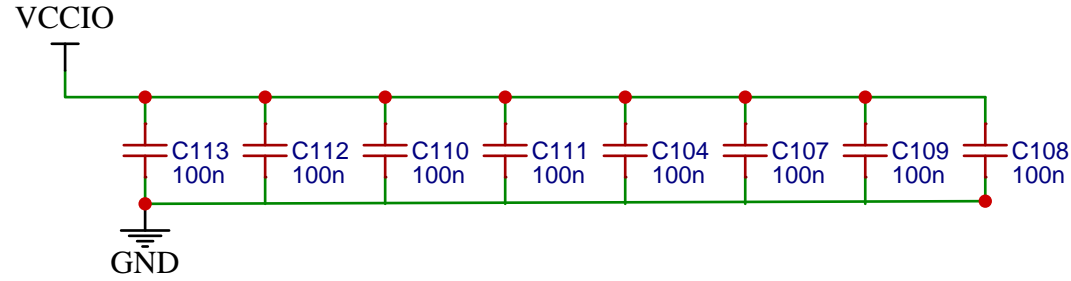
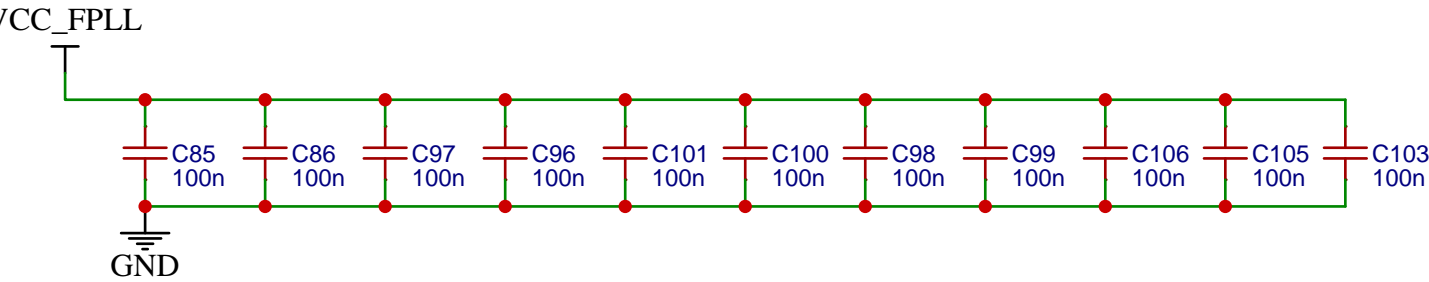
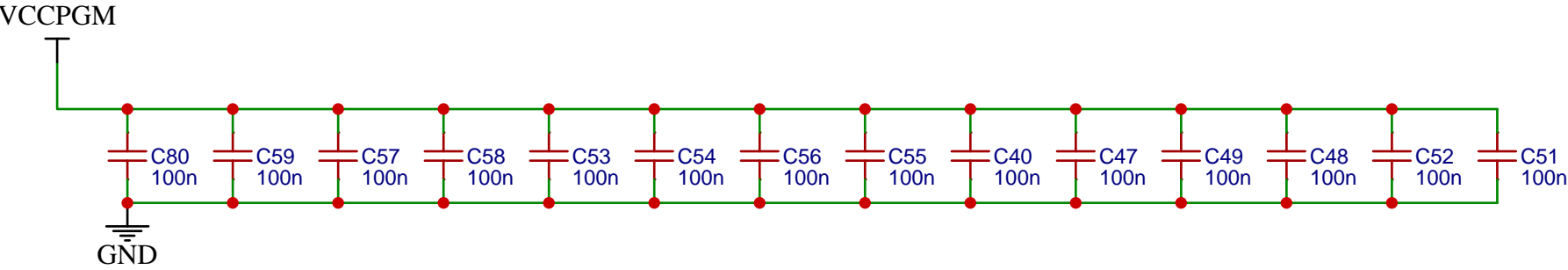
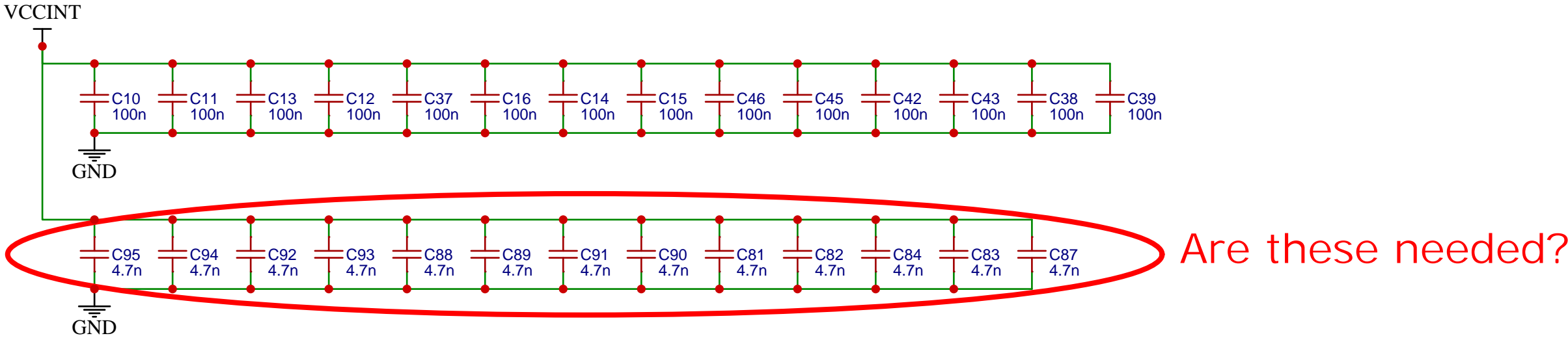


Supplies: U13 - 3.3V supply ( 3.3VA )  
 U14 - 2.5V supply ( VCCA\_FPLL, VCC\_AUX )  
 U15 - 1.1V supply ( VCCINT )  
 U16 - 3.3V supply ( VCCIO, VCCPGM )



# FPGA DECOUPLING

Note: Place capacitors near FPGA pins



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