HyperLynx®

DDR Simulation Report - DDR_Results_Jan-18-2023_21h-34m

Data Write

Data Write Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Data Write Worstcases

	Signal/Controller/DRAM			Status	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	tVAC
#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [ps]
1	/Bank34/DDR2_DM0	U2.E2	U5.F3	Pass	407.500	518.3	500.0	500.0	0.380	0.380	N/A
2	/Bank34/DDR2_DM1	U2.A5	U5.B3	Pass	403.7	524.6	500.0	500.0	0.380	0.380	N/A
3	/Bank34/DDR2_DQ1	U2.F4	U5.G2	Pass	410.8	517.0	500.0	500.0	0.380	0.380	N/A
4	/Bank34/DDR2_DQ10	U2.B2	U5.D7	Pass	431.200	495.300	500.0	500.0	0.380	0.380	N/A
5	/Bank34/DDR2_DQ11	U2.A3	U5.D3	Pass	403.300	525.1	500.0	500.0	0.380	0.380	N/A
6	/Bank34/DDR2_DQ12	U2.A4	U5.D1	Pass	402.000	523.8	500.0	500.0	0.380	0.380	N/A
7	/Bank34/DDR2_DQ13	U2.B1	U5.D9	Pass	415.300	490.700	500.0	500.0	0.380	0.380	N/A
8	/Bank34/DDR2_DQ14	U2.B5	U5.B1	Pass	400.300	527.3	500.0	500.0	0.380	0.380	N/A
9	/Bank34/DDR2_DQ15	U2.C4	U5.B9	Pass	414.300	486.700	500.0	500.0	0.380	0.380	N/A
10	/Bank34/DDR2_DQ2	U2.F2	U5.H7	Pass	437.2	488.4	500.0	500.0	0.380	0.380	N/A
11	/Bank34/DDR2_DQ3	U2.G4	U5.H3	Pass	408.200	518.6	500.0	500.0	0.380	0.380	N/A
12	/Bank34/DDR2_DQ4	U2.F3	U5.H1	Pass	405.000	516.4	500.0	500.0	0.380	0.380	N/A
13	/Bank34/DDR2_DQ5	U2.D1	U5.H9	Pass	427.100	485.800	500.0	500.0	0.380	0.380	N/A
14	/Bank34/DDR2_DQ6	U2.D4	U5.F1	Pass	407.500	517.1	500.0	500.0	0.380	0.380	N/A
15	/Bank34/DDR2_DQ7	U2.C1	U5.F9	Pass	427.6	488.0	500.0	500.0	0.380	0.380	N/A
16	/Bank34/DDR2_DQ8	U2.C3	U5.C8	Pass	421.4	493.800	500.0	500.0	0.380	0.380	N/A
17	/Bank34/DDR2_DQ9	U2.C5	U5.C2	Pass	404.500	524.1	500.0	500.0	0.380	0.380	N/A

Data Read

Data Read Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Data Read Worstcases

	Signal/DRAM/Controller			Status	Setup	Hold
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Margin [ps]	Margin [ps]
1	/Bank34/DDR2_DQ1	U5.G2	U2.F4	Pass	528.3	527.8
2	/Bank34/DDR2_DQ10	U5.D7	U2.B2	Pass	566.5	487.9
3	/Bank34/DDR2_DQ11	U5.D3	U2.A3	Pass	542.8	514.5
4	/Bank34/DDR2_DQ12	U5.D1	U2.A4	Pass	528.8	527.1
5	/Bank34/DDR2_DQ13	U5.D9	U2.B1	Pass	549.2	503.300
6	/Bank34/DDR2_DQ14	U5.B1	U2.B5	Pass	526.2	529.6
7	/Bank34/DDR2_DQ15	U5.B9	U2.C4	Pass	542.4	508.700
8	/Bank34/DDR2_DQ2	U5.H7	U2.F2	Pass	564.8	490.5
9	/Bank34/DDR2_DQ3	U5.H3	U2.G4	Pass	536.5	520.9
10	/Bank34/DDR2_DQ4	U5.H1	U2.F3	Pass	519.4	535.4
11	/Bank34/DDR2_DQ5	U5.H9	U2.D1	Pass	549.4	504.4
12	/Bank34/DDR2_DQ6	U5.F1	U2.D4	Pass	523.6	532.4
13	/Bank34/DDR2_DQ7	U5.F9	U2.C1	Pass	549.0	504.300
14	/Bank34/DDR2_DQ8	U5.C8	U2.C3	Pass	555.1	497.800
15	/Bank34/DDR2_DQ9	U5.C2	U2.C5	Pass	535.7	521.0

Address

Address Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Address Worstcases

	Signal/Dram		Status	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	tVAC
#	Signal	Accessed DRAM	Pass/Fail	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [ps]
1	/Bank34/DDR2_A0	U5.M8	Fail	1466.9	1352.8	-421.3	-101.2	0.805	0.930	N/A
2	/Bank34/DDR2_A1	U5.M3	Fail	1448.5	1358.6	-416.6	-99.7	0.774	0.893	N/A
3	/Bank34/DDR2_A10	U5.M2	Fail	1428.0	1386.6	-432.6	-120.6	0.753	0.884	N/A
4	/Bank34/DDR2_A11	U5.P7	Fail	1462.6	1351.4	-429.8	-107.6	0.803	0.923	N/A
5	/Bank34/DDR2_A12	U5.R2	Fail	1421.7	1392.8	-425.4	-137.7	0.750	0.879	N/A
6	/Bank34/DDR2_A2	U5.M7	Fail	1472.5	1355.2	-411.1	-94.8	0.810	0.932	N/A
7	/Bank34/DDR2_A3	U5.N2	Fail	1426.5	1388.2	-431.6	-122.1	0.752	0.881	N/A
8	/Bank34/DDR2_A4	U5.N8	Fail	1458.7	1350.4	-433.2	-109.9	0.797	0.918	N/A
9	/Bank34/DDR2_A5	U5.N3	Fail	1469.4	1353.6	-423.8	-104.7	0.810	0.932	N/A
10	/Bank34/DDR2_A6	U5.N7	Fail	1468.2	1353.0	-419.8	-103.6	0.806	0.928	N/A
11	/Bank34/DDR2_A7	U5.P2	Fail	1420.3	1396.7	-431.1	-133.2	0.749	0.867	N/A
12	/Bank34/DDR2_A8	U5.P8	Fail	1455.2	1348.0	-440.7	-114.8	0.798	0.921	N/A
13	/Bank34/DDR2_A9	U5.P3	Fail	1464.6	1351.4	-428.1	-104.9	0.806	0.930	N/A
14	/Bank34/DDR2_BA0	U5.L2	Fail	1431.7	1382.5	-429.2	-115.2	0.755	0.886	N/A
15	/Bank34/DDR2_BA1	U5.L3	Fail	1474.1	1353.3	-414.6	-98.0	0.814	0.933	N/A
16	/Bank34/DDR2_BA2	U5.L1	Fail	1397.6	1419.9	-432.4	-167.2	0.721	0.815	N/A
17	/Bank34/DDR2_CAS	U5.L7	Fail	1475.2	1352.7	-413.2	-96.6	0.816	0.936	N/A
18	/Bank34/DDR2_CKE	U5.K2	Fail	1398.7	1423.1	-431.8	-141.3	0.727	0.819	N/A
19	/Bank34/DDR2_ODT	U5.K9	Fail	1454.0	1354.5	-434.9	-113.9	0.803	0.918	N/A
20	/Bank34/DDR2_RAS	U5.K7	Fail	1477.1	1349.5	-407.3	-94.2	0.820	0.937	N/A
21	/Bank34/DDR2_WE	U5.K3	Fail	1477.3	1350.0	-406.8	-95.2	0.820	0.940	N/A

Differential Nets

Differential Nets Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Differential Nets Worstcases

	Signal/Driver/Receicer				Status	Overshoot	Undershoot	Overshoot Area	Undershoot Area	tDVAC	Vix			
#	Signal	Driver.Pins	Receiver.Pins	Operation	Pass/Fail	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [ps]	Margin [mV]	VID(AC) [mV]	VID(DC)	VSEH/L
1	/Bank34/DDR2_CK+	U2.P4&P3	U5.J8&K8	Write rank(1,1)	Pass	500.0	500.0	0.380	0.380	N/A	140.5	1000.4	Pass	N/A
2	/Bank34/DDR2_DQS0+	U5.F7&E8	U2.G1&F1	Read rank(1,1)	Pass	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3	/Bank34/DDR2_DQS0+	U2.G1&F1	U5.F7&E8	Write rank(1,1)	Pass	500.0	500.0	0.380	0.380	N/A	130.1	1145.2	Pass	N/A
4	/Bank34/DDR2_DQS1+	U5.B7&A8	U2.B3&A2	Read rank(1,1)	Pass	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
5	/Bank34/DDR2_DQS1+	U2.B3&A2	U5.B7&A8	Write rank(1,1)	Pass	500.0	500.0	0.380	0.380	N/A	162.3	1061.8	Pass	N/A

CLK-DQS Skew

CLK-DQS Skew Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

CLK-DQS Skew Worstcases

	Signal/Dram				Status	DQSS - Earliest DQS	DQSS - Latest DQS	tDSS	tDSH
#	Signal	Accessed DRAM	DRAM CLK Pins	DRAM DQS Pins	Pass/Fail	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]
1	/Bank34/DDR2_DQS0+	U5	J8&K8	F7&E8	Pass	745.2	754.7	1003.0	996.5
2	/Bank34/DDR2_DQS1+	U5	J8&K8	B7&A8	Pass	739.8	760.2	1010.0	989.5

Setup Info

Design: S7_Min.hyp

VX2.11 build 20158559

Date: Jan-18-2023 21h-34m

Setup Information

Interface Setup

Parameter	Value
DDR Interface	DDR2
Crosstalk	Disabled
Power-Aware	Disabled
IC Corners	Slow
Probing location	Controller - at Die, DRAM - at Pin
Total Run Time	0 Days, 00 Hours, 00 Minutes 56 Seconds

Rank Setup

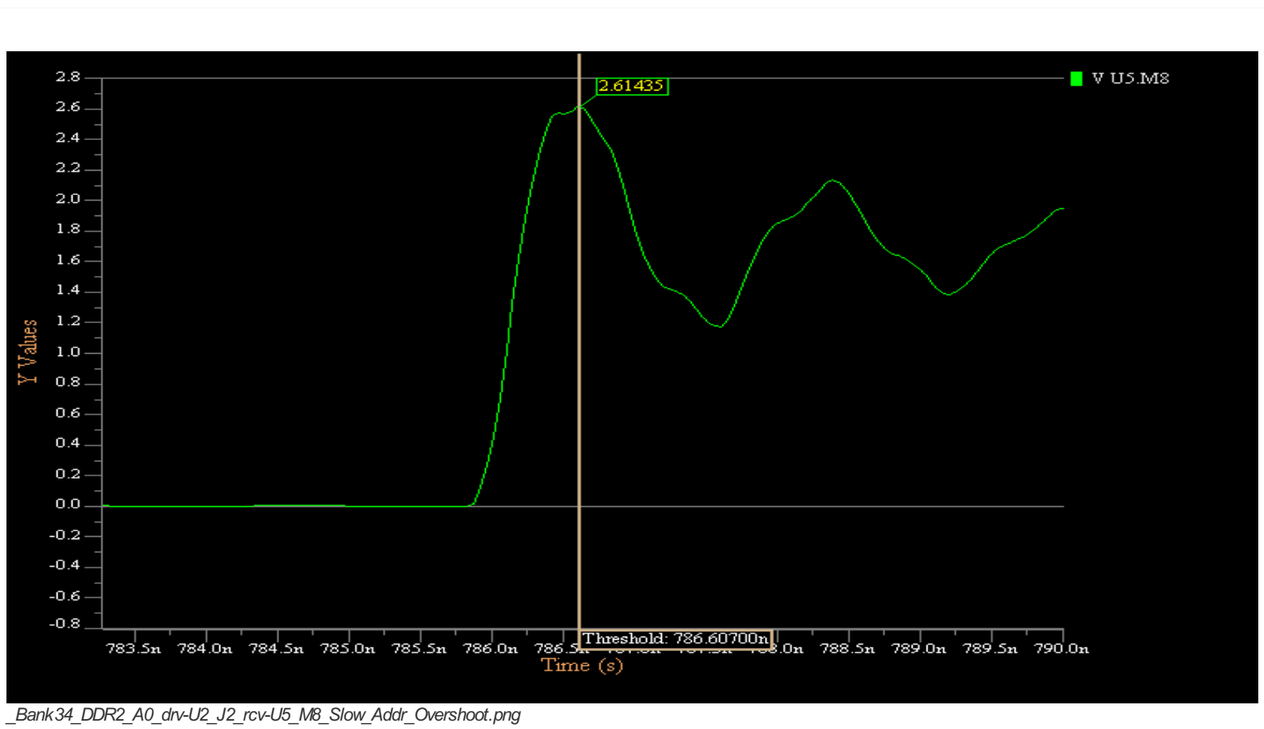
Rank	Ref. Des.	IBIS File	Component	Timing Model	Speed Grade
Controller	U2	spartan7.ibs	SPARTAN7	C:\PADs\PADSVX.2.11\SDD_HOME\hyperlynx64\Libs\ddr2_ctl.v	DDR2_400
Rank[1,1]	U5	MT47H64M16NF-25E.ibs	MT47H64M16NF	C:\PADs\PADSVX.2.11\SDD_HOME\hyperlynx64\Libs\ddr2_dram.v	DDR2_400

Address Images

Page Content

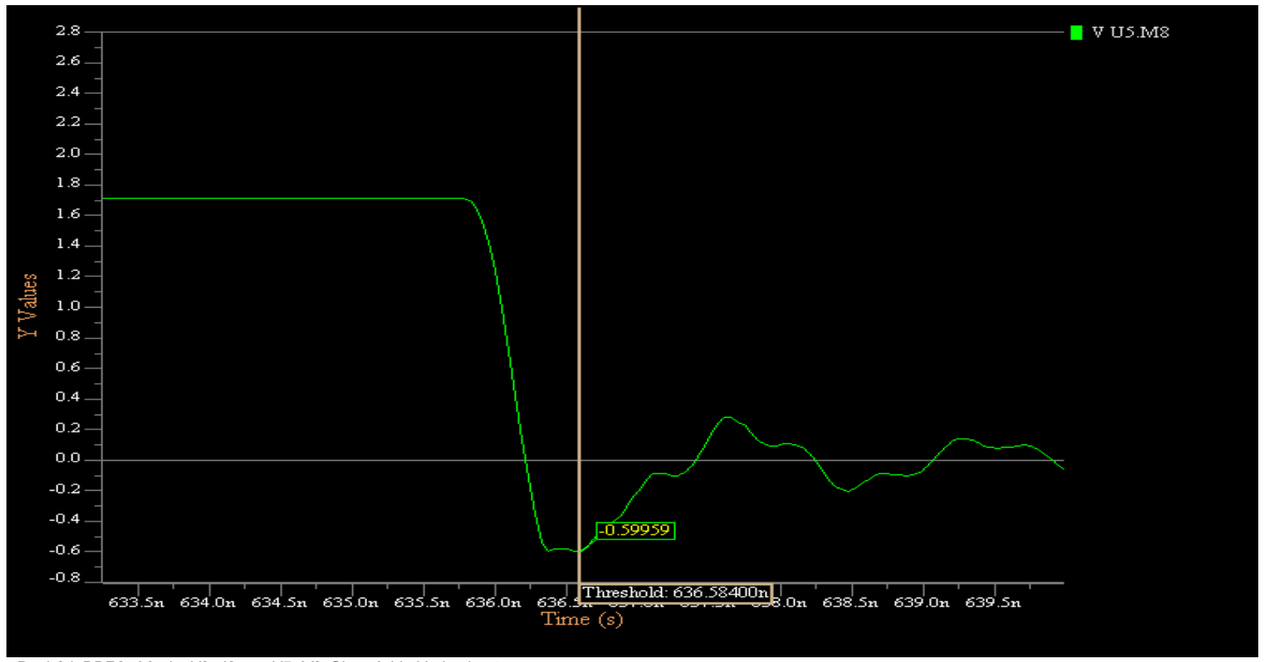
Images

/Bank34/DDR2_A0



_Bank34_DDR2_A0_drv-U2_J2_rcv-U5_M8_Slow_Addr_Overshoot.png

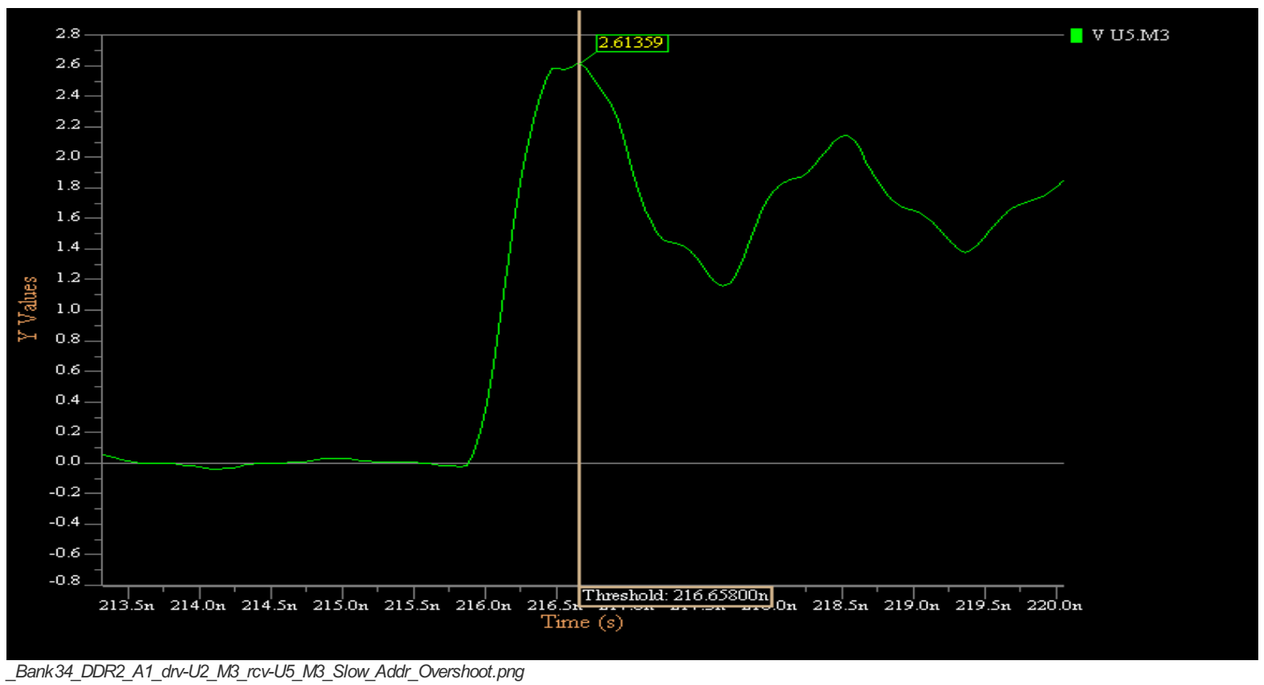
Return to table Launch in EZwave



_Bank34_DDR2_A0_drv-U2_J2_rcv-U5_M8_Slow_Addr_Undershoot.png

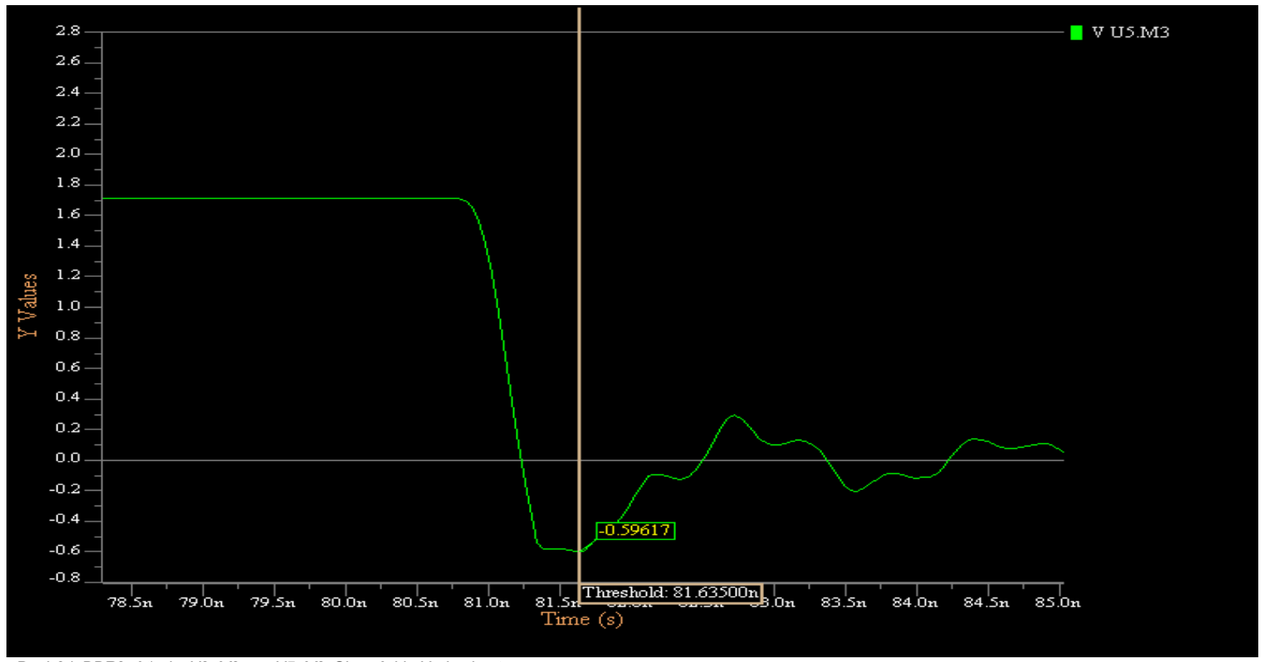
Return to table Launch in EZwave

/Bank34/DDR2_A1



_Bank34_DDR2_A1_drv-U2_M3_rcv-U5_M3_Slow_Addr_Overshoot.png

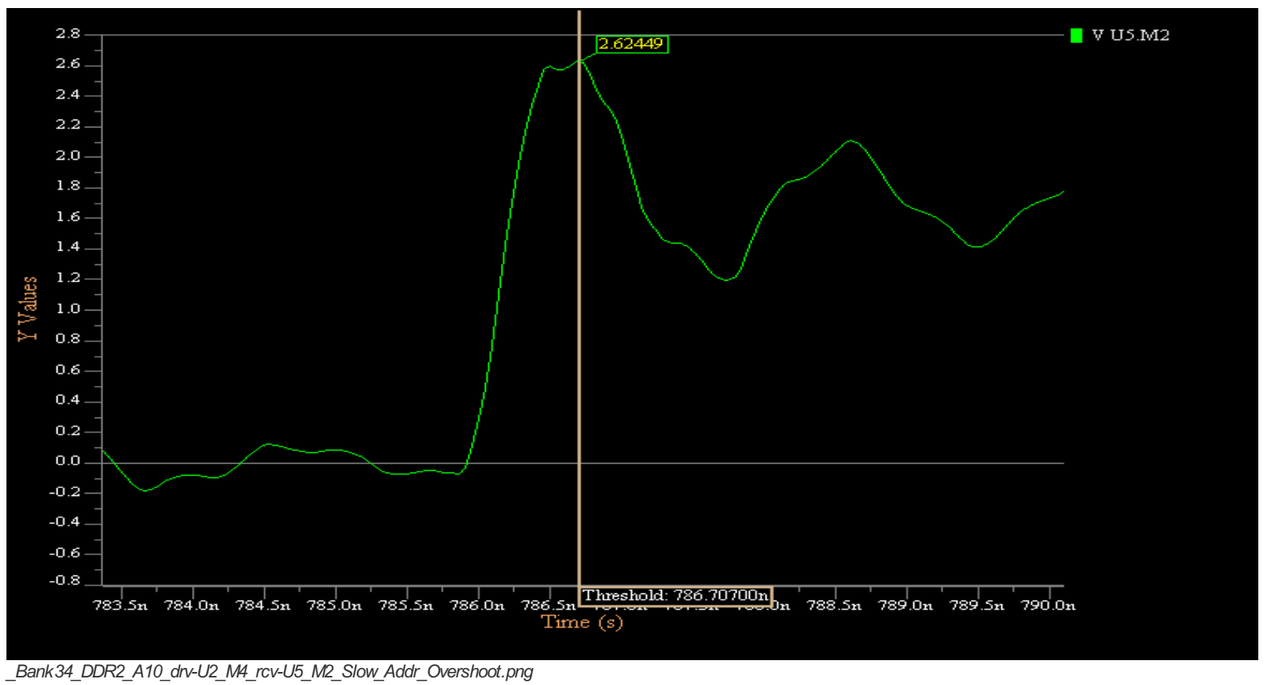
Return to table Launch in EZwave



_Bank34_DDR2_A1_drv-U2_M3_rcv-U5_M3_Slow_Addr_Undershoot.png

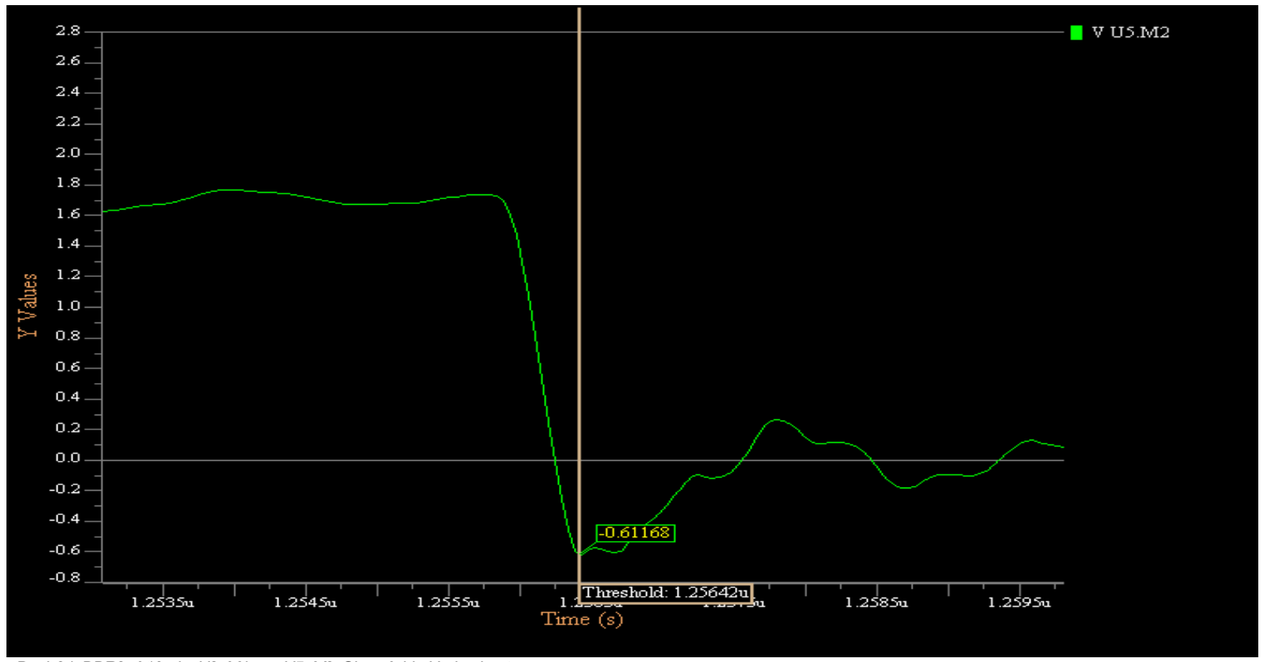
Return to table Launch in EZwave

/Bank34/DDR2_A10



_Bank34_DDR2_A10_drv-U2_M4_rcv-U5_M2_Slow_Addr_Overshoot.png

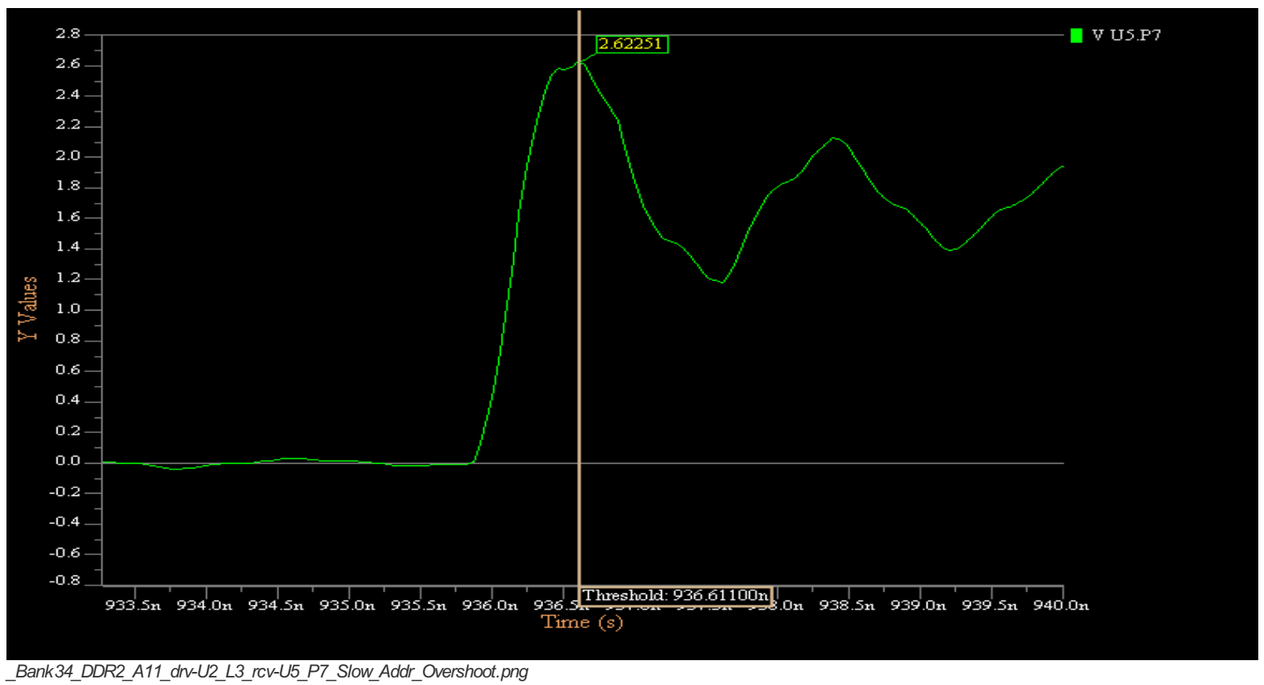
Return to table Launch in EZwave



_Bank34_DDR2_A10_drv-U2_M4_rcv-U5_M2_Slow_Addr_Undershoot.png

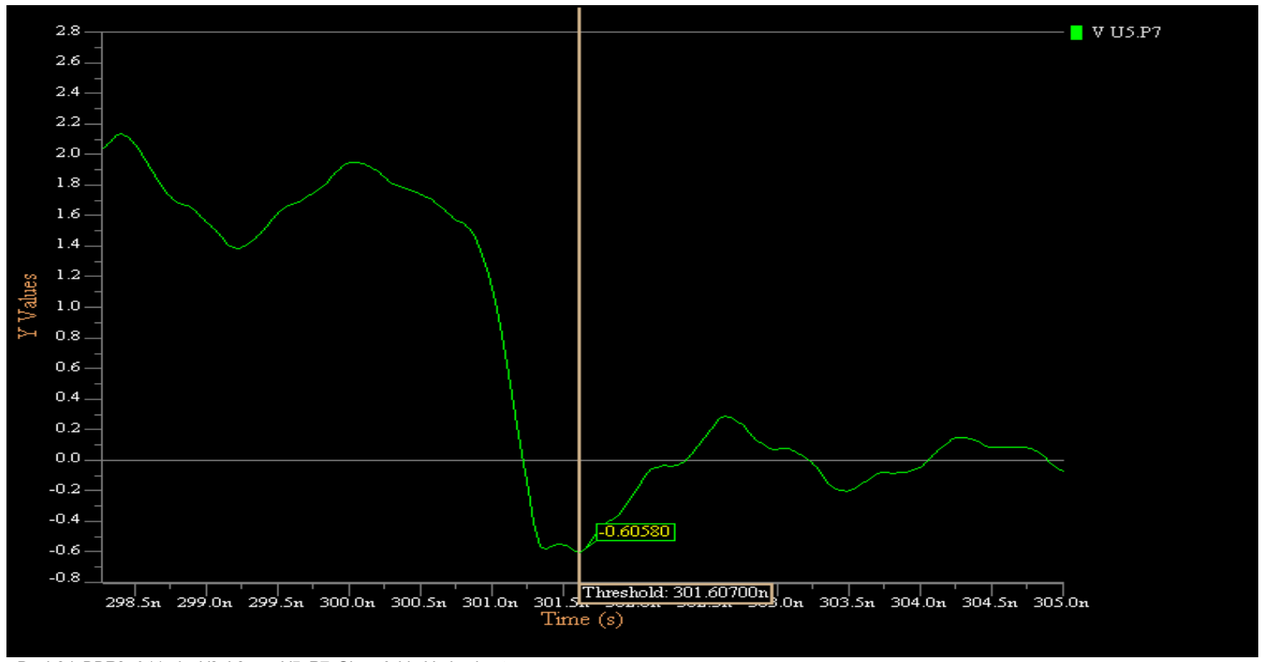
Return to table Launch in EZwave

/Bank34/DDR2_A11



_Bank34_DDR2_A11_drv-U2_L3_rcv-U5_P7_Slow_Addr_Overshoot.png

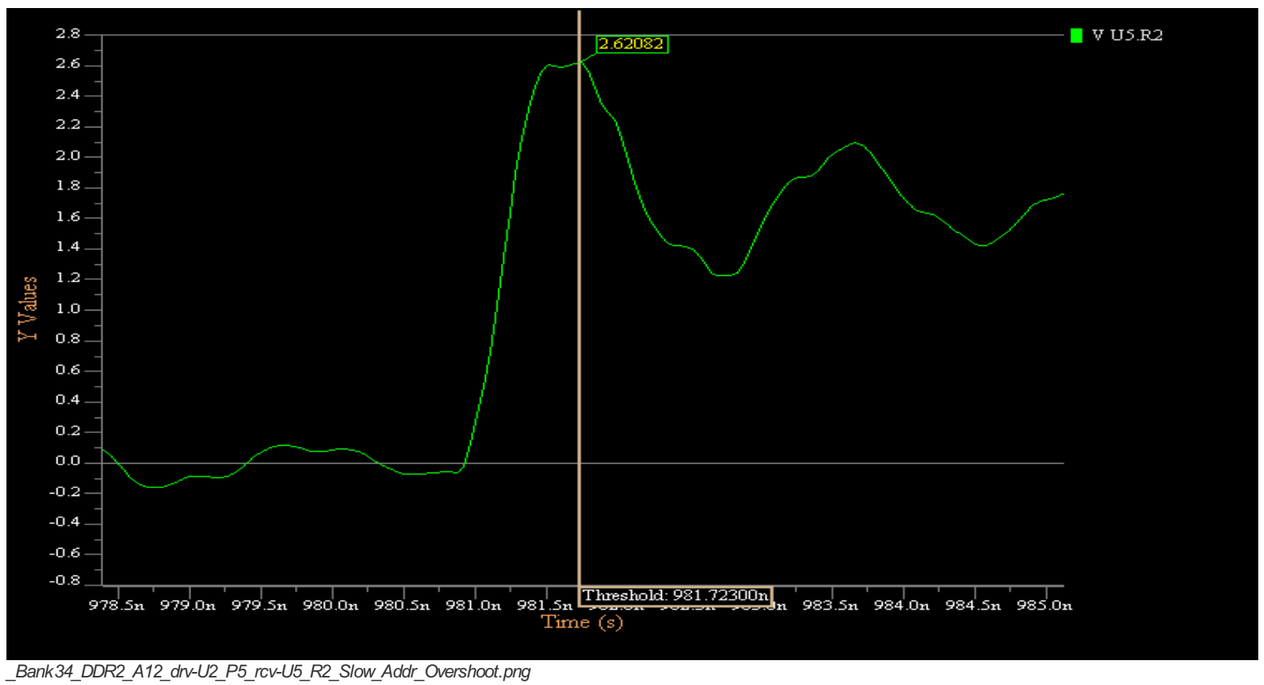
Return to table Launch in EZwave



_Bank34_DDR2_A11_drv-U2_L3_rcv-U5_P7_Slow_Addr_Undershoot.png

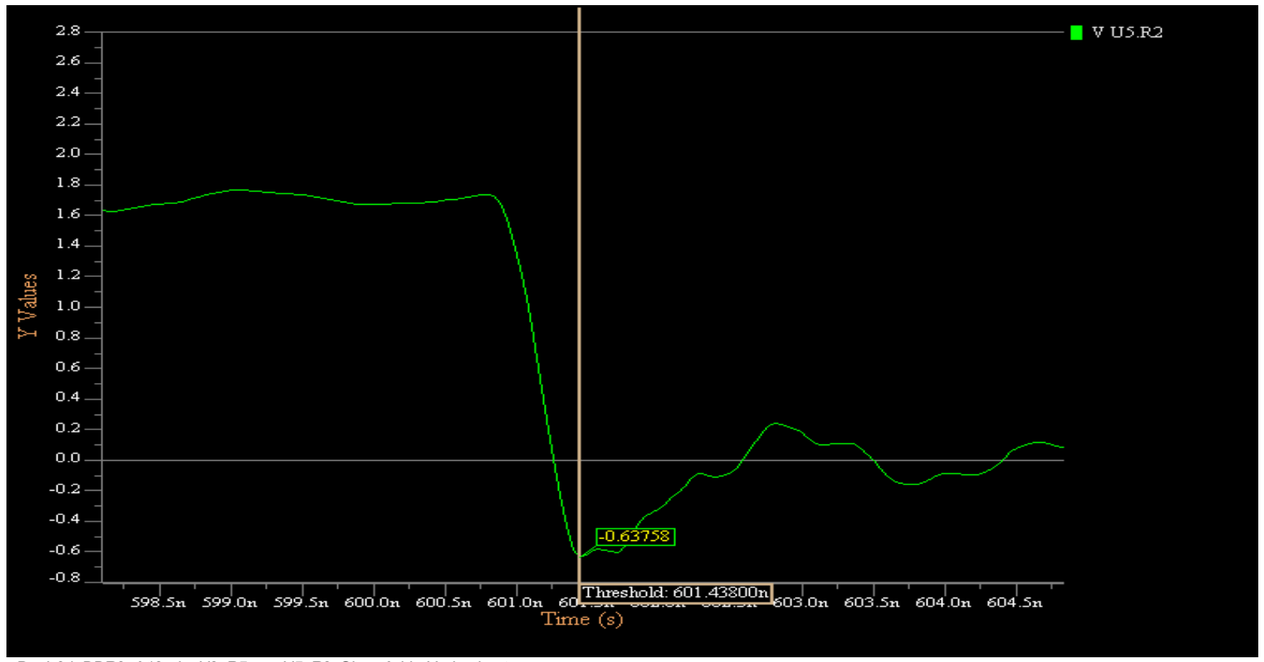
Return to table Launch in EZwave

/Bank34/DDR2_A12



_Bank34_DDR2_A12_drv-U2_P5_rcv-U5_R2_Slow_Addr_Overshoot.png

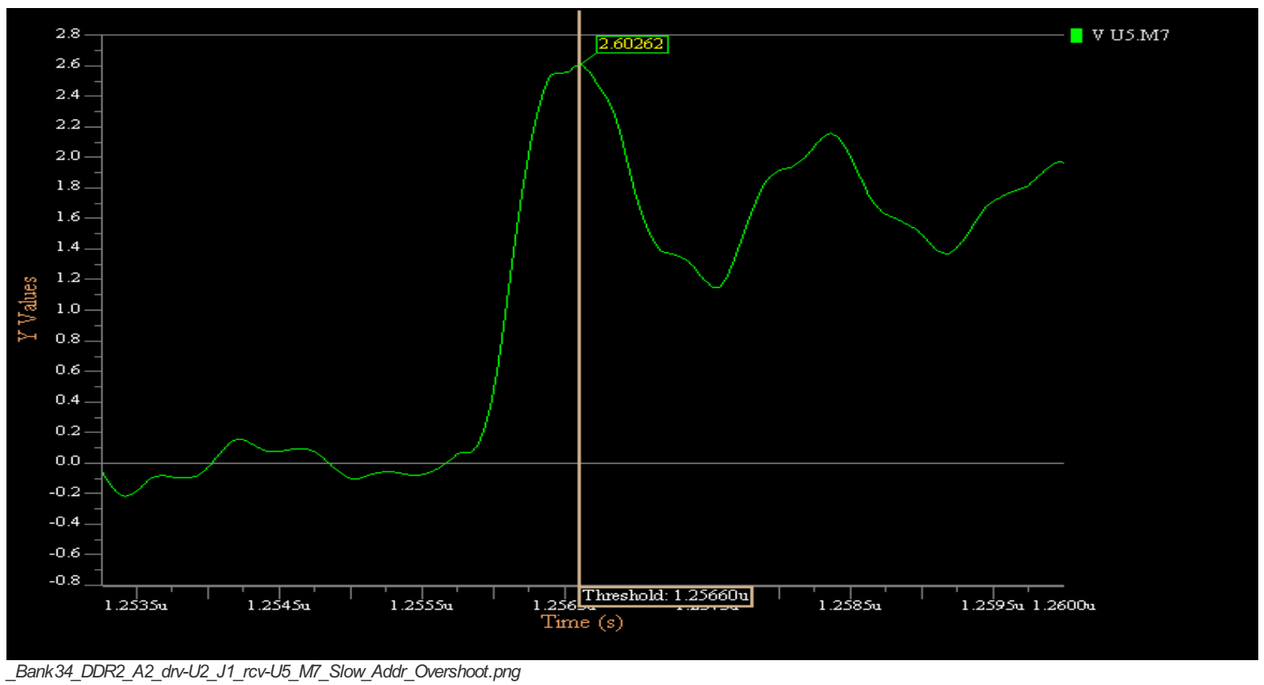
Return to table Launch in EZwave



_Bank34_DDR2_A12_drv-U2_P5_rcv-U5_R2_Slow_Addr_Undershoot.png

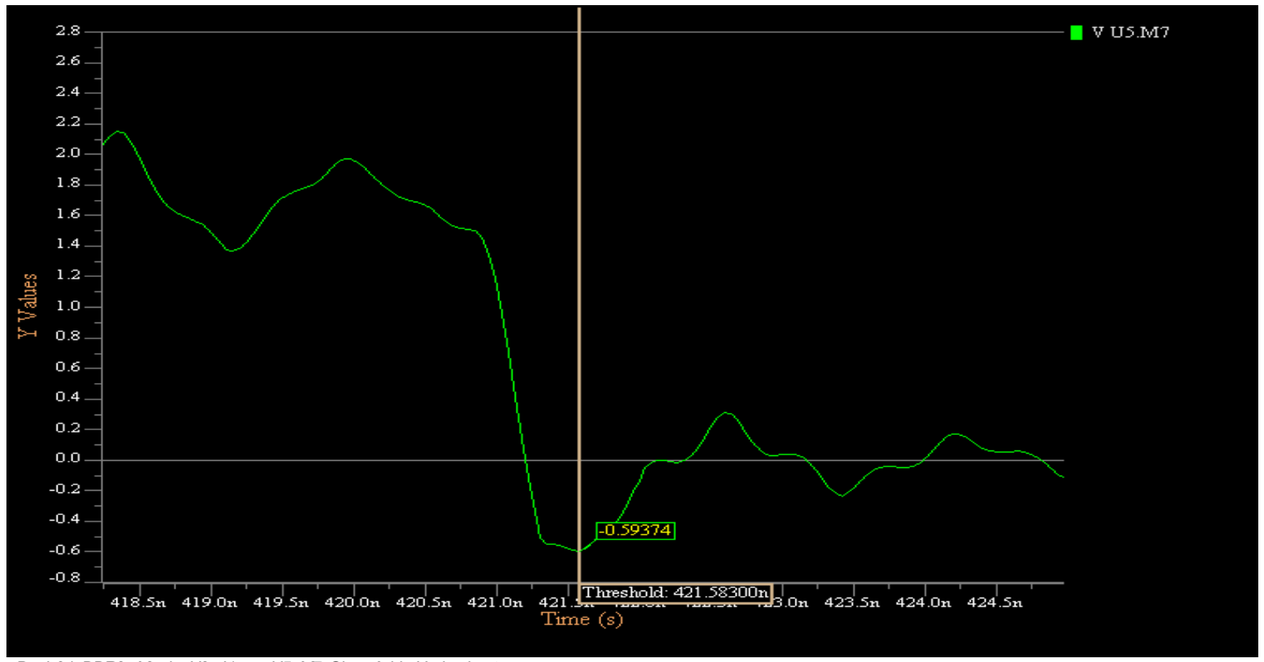
Return to table Launch in EZwave

/Bank34/DDR2_A2



_Bank34_DDR2_A2_drv-U2_J1_rcv-U5_M7_Slow_Addr_Overshoot.png

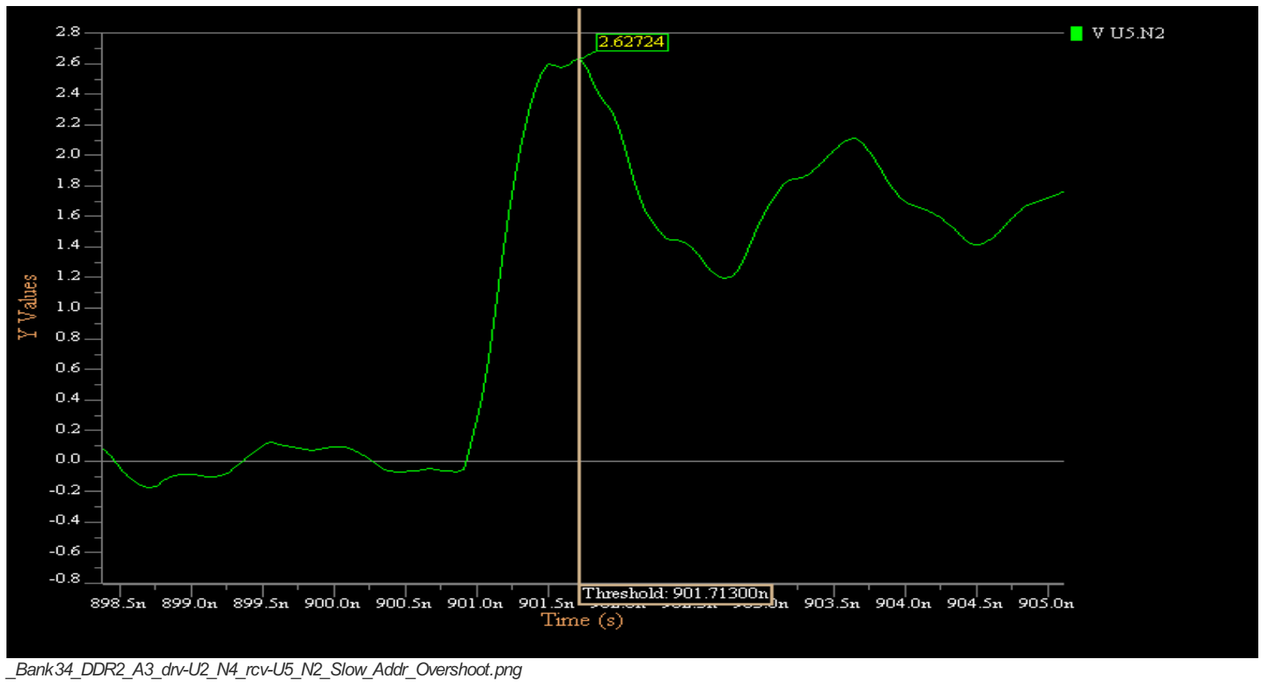
Return to table Launch in EZwave



_Bank34_DDR2_A2_drv-U2_J1_rcv-U5_M7_Slow_Addr_Undershoot.png

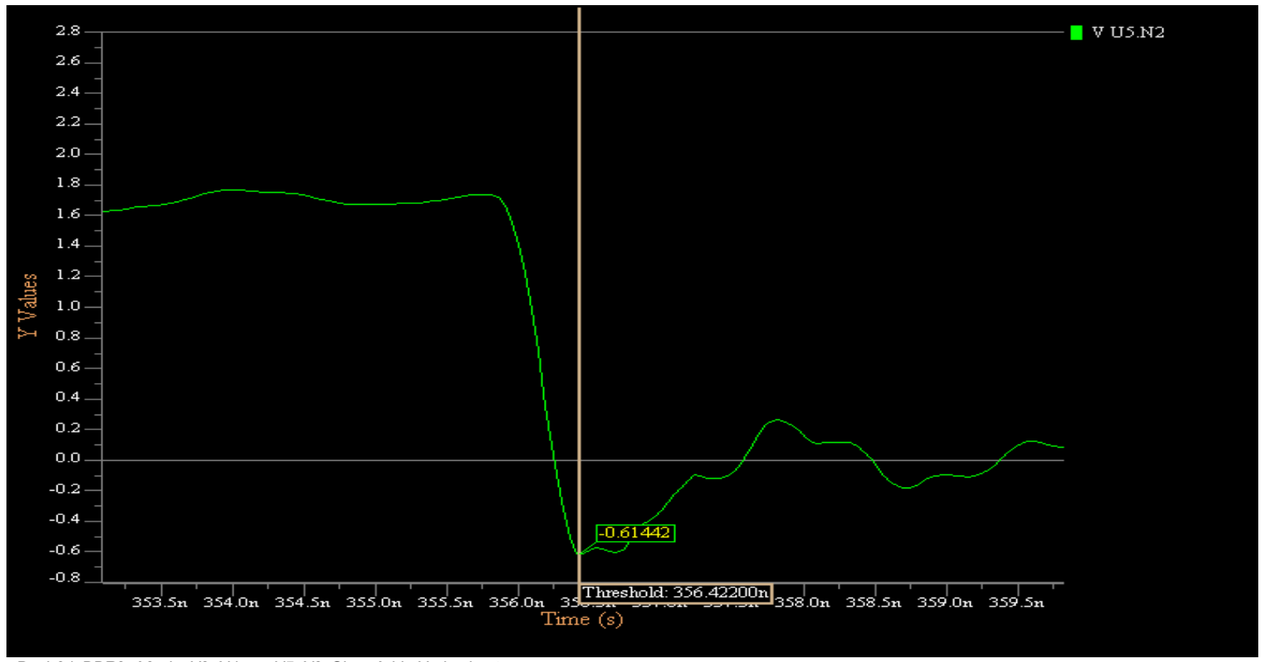
Return to table Launch in EZwave

/Bank34/DDR2_A3



_Bank34_DDR2_A3_drv-U2_N4_rcv-U5_N2_Slow_Addr_Overshoot.png

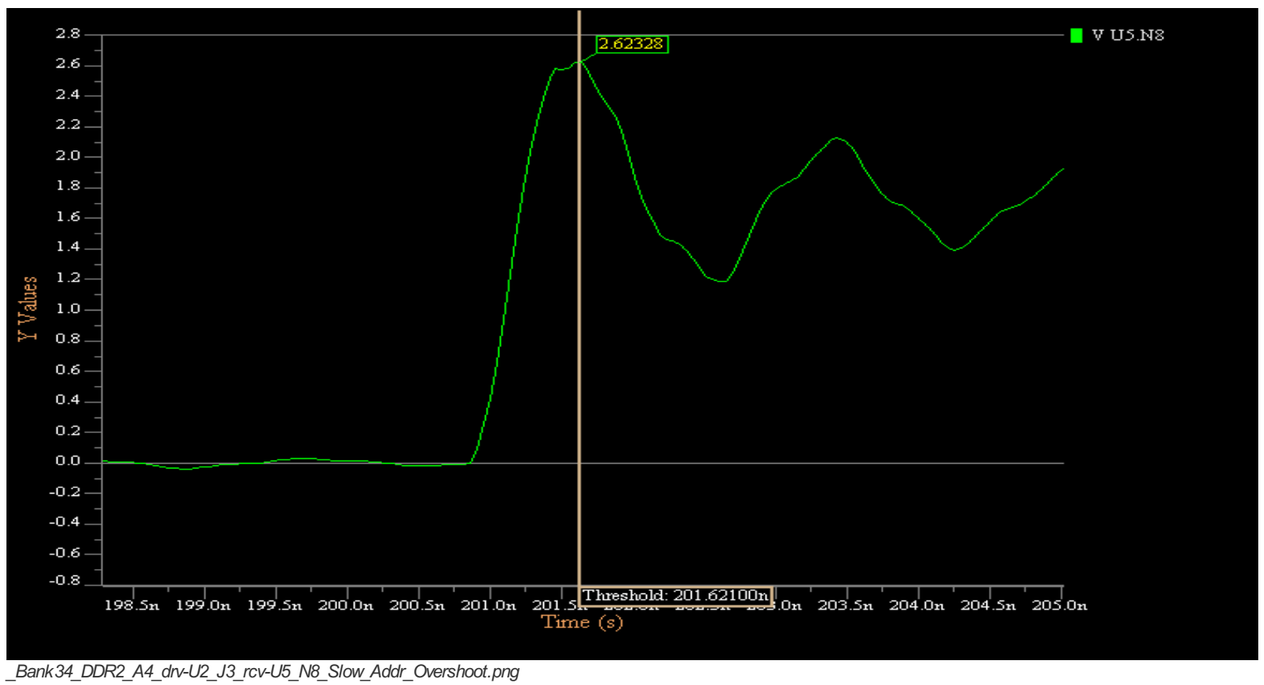
Return to table Launch in EZwave



_Bank34_DDR2_A3_drv-U2_N4_rcv-U5_N2_Slow_Addr_Undershoot.png

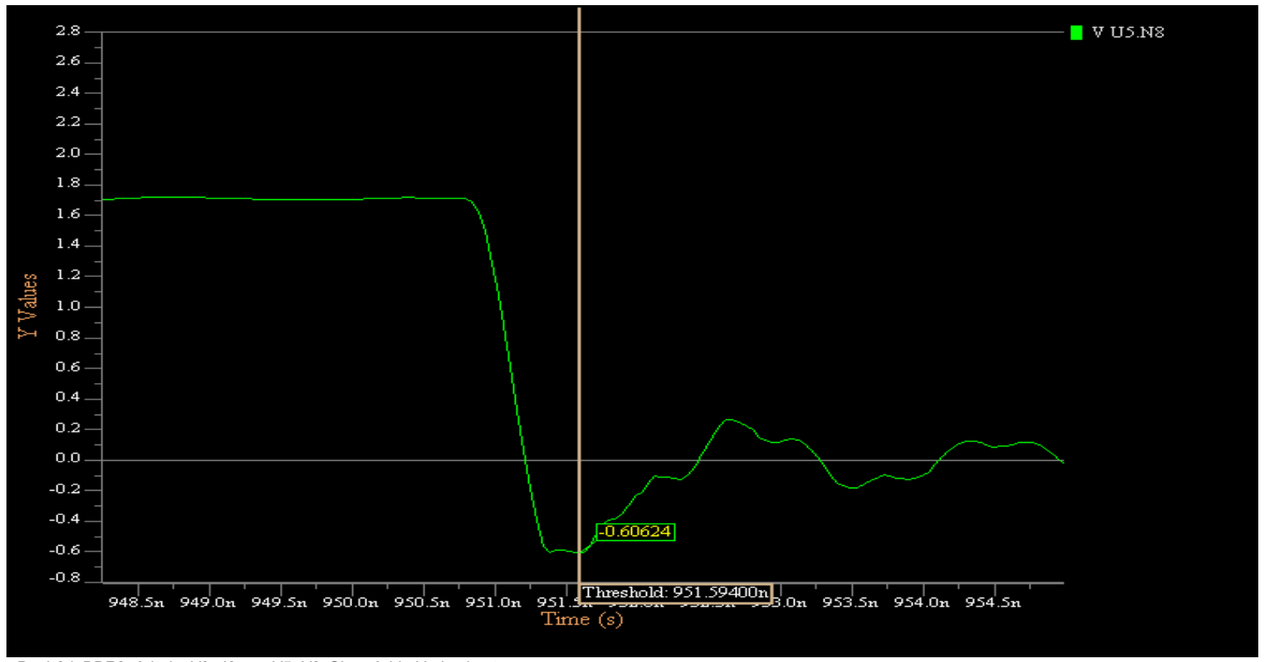
Return to table Launch in EZwave

/Bank34/DDR2_A4



_Bank34_DDR2_A4_drv-U2_J3_rcv-U5_N8_Slow_Addr_Overshoot.png

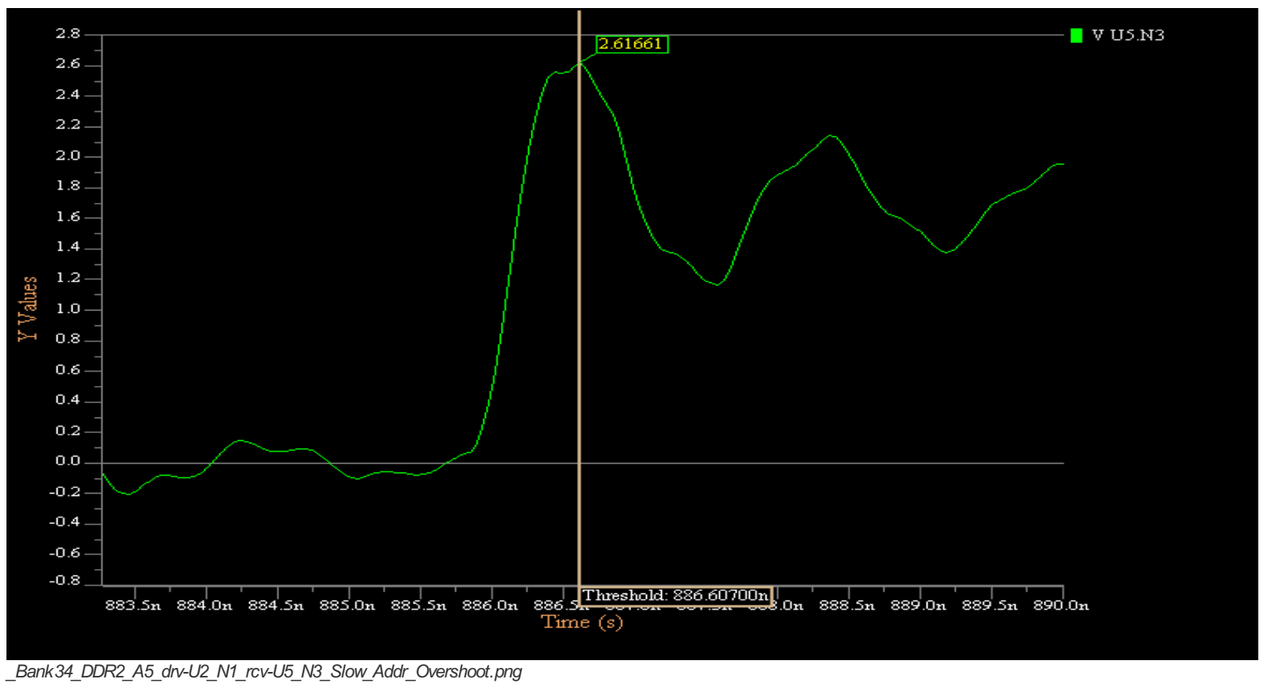
Return to table Launch in EZwave



_Bank34_DDR2_A4_drv-U2_J3_rcv-U5_N8_Slow_Addr_Undershoot.png

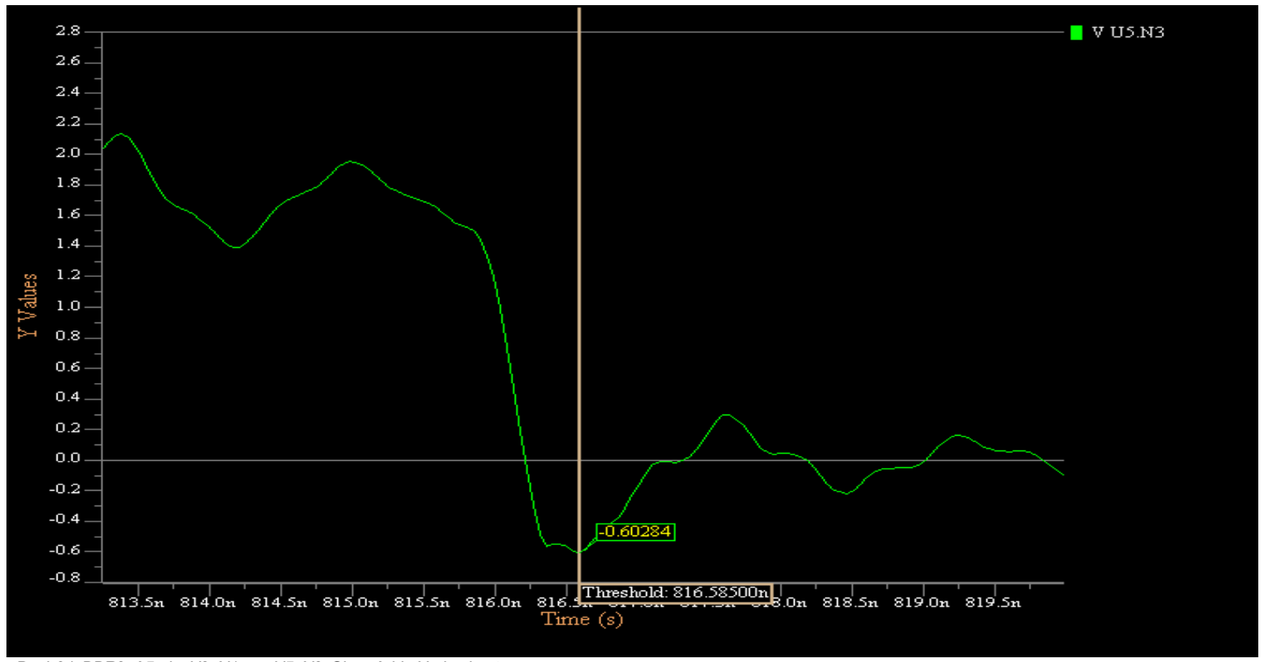
Return to table Launch in EZwave

/Bank34/DDR2_A5



_Bank34_DDR2_A5_drv-U2_N1_rcv-U5_N3_Slow_Addr_Overshoot.png

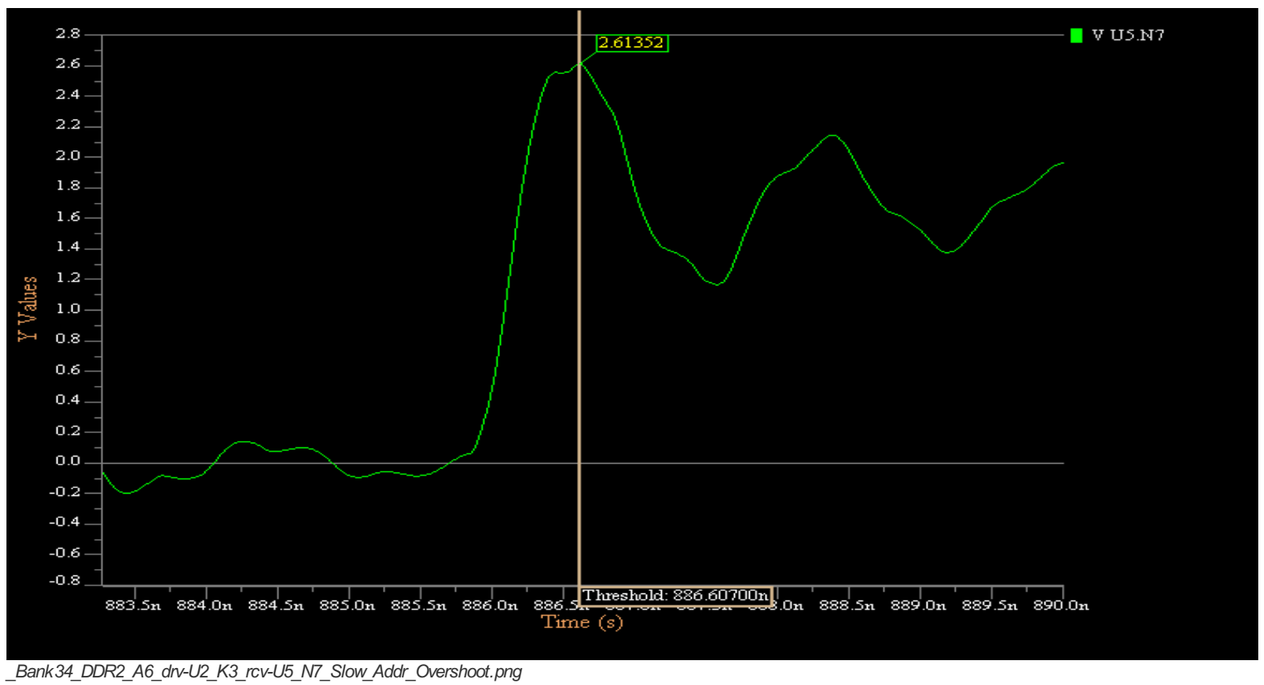
Return to table Launch in EZwave



_Bank34_DDR2_A5_drv-U2_N1_rcv-U5_N3_Slow_Addr_Undershoot.png

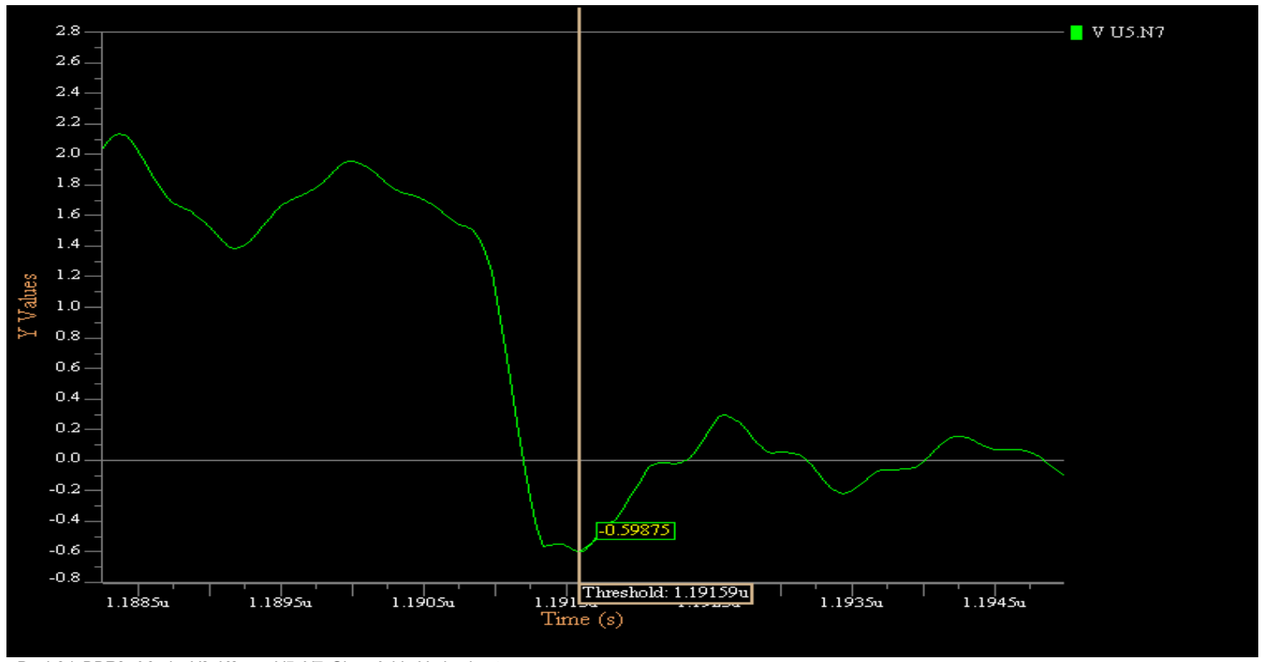
Return to table Launch in EZwave

/Bank34/DDR2_A6



_Bank34_DDR2_A6_drv-U2_K3_rcv-U5_N7_Slow_Addr_Overshoot.png

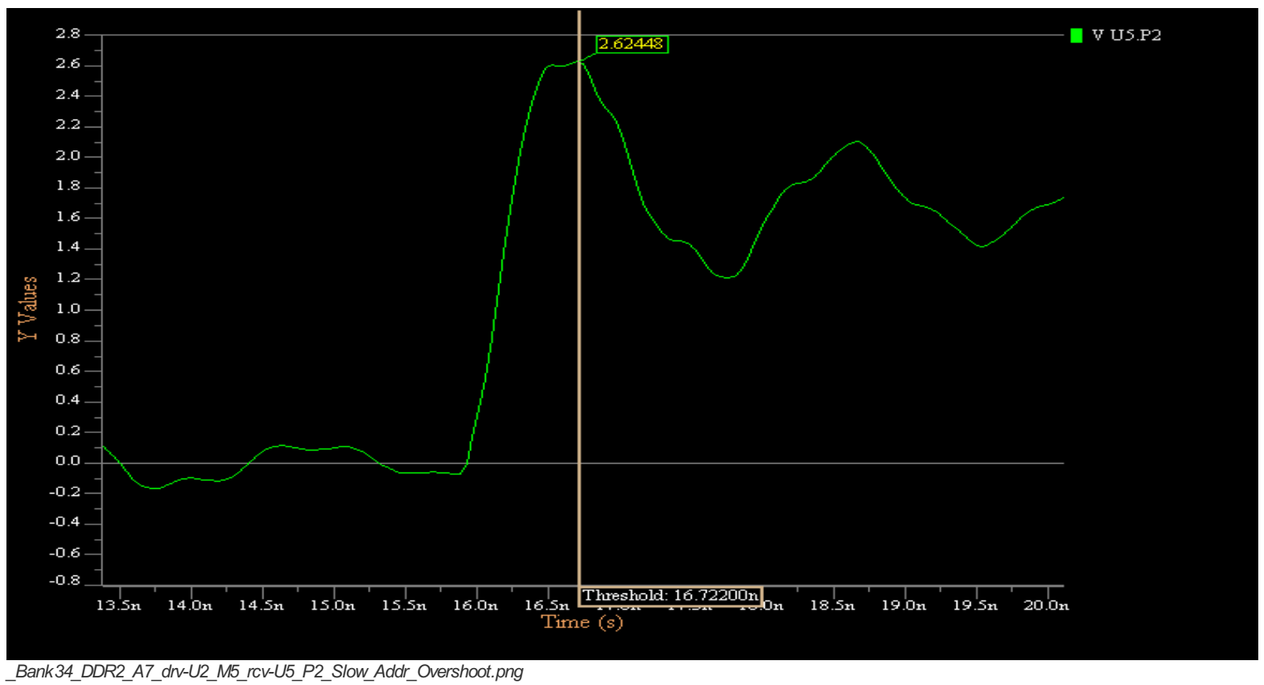
Return to table Launch in EZwave



_Bank34_DDR2_A6_drv-U2_K3_rcv-U5_N7_Slow_Addr_Undershoot.png

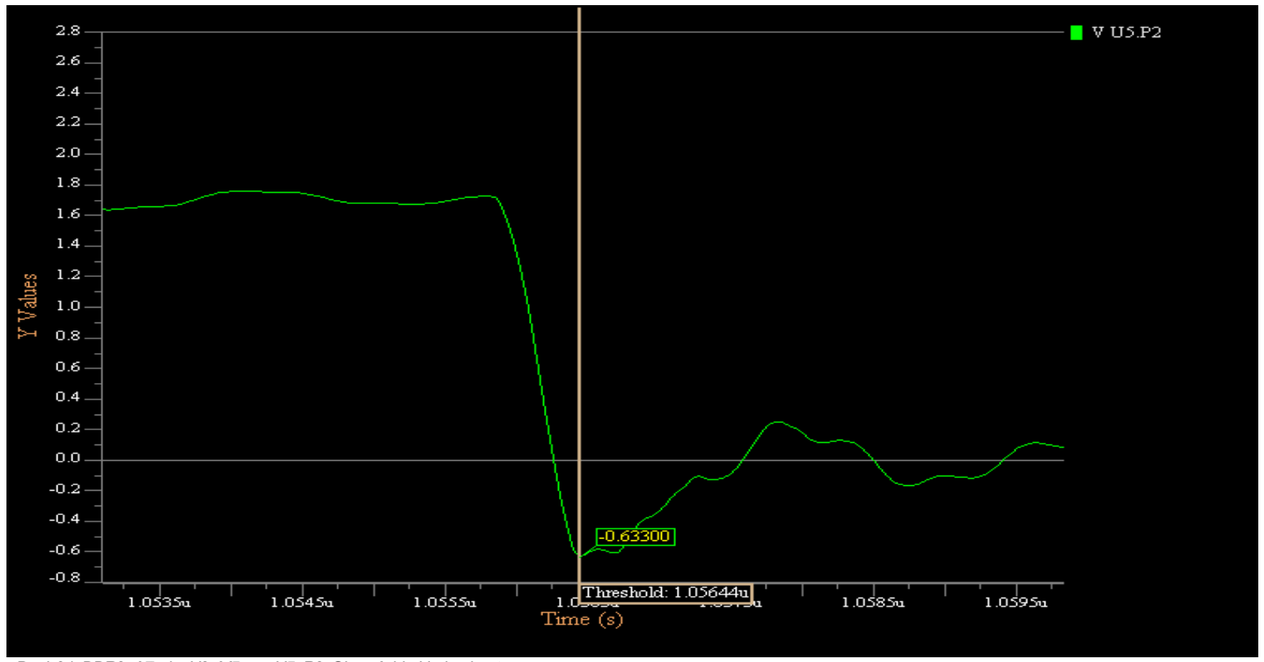
Return to table Launch in EZwave

/Bank34/DDR2_A7



_Bank34_DDR2_A7_drv-U2_M5_rcv-U5_P2_Slow_Addr_Overshoot.png

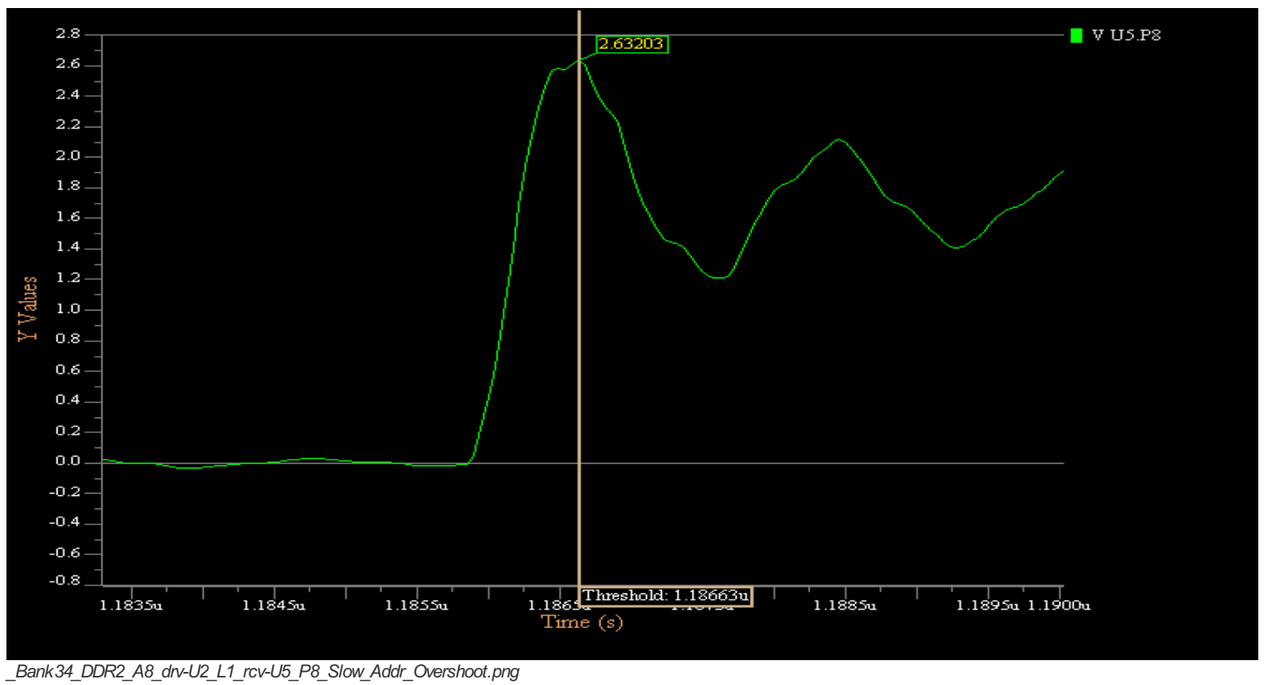
Return to table Launch in EZwave



_Bank34_DDR2_A7_drv-U2_M5_rcv-U5_P2_Slow_Addr_Undershoot.png

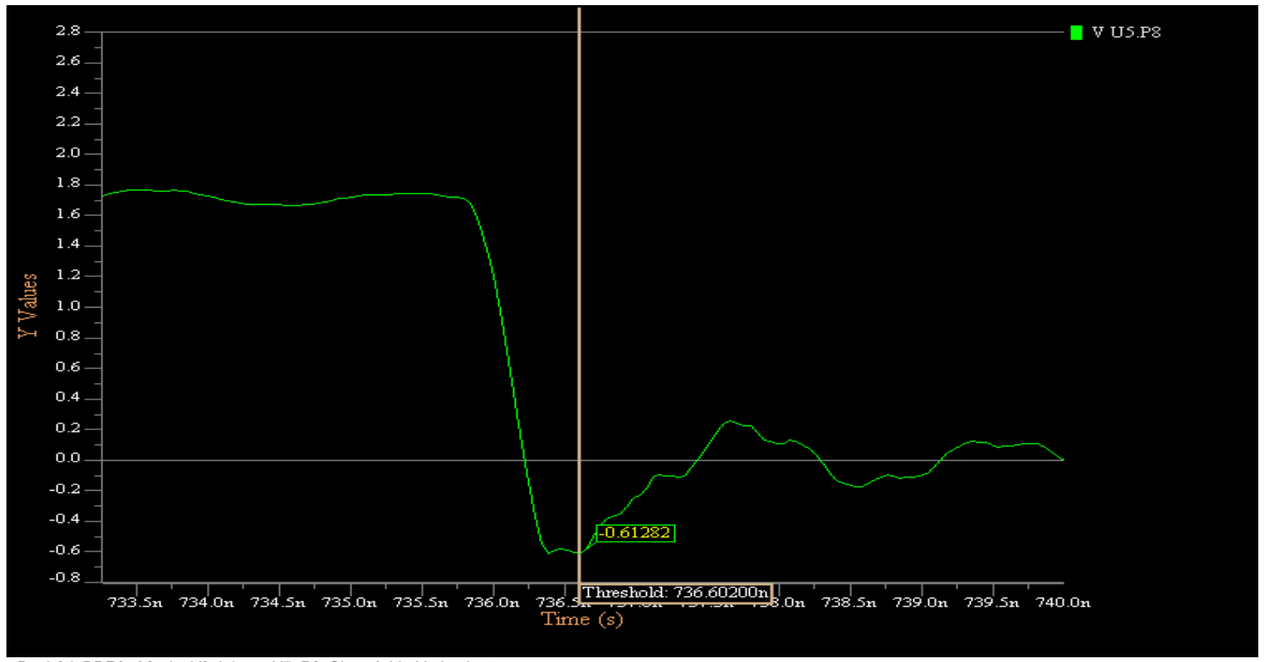
Return to table Launch in EZwave

/Bank34/DDR2_A8



_Bank34_DDR2_A8_drv-U2_L1_rcv-U5_P8_Slow_Addr_Overshoot.png

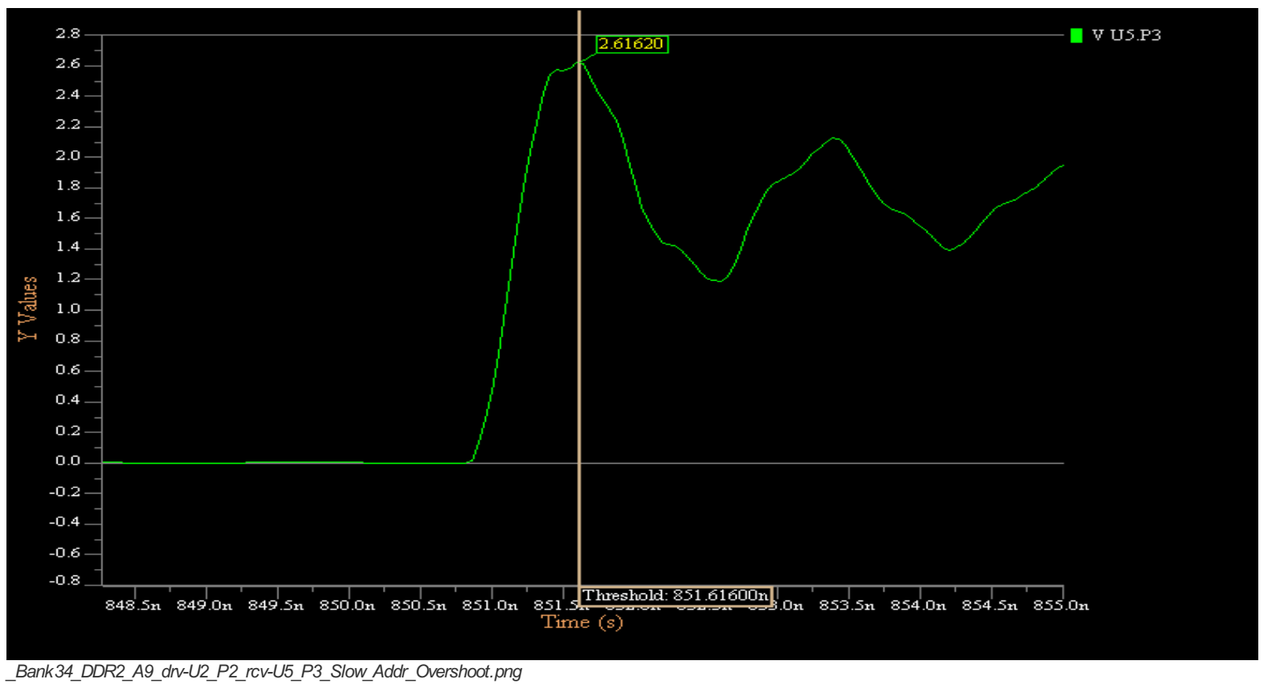
Return to table Launch in EZwave



_Bank34_DDR2_A8_drv-U2_L1_rcv-U5_P8_Slow_Addr_Undershoot.png

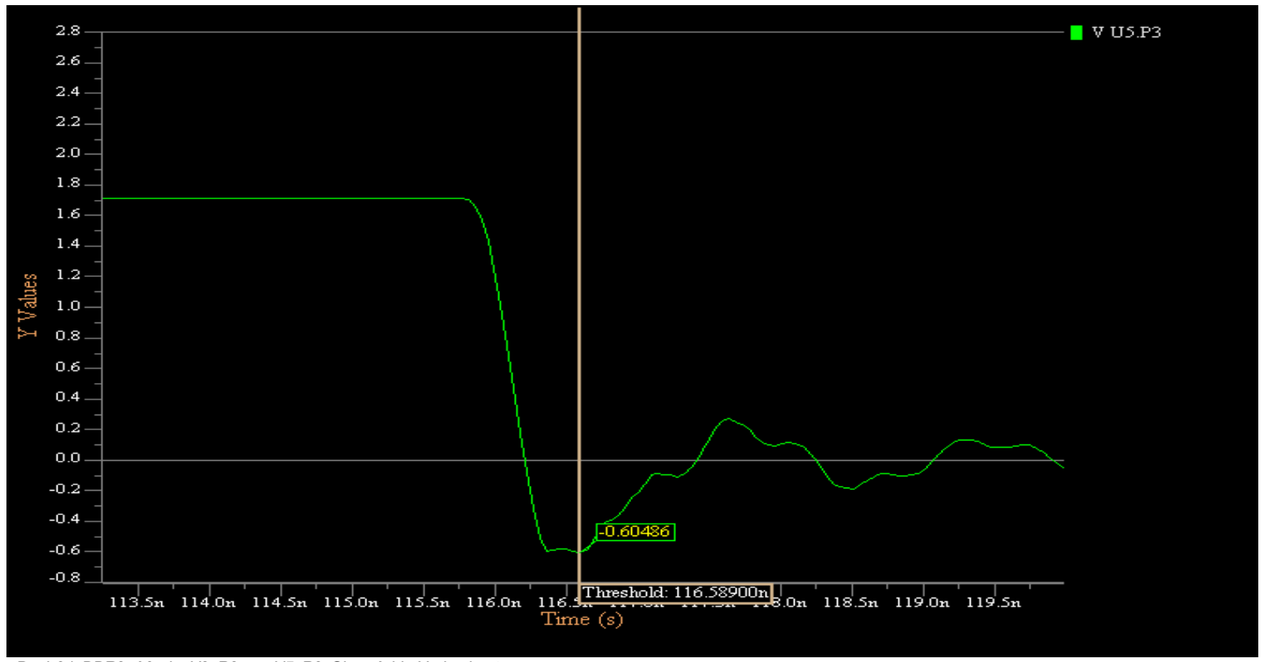
Return to table Launch in EZwave

/Bank34/DDR2_A9



_Bank34_DDR2_A9_drv-U2_P2_rcv-U5_P3_Slow_Addr_Overshoot.png

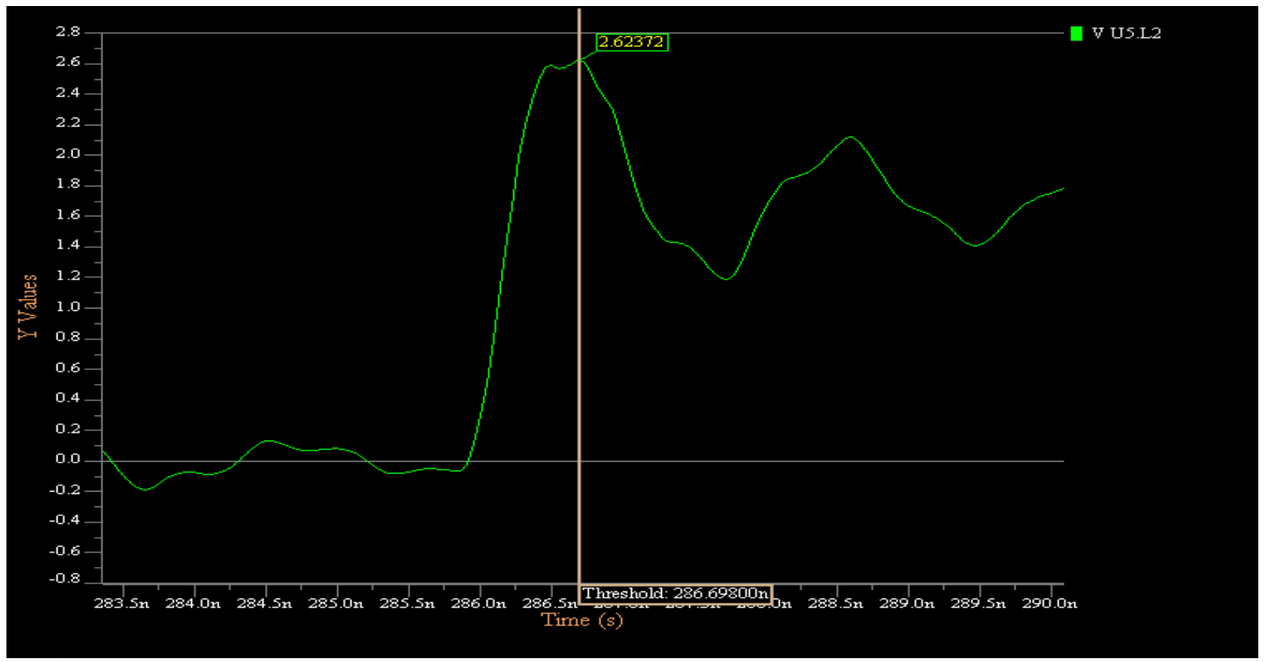
Return to table Launch in EZwave



_Bank34_DDR2_A9_drv-U2_P2_rcv-U5_P3_Slow_Addr_Undershoot.png

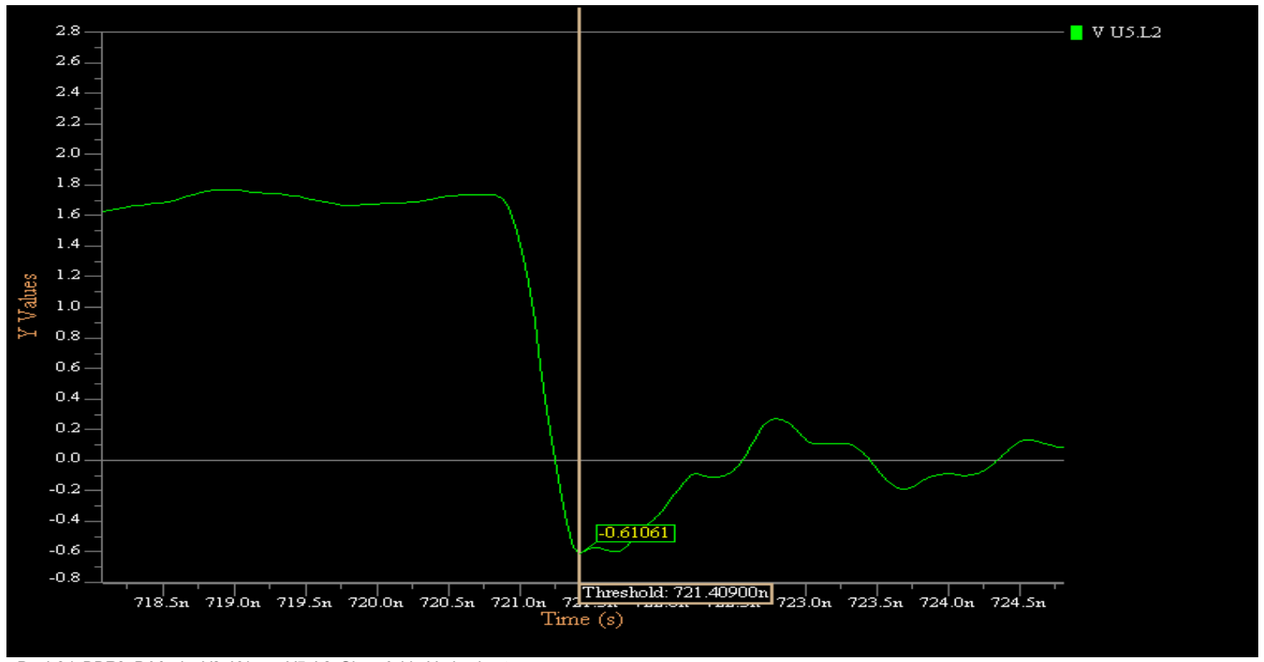
Return to table Launch in EZwave

/Bank34/DDR2_BA0



_Bank34_DDR2_BA0_drv-U2_K4_rcv-U5_L2_Slow_Addr_Overshoot.png

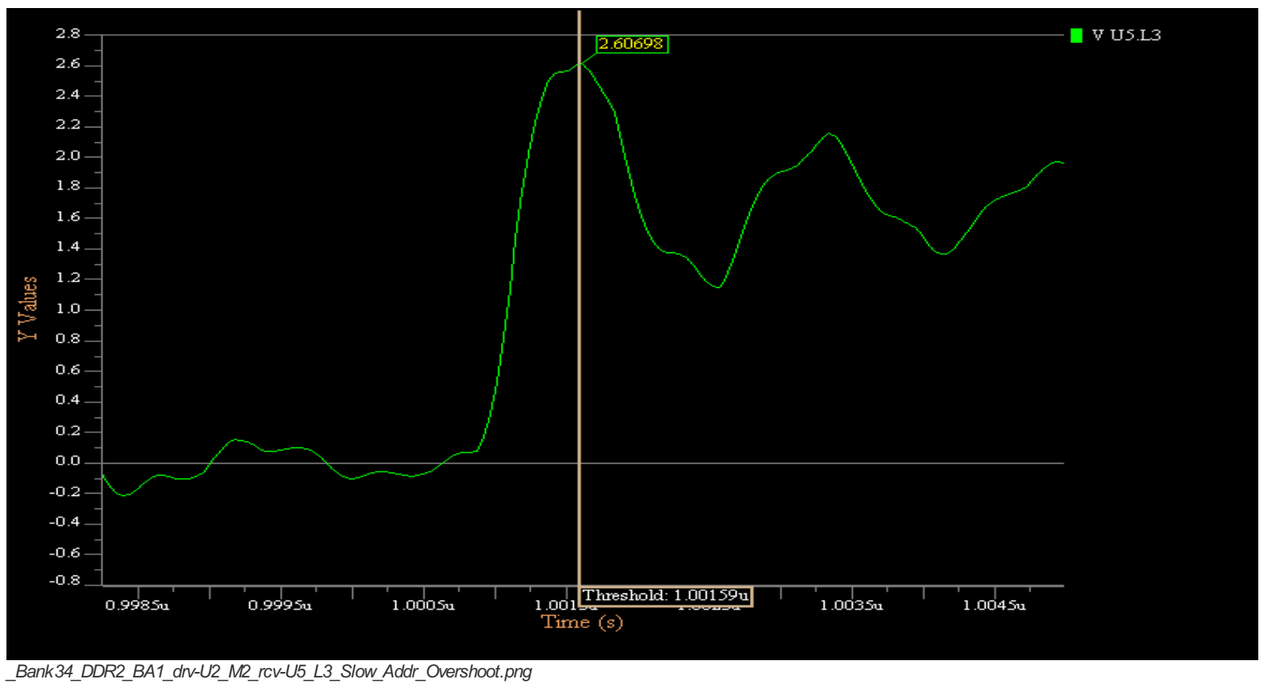
Return to table Launch in EZwave



_Bank34_DDR2_BA0_drv-U2_K4_rcv-U5_L2_Slow_Addr_Undershoot.png

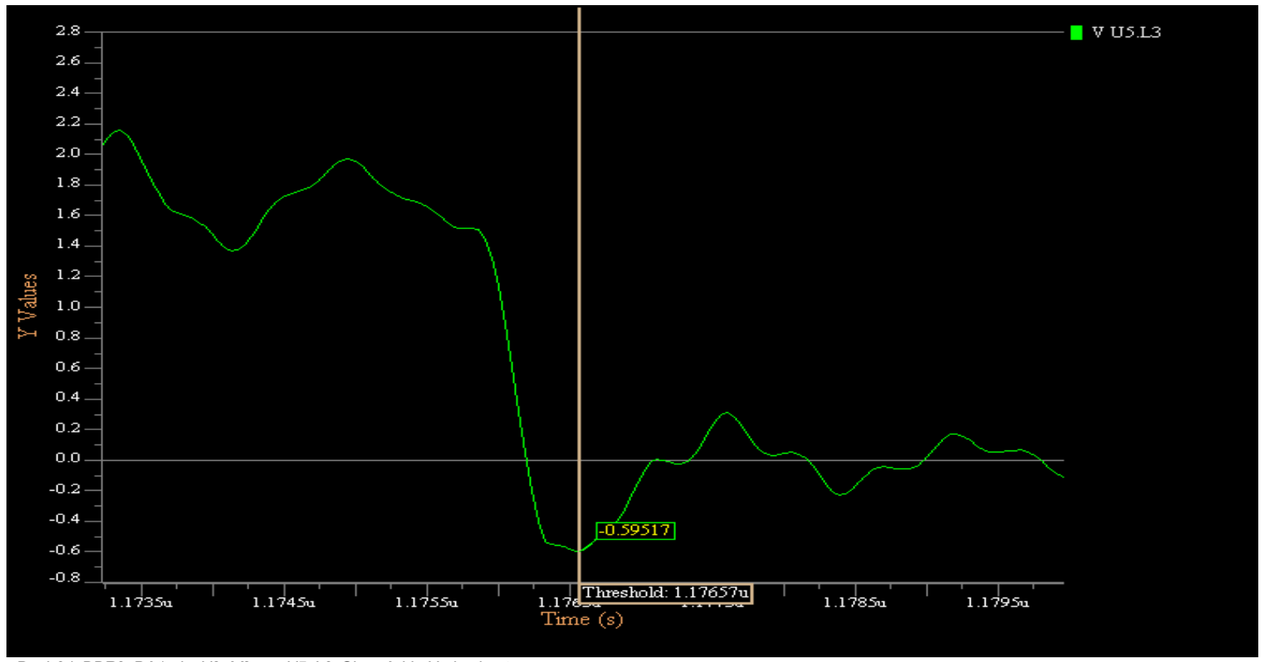
Return to table Launch in EZwave

/Bank34/DDR2_BA1



_Bank34_DDR2_BA1_drv-U2_M2_rcv-U5_L3_Slow_Addr_Overshoot.png

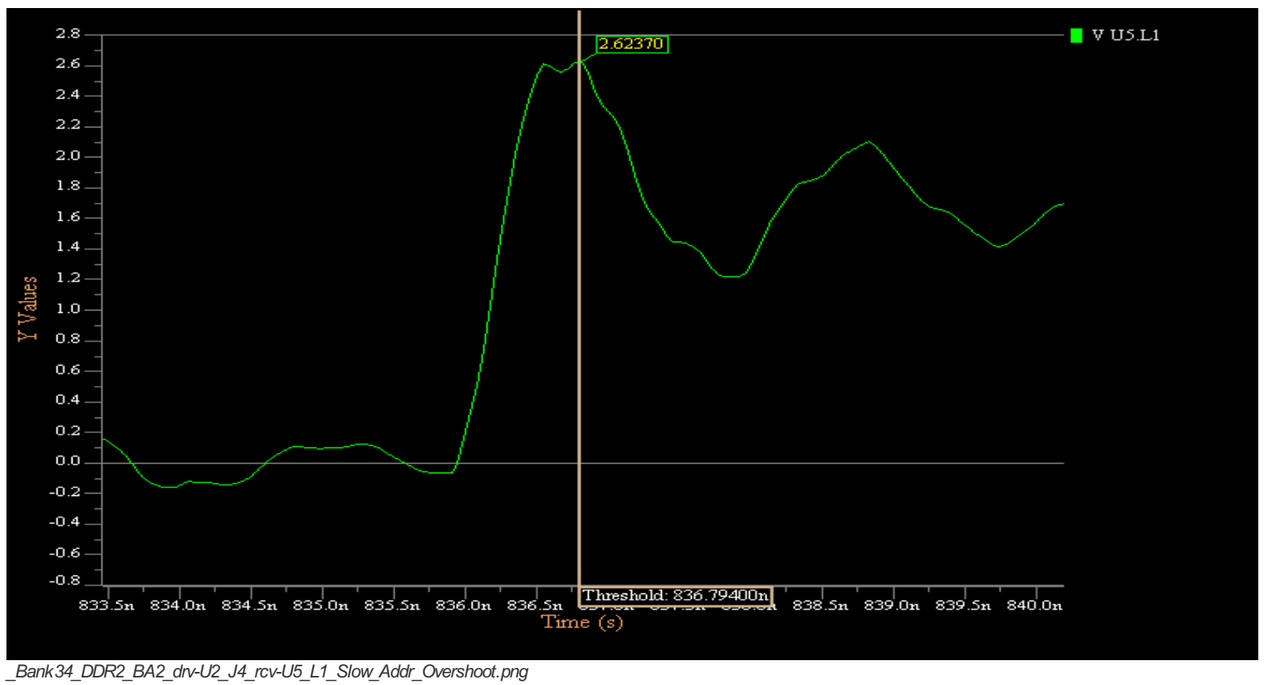
Return to table Launch in EZwave



_Bank34_DDR2_BA1_drv-U2_M2_rcv-U5_L3_Slow_Addr_Undershoot.png

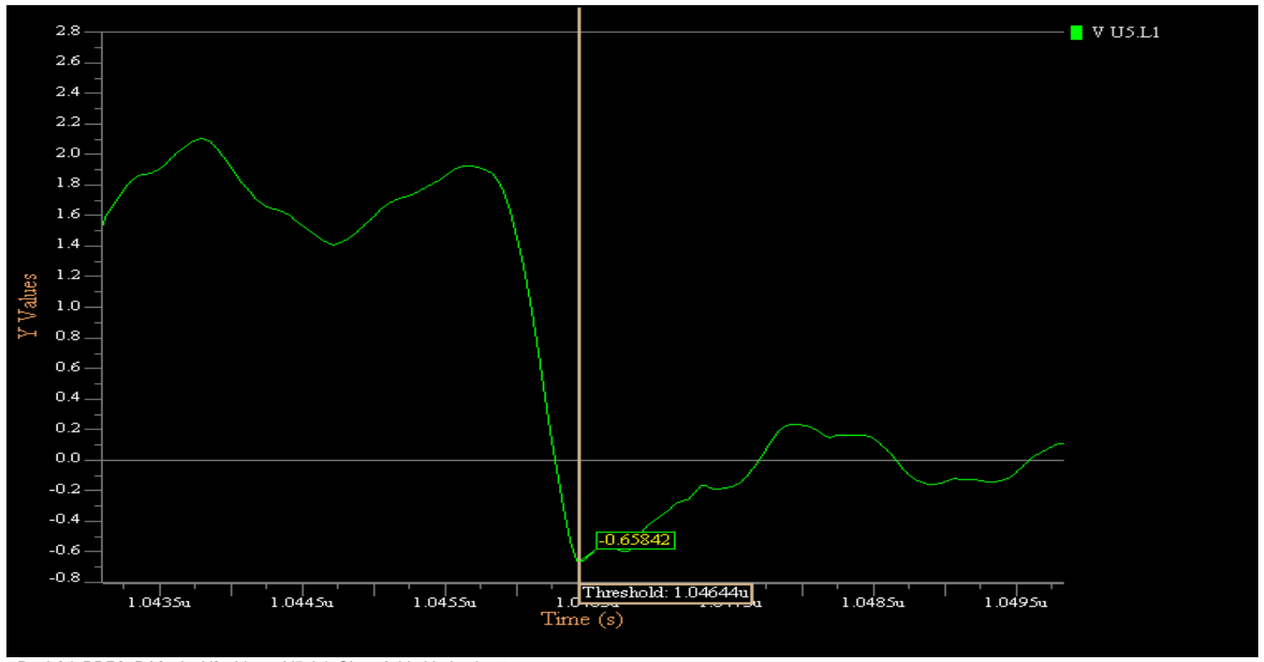
Return to table Launch in EZwave

/Bank34/DDR2_BA2



_Bank34_DDR2_BA2_drv-U2_J4_rcv-U5_L1_Slow_Addr_Overshoot.png

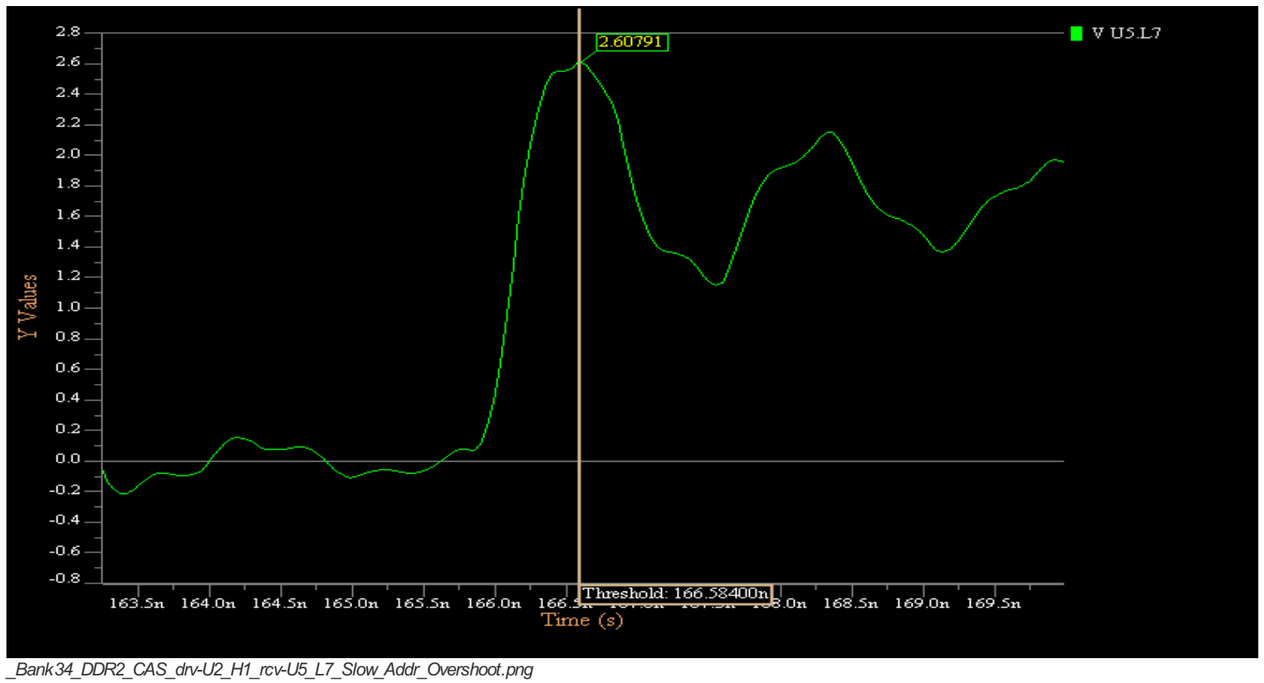
Return to table Launch in EZwave



_Bank34_DDR2_BA2_drv-U2_J4_rcv-U5_L1_Slow_Addr_Undershoot.png

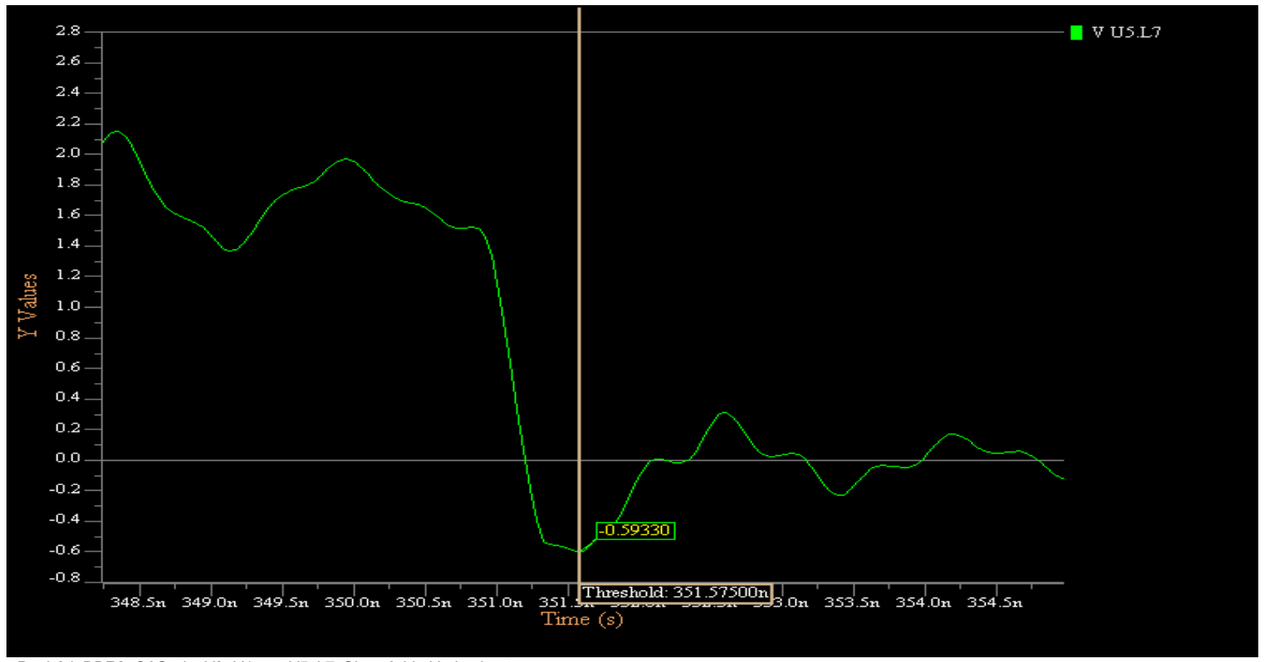
Return to table Launch in EZwave

/Bank34/DDR2_CAS



_Bank34_DDR2_CAS_drv-U2_H1_rcv-U5_L7_Slow_Addr_Overshoot.png

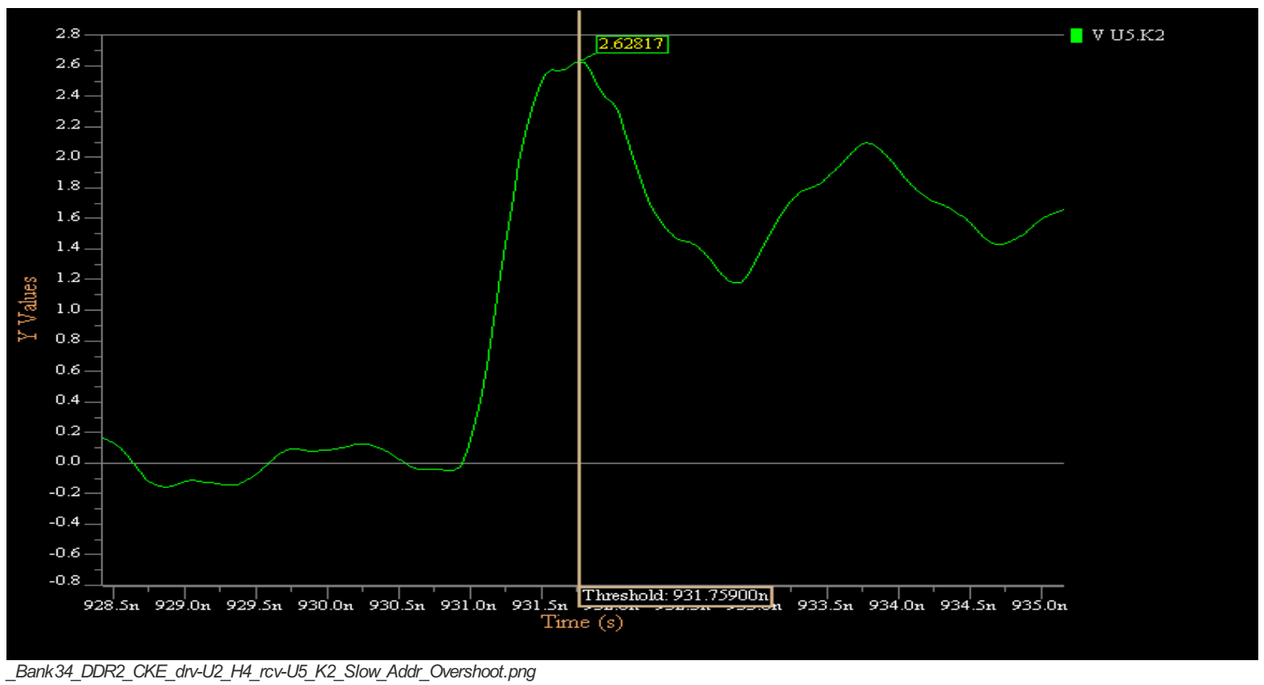
Return to table Launch in EZwave



_Bank34_DDR2_CAS_drv-U2_H1_rcv-U5_L7_Slow_Addr_Undershoot.png

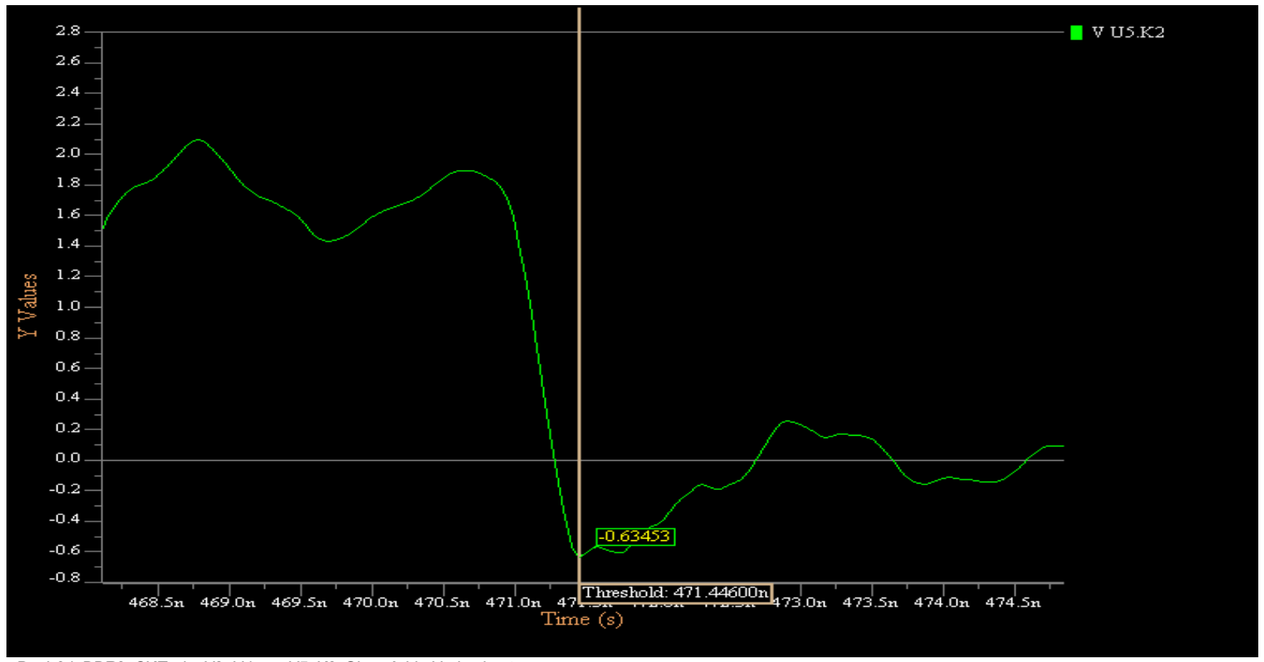
Return to table Launch in EZwave

/Bank34/DDR2_CKE



_Bank34_DDR2_CKE_drv-U2_H4_rcv-U5_K2_Slow_Addr_Overshoot.png

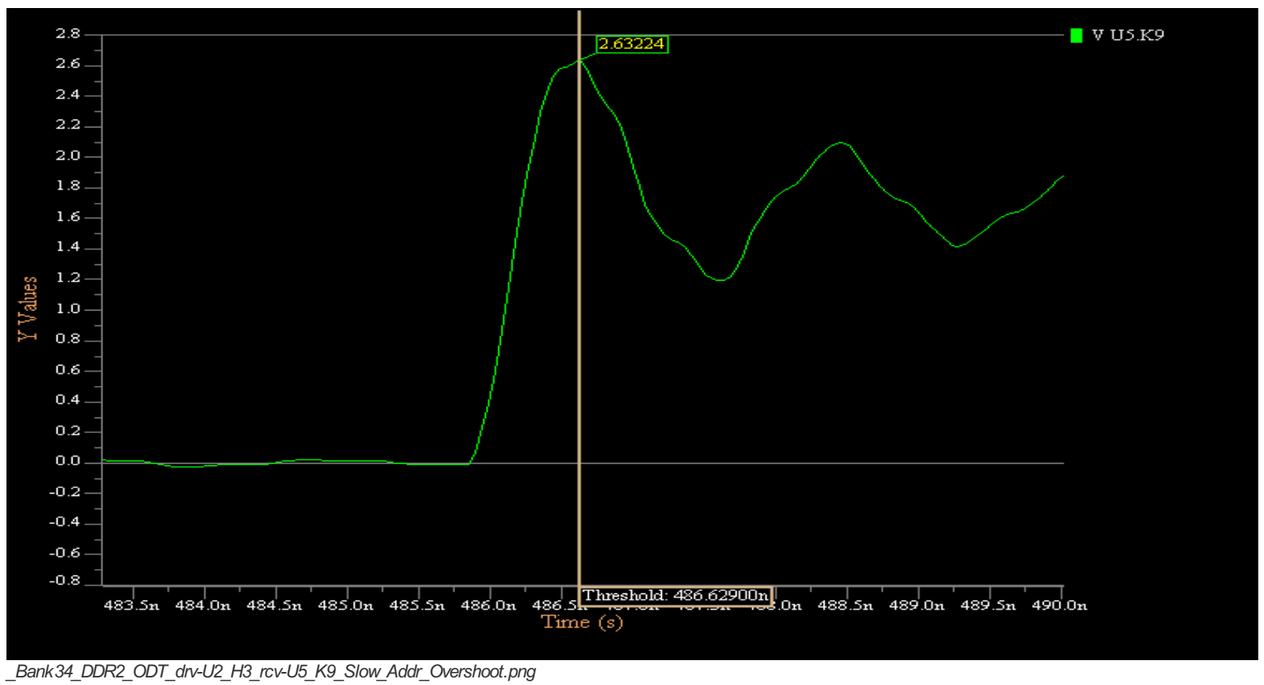
Return to table Launch in EZwave



_Bank34_DDR2_CKE_drv-U2_H4_rcv-U5_K2_Slow_Addr_Undershoot.png

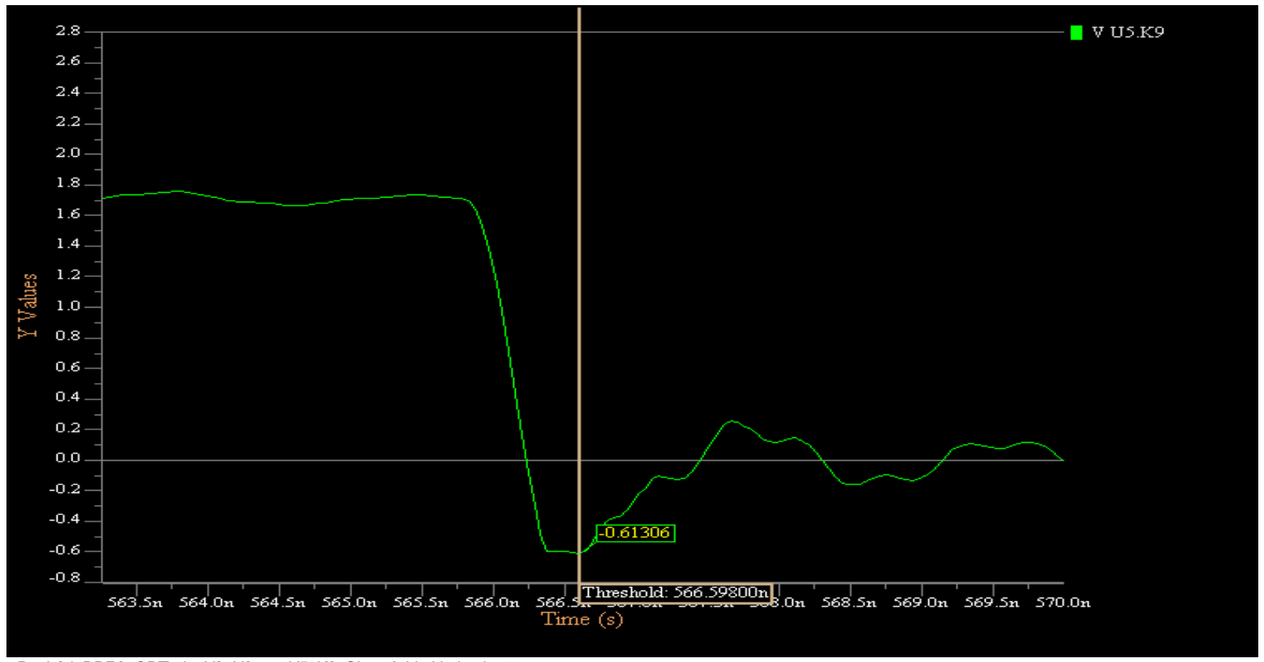
Return to table Launch in EZwave

/Bank34/DDR2_ODT



_Bank34_DDR2_ODT_drv-U2_H3_rcv-U5_K9_Slow_Addr_Overshoot.png

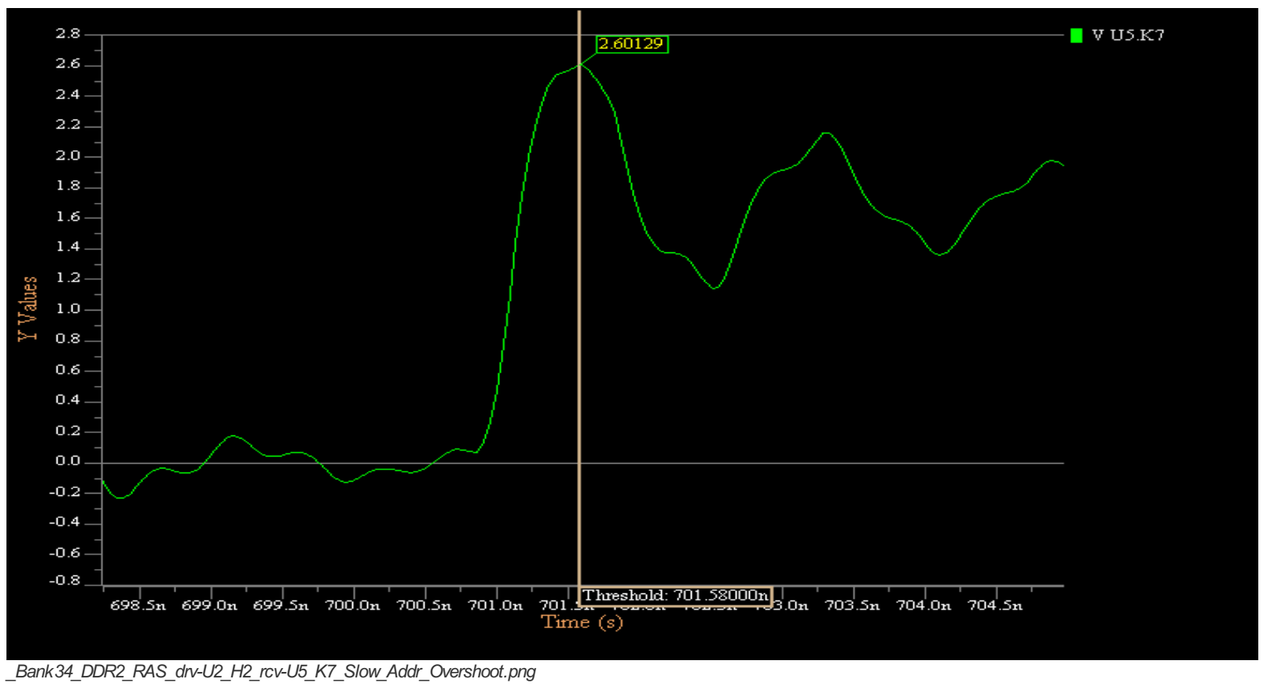
Return to table Launch in EZwave



_Bank34_DDR2_ODT_drv-U2_H3_rcv-U5_K9_Slow_Addr_Undershoot.png

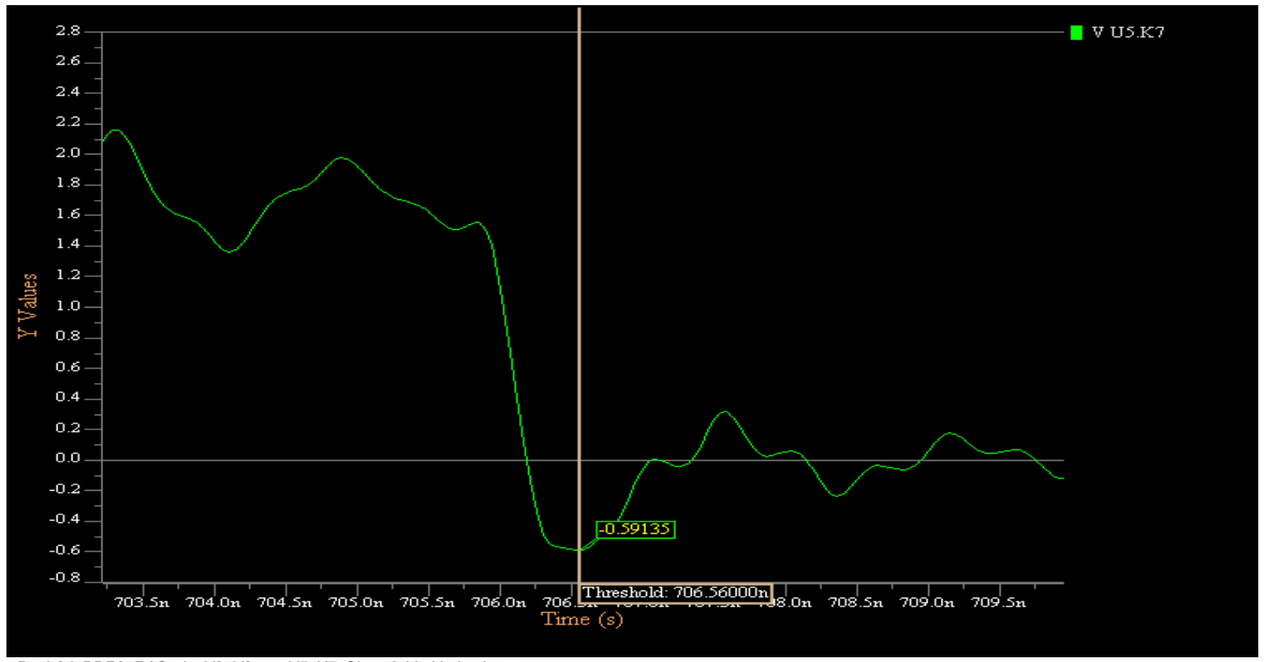
Return to table Launch in EZwave

/Bank34/DDR2_RAS



_Bank34_DDR2_RAS_drv-U2_H2_rcv-U5_K7_Slow_Addr_Overshoot.png

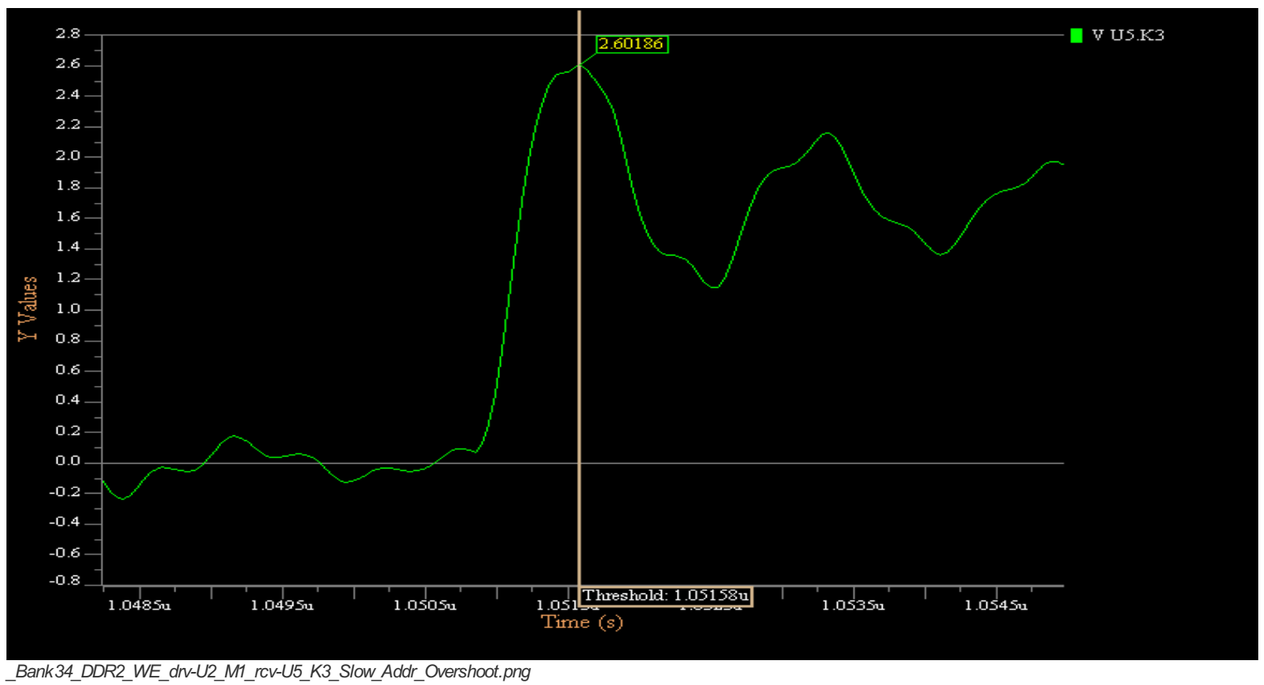
Return to table Launch in EZwave



_Bank34_DDR2_RAS_drv-U2_H2_rcv-U5_K7_Slow_Addr_Undershoot.png

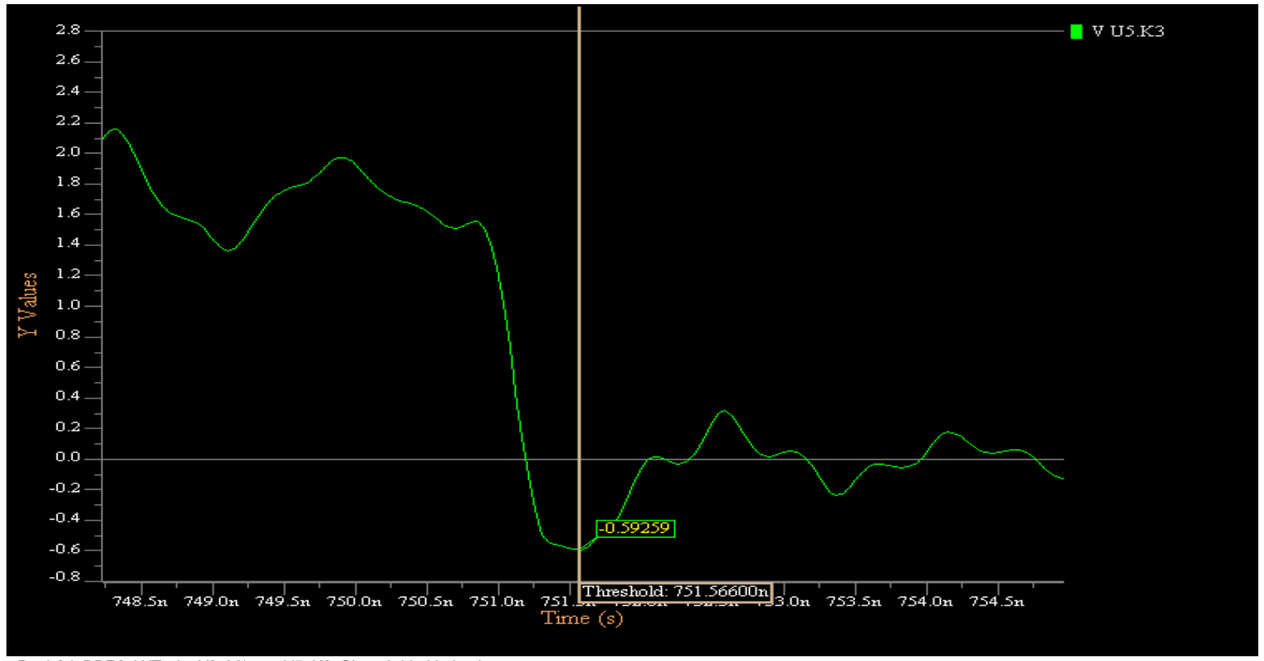
Return to table Launch in EZwave

/Bank34/DDR2_WE



_Bank34_DDR2_WE_drv-U2_M1_rcv-U5_K3_Slow_Addr_Overshoot.png

Return to table Launch in EZwave



_Bank34_DDR2_WE_drv-U2_M1_rcv-U5_K3_Slow_Addr_Undershoot.png

Return to table Launch in EZwave