PEEL™ 16CV8 PROGRAM/VERIFY SPECIFICATION

Revision 2.0, September 15, 2000

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Revision Number	Date	Description
1-1	6/2/94	Changed SYN and ACO bit position
1-2	9/1/94	Changed SYN to MSO Changed ACO to MSI Changed XOR and ACI to OP and RC Revised Register mode algorithms on Table17, 19-1 and 20
2.0	9/15/00	Complete Re-write of Spec.

PEEL™ 16CV8 Program/Verify Specification Revision History

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1 Introduction

This document contains the necessary technical specifications for proper program/verify operation of the PEEL™ 16CV8 Programmable Electrically Erasable Logic Device. Information provided assumes the reader has general knowledge of PLDs. It is recommended to use the PEEL™ 16CV8 datasheet in conjunction with this specification.

Note: The specification includes the “fast program” byte mode algorithm (See Table 10) that typically reduces programming time by 90%.

2 Pre-Conditioning

The PEEL™ 16CV8 requires a pre-conditioning prior to programming. The pre-conditioning, which ensures better reliability in the PEEL™ 16CV8, involves the ERASE ALL and PROGRAM (WRITE) ALL modes. (See Figure 1)

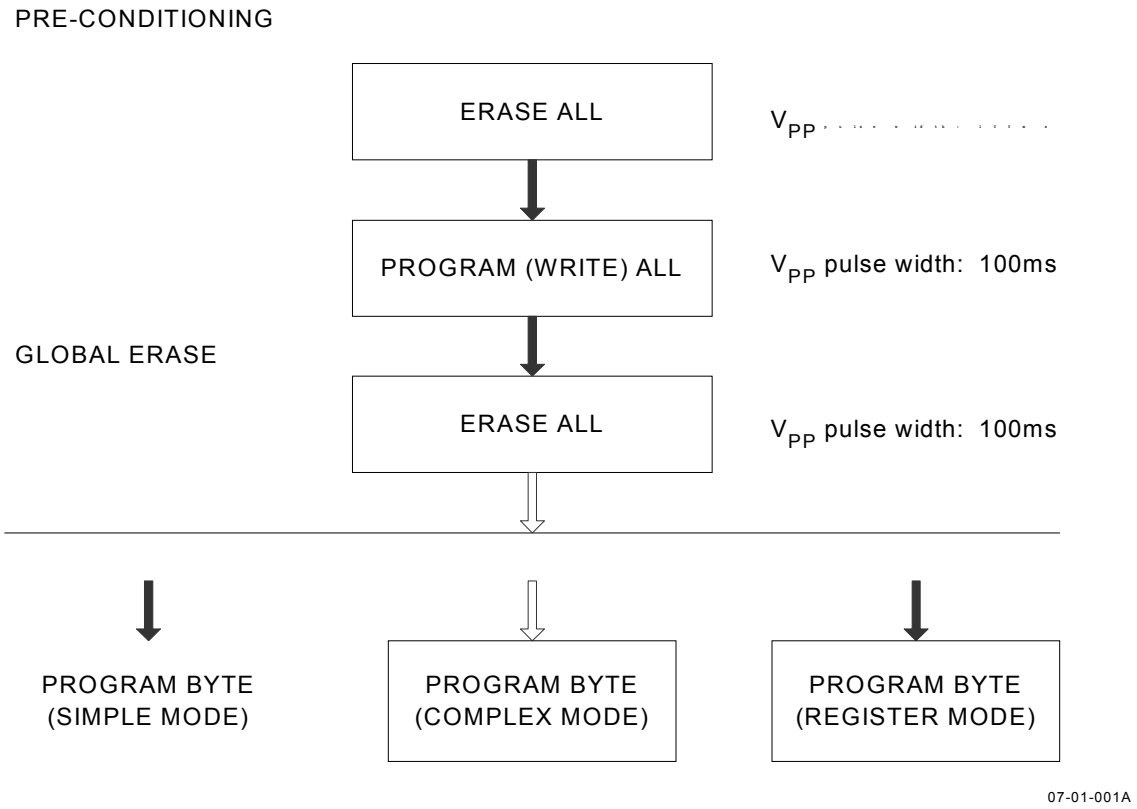

Figure 1 Preconditioning Flowchart

3 Program/Verify Operation Description

Program/Verify operation of the PEEL™ 16CV8 Programmable Electrically Erasable Logic Device is similar to that of other CMOS PLDs that use a parallel interface scheme. The PEEL™ 16CV8 can be enabled for program and verification by raising and holding pin 1 to V_{HH1}. Doing this will cause the pin functions of the 16CV8 to change from normal operation to program/verify operation as shown in the pin connection diagram and table, Figure 2 and Table 2, respectively. Four of the pins (PVE, PVP, SEC/OD and ALE/ERA) use high voltage levels to implement specific program/verify functions. All other pins use standard TTL levels with the exception of V_{CC} and GND, which must be maintained at +5V and ground, respectively.

A total of 2194 programmable electrically erasable cells are used to configure the PEEL™ 16CV8. The numbers on the logic array diagrams in Figure 4, Figure 5 and Figure 6 designate the order each E2 cell is programmed via the JEDEC "fuse" map. Table 4 contains the conversion formula and examples from device Product Term and Line number to Fuse Number

Note that since the PEEL™ 16CV8 does not use actual fuses as with bipolar technology, the term fuse is used here purely for the sake of convention. An example JEDEC fuse map file is shown in Figure 7

These are four primary modes used in program/verify operation; program byte, verify byte, erase-all and set security bit. The selection of these modes is controlled by the MODE A-B pin. Depending on the mode selected, an input line address (IAD0-7) and term group address (TGA0-3) must be set to a specific value as listed in program/verify Table 5, Table 6 and Table 7. Besides input addressing, the multiplexed IAD0-7 pins are also used for programming fuse state data from the JEDEC fuse map.

Also, there are three global configuration modes **Simple, Complex and Register**. The selection of these modes is controlled by two global bits, **MS0 and MS1** for all macro cell configurations.

MS0	MS1	Mode
1	0	Simple
1	1	Complex
0	1	Register

Table 1 Mode Select Bit Configuration

Note: The mapping to IAD address and "Fuse State" values are different for each operating mode (Simple, Complex and Register). Please note the appropriate mode when mapping information in Table 5 to Table 9.

When reading (verifying) data from the PEEL™ 16CV8, a 0 data bit equals a "connected fuse" and a 1 equals an "open fuse" as with the standard JEDEC fuse map convention. However, when writing (programming) data to the PEEL™ 16CV8, data must first be inverted from that of the JEDEC map for correct program operation. This inversion is handled in Table 10 Fast Program Byte Mode Flow

After the PEEL™ 16CV8 is erased, the "fuse states" will all be open. The macro cell after pre-program initialization will set Input/Feedback to "Bi-Directional I/O" and output to "Combinatorial Output and Active Low".

De-multiplexing of the IAD0-7 is accomplished using the SEC/OD and ALE/ERA pins in conjunction with the PVP pin. ALE/ERA latches the address when raised to V_{IH}. SEC/OD disables the I/O's when raised to V_{IH}. Before ALE/ERA and SEC/OD can be brought back to V_{IL}, the PVP pin must be raised to V_{HH2} (ramp is not required for verify operation) and maintain at V_{HH2} for 10uS. The ALE/ERA pin also serves as an enable for the erase-all mode when raised to V_{HH2}. Likewise, the SEC/OD pin when raised to V_{HH2} enables the set security bit mode. Once the security bit is set, verification is not possible until the erase-all mode is again implemented.

The PVP (program/verify pulse) pin is the primary gating pulse for any mode of operation. Once all other conditions are set up, PVP is raised to V_{HH3} and then ramped to the V_{HH2} high voltage level at a 50uS/V or greater rise time. If the program byte or erase-all modes have been selected, the pulse on PVP must be maintained at V_{HH2} for 10ms. If the security mode has been selected, the pulse on PVP must be maintained at V_{HH2} for 300ms. During verify mode, however, PVP need only be held high for 10uS. Less crucial than the rise time, the fall time of PVP can be 1uS or greater. For a complete understanding of the PEEL™ 16CV8 programming signals and their relative timings, please refer to the Program/Verify Parameters and Waveform Timing starting in Section 5 of this specification.

For the convenience of deciphering the PEEL™ 16CV8 programming algorithms, the procedural flow for each of the four modes is shown in Table 10 through Table 14. Note that the PEEL™ 16CV8 should always be erased first before programming any "fuse state" data. Additionally, it is best to start with all pins in a low (V_{IL}) state and then proceed with the program/verify operation.

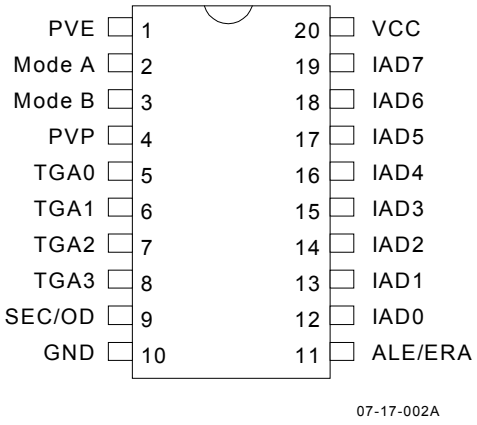

Figure 2 PEEL™16CV8 Program/Verify Pin Configuration

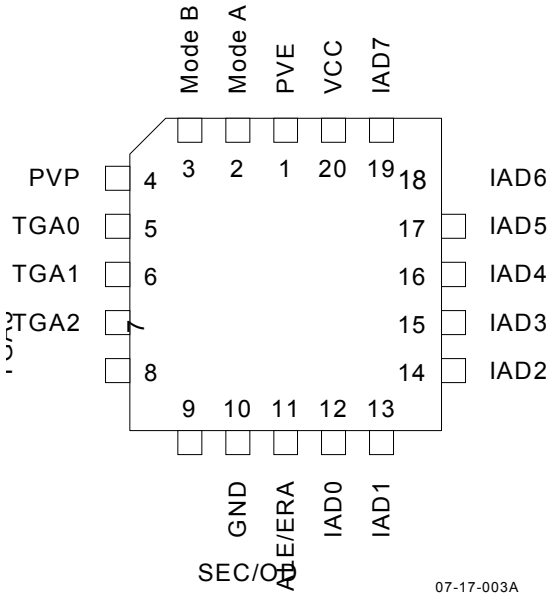

Figure 3 PEEL™16CV8 PLCC Program/Verify Pin Configuration

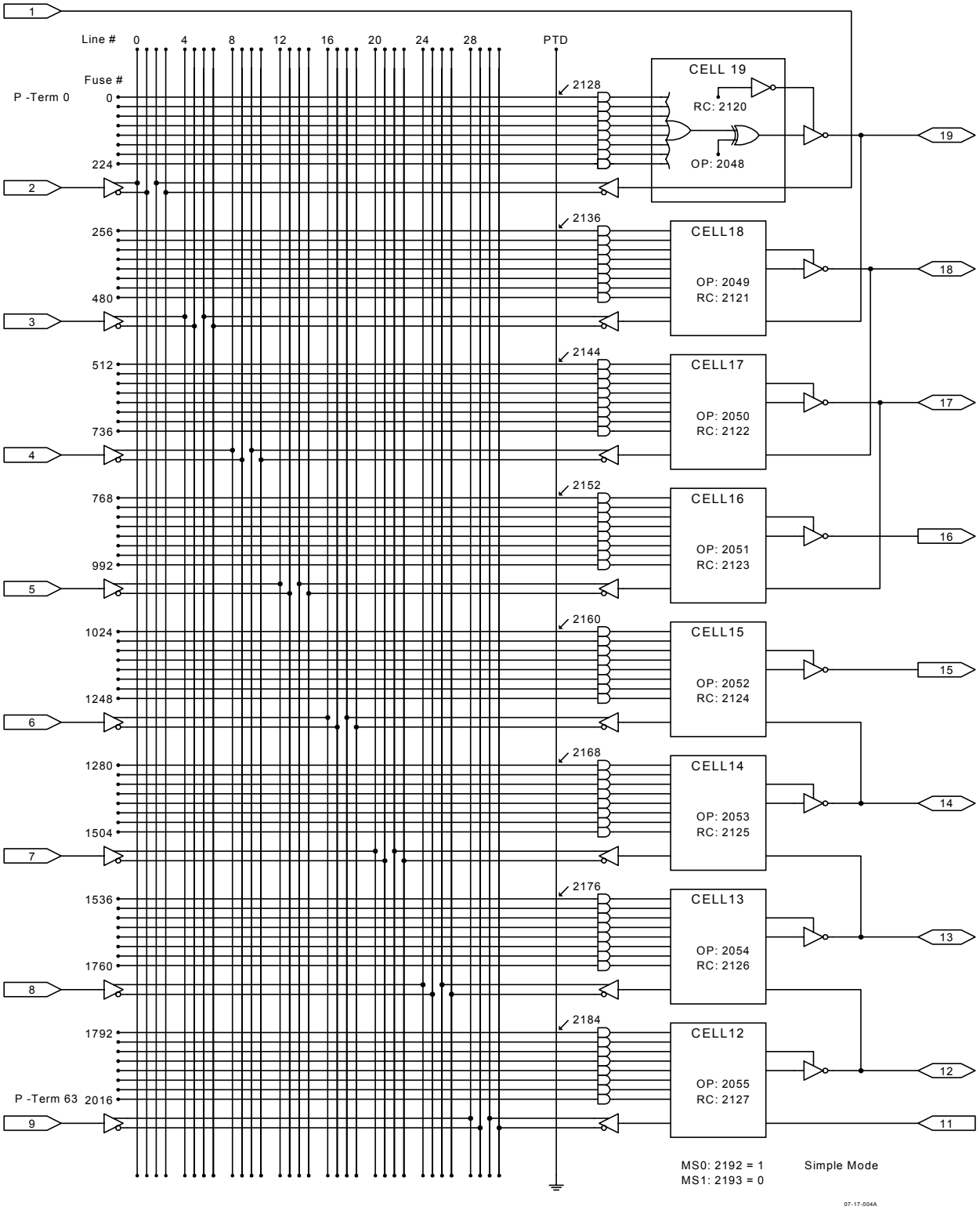

Figure 4 Logic Array Diagram With Fuse Map Numbers (Simple Mode)

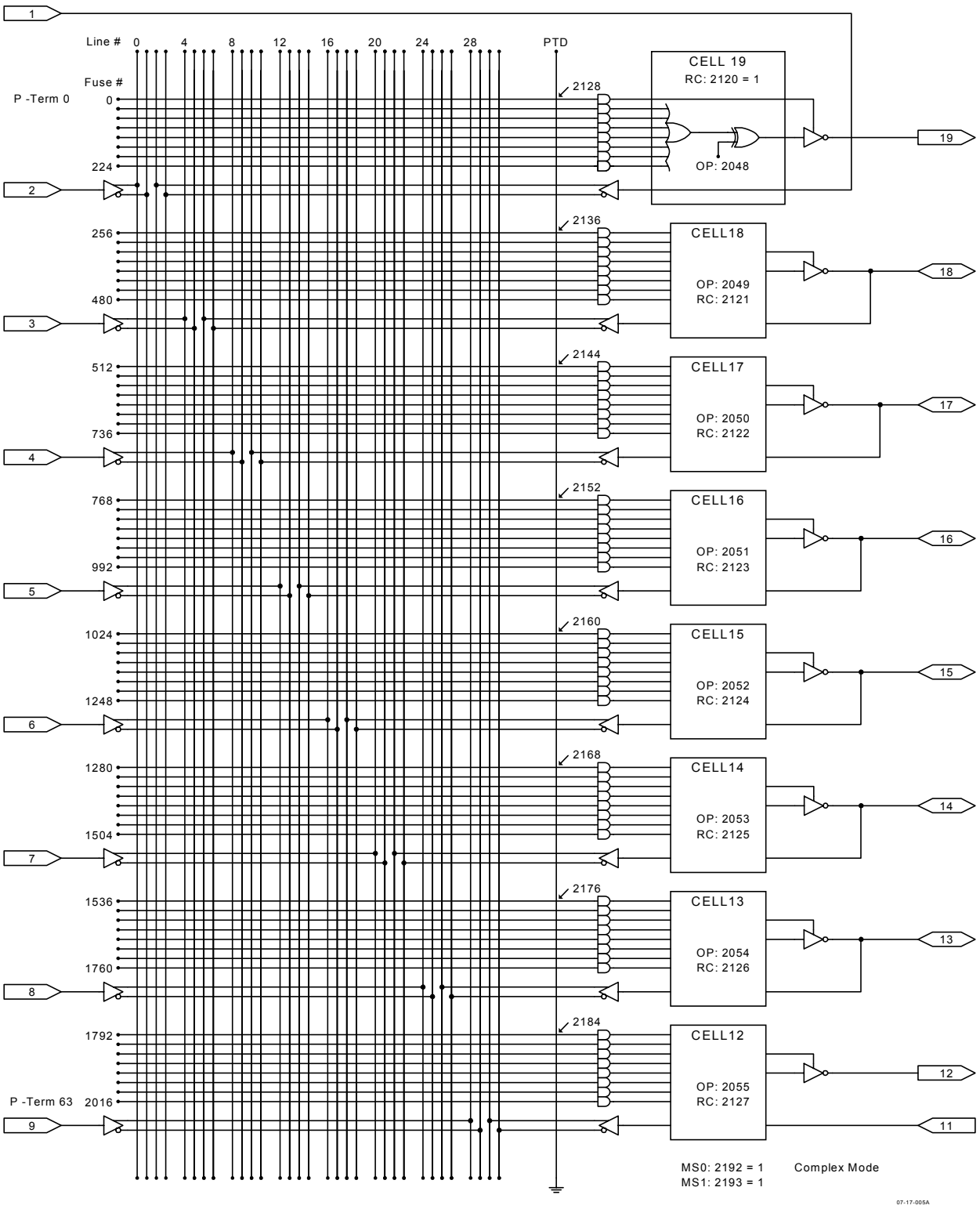

Figure 5 Logic Array Diagram with Map Numbers (Complex Mode)

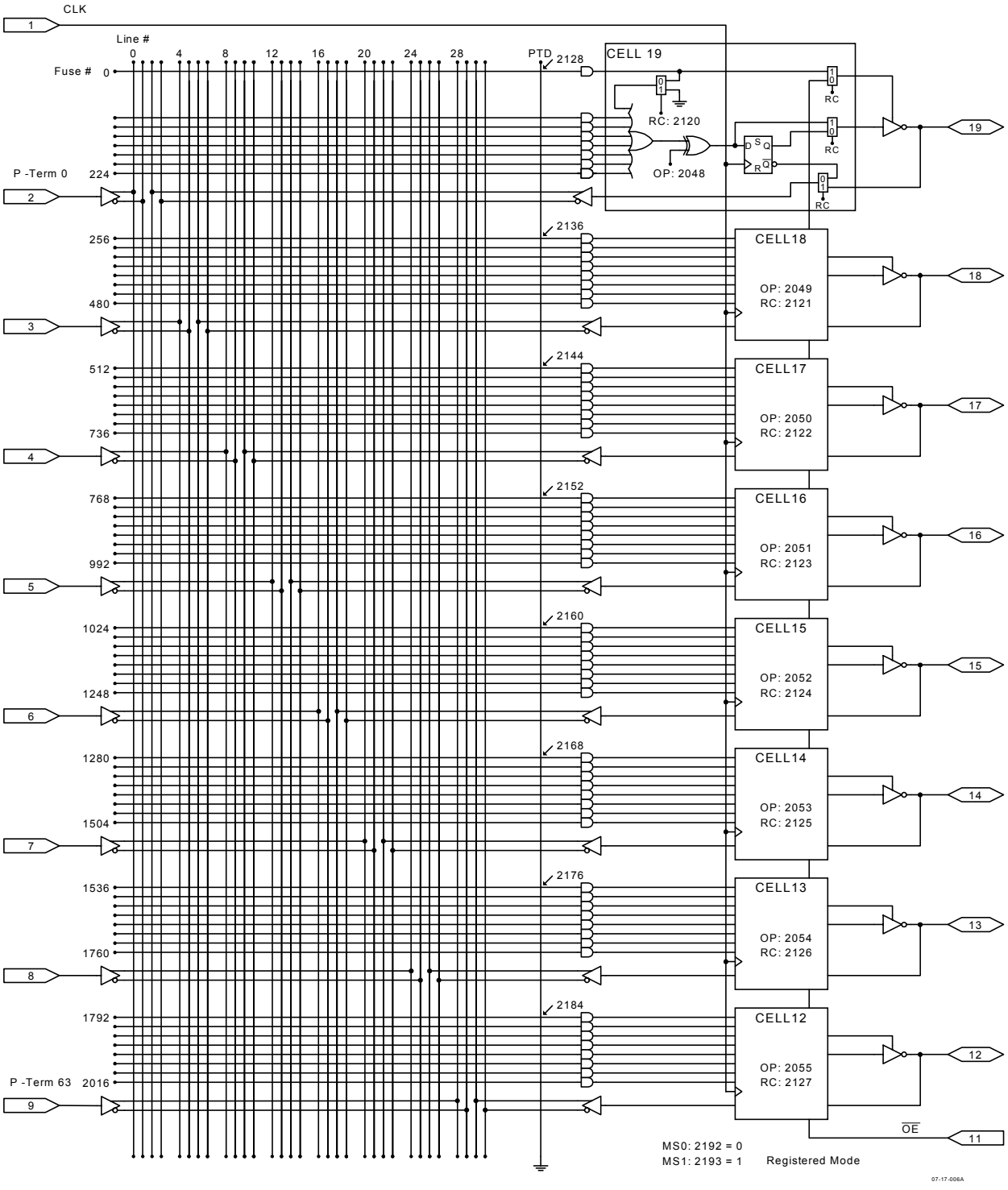

Figure 6 Logic Array Diagram with Map Numbers (Register Mode)

Table 2 Program/Verify Pin Configuration

Pin #	Name	Function
1	PVE	Program/Verify Enable
2,3	MODE A-B	Erase, Write And Verify Mode Selection
4	PVP	Program/Verify Pulse
5-8	TGA 0-3	Term Group Address
9	SEC/OD	Security Enable/Output Disable
10	GND	Ground
11	ALE/ERA	Input Address Latch/Erase Enable
12-19	IAD 0-7	Input Address/Term Group Data (Fuse Data)
20	V_{CC}	Power Supply (+5v)

Figure 7 Example JEDEC Fuse Map For The PEEL™ 16CV8

```
DF PEEL
DD 16CV8*
DM ICT*
*QP20
*QF2194
*F1
L0000 0101 0101 0101 0101 0101 0101 0101 0101 *
L0032 0101 0101 0101 0101 0101 0101 0101 0101 *
L0064 0101 0101 0101 0101 0101 0101 0101 0101 *
L0096 0101 0101 0101 0101 0101 0101 0101 0101 *
L0128 0101 0101 0101 0101 0101 0101 0101 0101 *
L0160 0101 0101 0101 0101 0101 0101 0101 0101 *
L0192 0101 0101 0101 0101 0101 0101 0101 0101 *
L0224 0101 0101 0101 0101 0101 0101 0101 0101 *

L0256 0101 0101 0101 0101 0101 0101 0101 0101 *
L0288 0101 0101 0101 0101 0101 0101 0101 0101 *
L0320 0101 0101 0101 0101 0101 0101 0101 0101 *
L0352 0101 0101 0101 0101 0101 0101 0101 0101 *
L0384 0101 0101 0101 0101 0101 0101 0101 0101 *
L0416 0101 0101 0101 0101 0101 0101 0101 0101 *
L0448 0101 0101 0101 0101 0101 0101 0101 0101 *
L0480 0101 0101 0101 0101 0101 0101 0101 0101 *

L0512 0101 0101 0101 0101 0101 0101 0101 0101 *
L0544 0101 0101 0101 0101 0101 0101 0101 0101 *
L0576 0101 0101 0101 0101 0101 0101 0101 0101 *
L0608 0101 0101 0101 0101 0101 0101 0101 0101 *
L0640 0101 0101 0101 0101 0101 0101 0101 0101 *
L0672 0101 0101 0101 0101 0101 0101 0101 0101 *
L0704 0101 0101 0101 0101 0101 0101 0101 0101 *
L0736 0101 0101 0101 0101 0101 0101 0101 0101 *

L0768 0101 0101 0101 0101 0101 0101 0101 0101 *
L0800 0101 0101 0101 0101 0101 0101 0101 0101 *
L0832 0101 0101 0101 0101 0101 0101 0101 0101 *
L0864 0101 0101 0101 0101 0101 0101 0101 0101 *
L0928 0101 0101 0101 0101 0101 0101 0101 0101 *
L0960 0101 0101 0101 0101 0101 0101 0101 0101 *
L0992 0101 0101 0101 0101 0101 0101 0101 0101 *

L1024 0101 0101 0101 0101 0101 0101 0101 0101 *
L1056 0101 0101 0101 0101 0101 0101 0101 0101 *
L1088 0101 0101 0101 0101 0101 0101 0101 0101 *
```

```
L1120 0101 0101 0101 0101 0101 0101 0101 0101 *
L1152 0101 0101 0101 0101 0101 0101 0101 0101 *
L1184 0101 0101 0101 0101 0101 0101 0101 0101 *
L1216 0101 0101 0101 0101 0101 0101 0101 0101 *
L1248 0101 0101 0101 0101 0101 0101 0101 0101 *

L1280 0101 0101 0101 0101 0101 0101 0101 0101 *
L1312 0101 0101 0101 0101 0101 0101 0101 0101 *

L1344 0101 0101 0101 0101 0101 0101 0101 0101 *
L1376 0101 0101 0101 0101 0101 0101 0101 0101 *
L1408 0101 0101 0101 0101 0101 0101 0101 0101 *
L1440 0101 0101 0101 0101 0101 0101 0101 0101 *
L1472 0101 0101 0101 0101 0101 0101 0101 0101 *
L1504 0101 0101 0101 0101 0101 0101 0101 0101 *
L1536 0101 0101 0101 0101 0101 0101 0101 0101 *
L1568 0101 0101 0101 0101 0101 0101 0101 0101 *
L1600 0101 0101 0101 0101 0101 0101 0101 0101 *
L1632 0101 0101 0101 0101 0101 0101 0101 0101 *
L1664 0101 0101 0101 0101 0101 0101 0101 0101 *
L1696 0101 0101 0101 0101 0101 0101 0101 0101 *
L1728 0101 0101 0101 0101 0101 0101 0101 0101 *
L1760 0101 0101 0101 0101 0101 0101 0101 0101 *

L1792 0101 0101 0101 0101 0101 0101 0101 0101 *
L1824 0101 0101 0101 0101 0101 0101 0101 0101 *
L1856 0101 0101 0101 0101 0101 0101 0101 0101 *
L1888 0101 0101 0101 0101 0101 0101 0101 0101 *
L1920 0101 0101 0101 0101 0101 0101 0101 0101 *
L1952 0101 0101 0101 0101 0101 0101 0101 0101 *
L1984 0101 0101 0101 0101 0101 0101 0101 0101 *
L2016 0101 0101 0101 0101 0101 0101 0101 0101 *

N OP BITS*
L2048 0101 0101 *

N Signature Words (8 Bytes) *
L2056 0101 0101 0101 0101 0101 0101 0101 0101 *
L2088 0101 0101 0101 0101 0101 0101 0101 0101 *

N RC Bits *
L2120 0101 0101 *

N Product Term Disable*
L2128 0101 0101 0101 0101 0101 0101 0101 0101 *
L2160 0101 0101 0101 0101 0101 0101 0101 0101 *

N MSO Bit *
L2192 0 *

N MS1 Bit *
L2193 1 *

CXXXX*
<ETX> 0000
```

4 Program/Verify Operation Tables

Table 3 General Operation Table

Modes	Program/Verify Pins							
	PVE	MODEA-B		PVP	SEC	ALE	TGA(3-0)	IAD(7-0)
	1	2	3	4	9	11	8-5	19-12
Normal Operation	X	X	X	X	X	X	X	X
Erase All	H1	0	0	H2	0	H2	0h	00h
Program All	H1	0	1	H2	0	0	0h	FFh
Program Byte	H1	1	1	H2	0	^1	Table 5 through Table 9	
Verify Byte	H1	1	0	H2	0	^1		
Set Security Bit	H1	1	1	H2	H2	^1	0h	00h

X = V_{IH} or V_{IL} (TTL Don't care)
1 = V_{IL} (TTL Low)
0 = V_{IH} (TTL High)
^ = High level Latched
H1 = V_{HH1}
H2 = V_{HH2} (The rise time for PVP during Program, Verify and Set Security Bit is different. Please see the flow chart individually detail.)

Table 4 Product Term and Configuration Bit to Fuse Number Conversion

Product Term #, Input Line # to Fuse Number Conversion									
Input Line # (0 - 31)	Product Term # (0 - 63)	Conversion Equation: Fuse State = (Product Term #) * 32 + (Input Line #)							
		IAD19	IAD18	IAD17	IAD16	IAD15	IAD14	IAD13	IAD12
Examples:									
For Term Group #1 containing ->		PT08	PT09	PT10	PT11	PT12	PT13	PT14	PT15
Input Line #4 maps to: "Fuse State"		F0260	F0292	F0324	F0356	F0388	F0420	F0452	F0484
For Term Group #5 containing ->		PT40	PT41	PT42	PT43	PT44	PT45	PT46	PT47
Input Line #0 maps to "Fuse State"		F1280	F1312	F1344	F1376	F1408	F1440	F1472	F1504

MacroCell Configuration Bits to Fuse Number Mapping									
MacroCell Field		Bit Position							
Name	Description	0	1	2	3	4	5	6	7
OP	Output Polarity	F2048	F2049	F2050	F2051	F2052	F2053	F2054	F2055
RC	Register Control	F2120	F2121	F2122	F2123	F2124	F2125	F2126	F2127

Global Field Codes		
MS0	Mode Select 0	F2192
MS1	Mode Select 1	F2193

Table 5 Input Line Addressing

Input Line #	Simple Mode		Complex Mode		Register Mode	
	Function	IAD(7:0)	Function	IAD(7:0)	Function	IAD(7:0)
0	PIN 2	05h	PIN 2	05h	PIN 2	05h
1	/PIN 2	07h	/PIN 2	07h	/PIN 2	07h
2	PIN 1	01h	PIN 1	01h	FB 19	If (OP0 or RC0) 21h else 23h
3	/PIN 1	03h	/PIN 1	03h	/FB 19	If (OP0 or RC0) 23h else 21h
4	PIN 3	09h	PIN 3	09h	PIN 3	09h
5	/PIN 3	0Bh	/PIN 3	0Bh	/PIN 3	0Bh
6	FB 19	21h	FB 18	1Dh	FB 18	If (OP1 or RC1) 1Dh else 1Fh
7	/FB 19	23h	/FB 18	1Fh	/FB 18	If (OP1 or RC1) 1Fh else 1Dh
8	PIN 4	0Dh	PIN 4	0Dh	PIN 4	0Dh
9	/PIN 4	0Fh	/PIN 4	0Fh	/PIN 4	0Fh
10	FB 18	1Dh	FB 17	19h	FB 17	If (OP2 or RC2) 19h else 1Bh
11	/FB 18	1Fh	/FB 17	1Bh	/FB 17	If (OP2 or RC2) 1Bh else 19h
12	PIN 5	11h	PIN 5	11h	PIN 5	11h
13	/PIN 5	13h	/PIN 5	13h	/PIN 5	13h
14	FB 17	19h	FB 16	15h	FB 16	If (OP3 or RC3) 15h else 17h
15	/FB 17	1Bh	/FB 16	17h	/FB 16	If (OP3 or RC3) 17h else 15h
16	PIN 6	12h	PIN 6	12h	PIN 6	12h
17	/PIN 6	14h	/PIN 6	14h	/PIN 6	14h
18	FB 14	1Ch	FB 15	18h	FB 15	If (OP4 or RC4) 18h else 16h
19	/FB 14	1Ah	/FB 15	16h	/FB 15	If (OP4 or RC4) 16h else 18h
20	PIN 7	0Eh	PIN 7	0Eh	PIN 7	0Eh
21	/PIN 7	10h	/PIN 7	10h	/PIN 7	10h
22	FB 13	20h	FB 14	1Ch	FB 14	If (OP5 or RC5) 1Ch else 1Ah
23	/FB 13	1Eh	/FB 14	1Ah	/FB 14	If (OP5 or RC5) 1Ah else 1Ch
24	PIN 8	0Ah	PIN 8	0Ah	PIN 8	0Ah
25	/PIN 8	0Ch	/PIN 8	0Ch	/PIN 8	0Ch
26	FB 12	24h	FB 13	20h	FB 13	If (OP6 or RC6) 20h else 1Eh
27	/FB 12	22h	/FB 13	1Eh	/FB 13	If (OP6 or RC6) 1Eh else 20h
28	PIN 9	06h	PIN 9	06h	PIN 9	06h
29	/PIN 9	08h	/PIN 9	08h	/PIN 9	08h
30	PIN 11	02h	FB 11	02h	FB 12	If (OP7 or RC7) 24h else 22h
31	/PIN 11	04h	/FB 11	04h	/FB 12	If (OP7 or RC7) 22h else 24h
CFG0	Config 0	15h	Config 0	21h	Config 0	01h
CFG1	Config 1	16h	Config 1	22h	Config 1	02h
CFG2	Config 2	17h	Config 2	23h	Config 2	03h
CFG3	Config 3	18h	Config 3	24h	Config 3	04h
GLB	Global	25h	Global 0	25h	Global 0	25h
Note: Different address mappings for Simple, Complex and Register Mode						

Table 6 Signature Words Addressing And Fuse State

Term Group #	IAD(7-0) ADDRESS #			IAD(7-0) PINS AND "Fuse State"		
	Simple Mode	Complex Mode	Register Mode	19-14	13	12
SW	01h	01h	05h	<000000>	F2056	F2057
SW	02h	02h	06h	<000000>	F2058	F2059
SW	03h	03h	07h	<000000>	F2060	F2061
SW	04h	04h	08h	<000000>	F2062	F2063
SW	05h	05h	09h	<000000>	F2064	F2065
SW	06h	06h	0Ah	<000000>	F2066	F2067
SW	07h	07h	0Bh	<000000>	F2068	F2069
SW	08h	08h	0Ch	<000000>	F2070	F2071
SW	09h	09h	0Dh	<000000>	F2072	F2073
SW	0Ah	0Ah	0Eh	<000000>	F2074	F2075
SW	0Bh	0Bh	0Fh	<000000>	F2076	F2077
SW	0Ch	0Ch	10h	<000000>	F2078	F2079
SW	0Dh	0Dh	11h	<000000>	F2080	F2081
SW	0Eh	0Eh	12h	<000000>	F2082	F2083
SW	0Fh	0Fh	13h	<000000>	F2084	F2085
SW	10h	10h	14h	<000000>	F2086	F2087
SW	11h	11h	15h	<000000>	F2088	F2089
SW	12h	12h	16h	<000000>	F2090	F2091
SW	13h	13h	17h	<000000>	F2092	F2093
SW	14h	14h	18h	<000000>	F2094	F2095
SW	19h	15h	19h	<000000>	F2096	F2097
SW	1Ah	16h	1Ah	<000000>	F2098	F2099
SW	1Bh	17h	1Bh	<000000>	F2100	F2101
SW	1Ch	18h	1Ch	<000000>	F2102	F2103
SW	1Dh	19h	1Dh	<000000>	F2104	F2105
SW	1Eh	1Ah	1Eh	<000000>	F2106	F2107
SW	1Fh	1Bh	1Fh	<000000>	F2108	F2109
SW	20h	1Ch	20h	<000000>	F2110	F2111
SW	21h	1Dh	21h	<000000>	F2112	F2113
SW	22h	1Eh	22h	<000000>	F2114	F2115
SW	23h	1Fh	23h	<000000>	F2116	F2117
SW	24h	20h	24h	<000000>	F2118	F2119

Note: Different address mappings for Simple, Complex and Register Mode

Table 7 Term Group Addressing

Term Group #	Simple Mode	Complex Mode	Register Mode (RCn=1 / RCn=0)	TGA(3-0)
0	Product Terms 00-07	Product Terms 01-07	Product Terms 01-07 / 00-07	8h
1	Product Terms 08-15	Product Terms 09-15	Product Terms 09-15 / 08-15	7h
2	Product Terms 16-23	Product Terms 17-23	Product Terms 17-23 / 16-23	6h
3	Product Terms 24-31	Product Terms 25-31	Product Terms 25-31 / 24-31	5h
4	Product Terms 32-39	Product Terms 33-39	Product Terms 33-39 / 32-39	4h
5	Product Terms 40-47	Product Terms 41-47	Product Terms 41-47 / 40-47	3h
6	Product Terms 48-55	Product Terms 49-55	Product Terms 49-55 / 48-55	2h
7	Product Terms 56-63	Product Terms 57-63	Product Terms 57-63 / 56-63	1h
OE		OE Product Terms 0, 8, 16, 24, 32, 40, 48, 56	OE Product Terms *1 0, 8, 16, 24, 32, 40, 48, 56	9h
SW	Signature Word			0Ah

Note 1: Register Mode: OE Product Term is based on each IO's RC. For example: if RCn='1', for all the IO's (Pin 19-12) then OE='PT00 PT08 PT16 PT24 PT32 PT40 PT48 PT56' if RC0, RC2, RC4, RC6 ='0' and RC1, RC3, RC5, RC7 = '1' then OE ='1 PT08 1 PT24 1 PT40 1 PT56'.

Table 8 Program Address And Fuse State Sequence

Term Group # *2	Input Line # *3	Function	IAD(7-0) PINS "Fuse State" *1 19	18	17	16	15	14	13	12
First section is common to All Modes:										
0-7, OE	CFG(0-3)	P-Term Disable	Table 9							
OE	GLB	Mode	1	MS0	1	MS1	1	1	1	1
SW	CFG(0-3)		1	1	1	1	1	1	0	0
SW	SW(0-31)	Signature Word	Table 6							
If Simple Mode then										
0-7	0-31	Product-Terms	LSB	-- (fuse state data *4) --						MSB
0-7	GLB	Output Polarity	1	1	1	1	1	1	/OPn *5	1
Else If Complex Mode then										
0-7	0-31	Product-Terms	LSB	-- (fuse state data) --					MSB	1
0-7	GLB	Output Polarity	1	1	1	1	0	1	/OPn	1
OE	0-31	OE Product-Terms	LSB	-- (fuse state data) --						MSB
Else If Register Mode then										
0-7	0-31	Product-Terms If (/RCn)	LSB	-- (fuse state data) --					MSB	1
		Product-Terms If (RCn)	LSB	-- (fuse state data) --						MSB
0-7	GLB	Output Polarity	RCn	1	RCn	1	/RCn	1	/OPn	1
OE	0-31	OE Product-Terms	LSB	-- (fuse state data) --						MSB
Note 1: Different programming sequence for Simple, Complex and Register Mode										
Note 2: See Table 7 Term Group Addressing										
Note 3: See Table 5 Input Line Addressing and Table 6 Signature Words Addressing And Fuse State										
Note 4: See Table 4 for Product Term#, Input Line # conversion to Fuse Number										
Note 5: For OPn and RCn, index n corresponds to the Term Group Number										

Table 9 Product Term Disable Fuse State (OPT)

Simple Mode									
Term Group #		**IAD(7-0) PIN AND "Fuse State" (OPT)**							
		19	**18**	**17**	**16**	**15**	**14**	**13**	**12**
0		F2128	F2129	F2130	F2131	F2132	F2133	F2134	F2135
1		F2136	F2137	F2138	F2139	F2140	F2141	F2142	F2143
2		F2144	F2145	F2146	F2147	F2148	F2149	F2150	F2151
3		F2152	F2153	F2154	F2155	F2156	F2157	F2158	F2159
4		F2160	F2161	F2162	F2163	F2164	F2165	F2166	F2167
5		F2168	F2169	F2170	F2171	F2172	F2173	F2174	F2175
6		F2176	F2177	F2178	F2179	F2180	F2181	F2182	F2183
7		F2184	F2185	F2186	F2187	F2188	F2189	F2190	F2191
OE		/RC0	/RC1	/RC2	/RC3	/RC4	/RC5	/RC6	/RC7
Complex Mode									
Term Group #		**IAD(7-0) PIN AND "Fuse State" (OPT)**							
		19	**18**	**17**	**16**	**15**	**14**	**13**	**12**
0		F2129	F2130	F2131	F2132	F2133	F2134	F2135	0
1		F2137	F2138	F2139	F2140	F2141	F2142	F2143	0
2		F2145	F2146	F2147	F2148	F2149	F2150	F2151	0
3		F2153	F2154	F2155	F2156	F2157	F2158	F2159	0
4		F2161	F2162	F2163	F2164	F2165	F2166	F2167	0
5		F2169	F2170	F2171	F2172	F2173	F2174	F2175	0
6		F2177	F2178	F2179	F2180	F2181	F2182	F2183	0
7		F2185	F2186	F2187	F2188	F2189	F2190	F2191	0
OE		F2128	F2136	F2144	F2152	F2160	F2168	F2176	F2184
Register Mode									
Term Group #		**IAD(7-0) PIN AND "Fuse State" (OPT)**							
		19	**18**	**17**	**16**	**15**	**14**	**13**	**12**
0	If (/RC0)	F2128	F2129	F2130	F2131	F2132	F2133	F2134	F2135
	If (RC0)	F2129	F2130	F2131	F2132	F2133	F2134	F2135	0
1	If (/RC1)	F2136	F2137	F2138	F2139	F2140	F2141	F2142	F2143
	If (RC1)	F2137	F2138	F2139	F2140	F2141	F2142	F2143	0
2	If (/RC2)	F2144	F2145	F2146	F2147	F2148	F2149	F2150	F2151
	If (RC2)	F2145	F2146	F2147	F2148	F2149	F2150	F2151	0
3	If (/RC3)	F2152	F2153	F2154	F2155	F2156	F2157	F2158	F2159
	If (RC3)	F2153	F2154	F2155	F2156	F2157	F2158	F2159	0
4	If (/RC4)	F2160	F2161	F2162	F2163	F2164	F2165	F2166	F2167
	If (RC4)	F2161	F2162	F2163	F2164	F2165	F2166	F2167	0
5	If (/RC5)	F2168	F2169	F2170	F2171	F2172	F2173	F2174	F2175
	If (RC5)	F2169	F2170	F2171	F2172	F2173	F2174	F2175	0
6	If (/RC6)	F2176	F2177	F2178	F2179	F2180	F2181	F2182	F2183
	If (RC6)	F2177	F2178	F2179	F2180	F2181	F2182	F2183	0
7	If (/RC7)	F2184	F2185	F2186	F2187	F2188	F2189	F2190	F2191
	If (RC7)	F2185	F2186	F2187	F2188	F2189	F2190	F2191	0
OE		F2128 ∨ /RC0	F2136 ∨ /RC1	F2144 ∨ /RC2	F2152 ∨ /RC3	F2160 ∨ /RC4	F2168 ∨ /RC5	F2176 ∨ /RC6	F2184 ∨ /RC7
Note: Different Product Term Disable Fuse Assignments for Simple, Complex and Register Mode									

∨ - Logic OR operand

/ - Logic NOT operand

5 Program/Verify Flow Tables (Simple, Complex And Register Modes)

Table 10 Fast Program Byte Mode Flow

Step	Pin #	Pin Name	Action
0	12-19	IAD0-7	Set to high impedance (Hi-Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IH}, MODE B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA0-3	Set next term group address in sequence (from Table 8)
5	12-19	IAD0-7	Set next input line address in sequence (from Table 8)
6	11	ALE/ERA	Set to V_{IH} (Latch Address)
7	12-19	IAD0-7	Set Data = /<"Fuse State">. **!!INVERT DATA for Write to device !!** If Data = 00h then jump to step #11 else go to step #8 (See Table 8 for “Fuse State” values)
8	4	PVP	Raise to V_{HH3}, then ramp to V_{HH2} at a 50u sec/V (See TRP and T_{RP2})
9	11	ALE/ERA	Set to VIL
10	4	PVP	Hold for T_{WP}, then set to V_{IL}
11	--	--	Repeat step 5-10 until all specified input lines have been programmed
12	--	--	Repeat step 4-11 until all specified term groups have been programmed
13	12-19	IAD0-7	Set to high impedance (Hi-Z)
14	1	PVE	Set to V_{IL}, return to normal operation

/ – Logic NOT operand

Table 11 Verify Byte Mode Flow

Step	Pin #	Pin Name	Action
0	12-19	IAD0-7	Set to high impedance (Hi-Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IH}, MODE B=V_{IL}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA0 -3	Set next term group address in sequence (from Table 8)
5	12-19	IAD0-7	Set next input line address in sequence (from Table 8)
6	9	SEC/OD	Set to V_{IH}
7	11	ALE/ERA	Set to V_{IH} (Latch address)
8	12-19	IAD0-7	Set to high impedance (Hi-Z)
9	4	PVP	Set to V_{HH2}
10	11	ALE/ERA	Set to V_{IL}
11	9	SEC/OD	Set to V_{IL}
12	12-19	IAD0-7	Read data "Fuse State" byte, (See Table 8 for “Fuse State” values) Note: Data reads TRUE from device.
13	4	PVP	Set to V_{IL}
14	--	--	Repeat step 5-13 until all 32 input lines have been read.
15	--	--	Repeat step 4-14 until all specified term groups have been read.
16	12-19	IADO -7	Set to high impedance (Hi-Z)
17	1	PVE	Set to V_{IL}, return to normal operation

Table 12 Erase-All Mode Flow

Step	Pin #	Pin Name	Action
0	12-19	IAD0 -7	Set to high impedance (Hi-Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A =V_{IL}, MODE B =V_{IL}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA0 -3	Set term group address to 0hex
5	12-19	IAD0 -7	Set input line address to 00hex
6 *[1]	11	ALE/ERA	Set to V_{HH2} (Enable Erase)
7	4	PVP	Raise to V_{HH3}, then ramp to V_{HH2} at a 50u sec/V (SEE T_{RP} and T_{WP}), set to V_{IL}
8	11	ALE/ERA	Set to V_{IL}
9	12-19	IAD0 -7	Set to high impedance (Hi-Z)
10	1	PVE	Set to V_{IL}, return to normal operation

Note 1: Pin 11 (ALE/ERA) may follow pin 4 (PVP) as an alternative to steps 6 and 8

Table 13 Program-All Mode Flow

Step	Pin #	Pin Name	Action
0	12-19	IADO -7	Set to high impedance (Hi-Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A=V_{IL}, MODE B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGAO-3	Set term group address to 0hex
5	12-19	IAD0-7	Set input line address to FFhex
6	4	PVP	Raise to V_{HH3}, then ramp to V_{HH2} at a 50u sec/V (SEE T_{RP} and T_{WP}) set to V_{IL}
7	12-19	IAD0-7	Set to high impedance (Hi-Z)
8	1	PVE	Set to V_{IL}, return to normal operation

Table 14 Set Security Bit Mode Flow

Step	Pin #	Pin Name	Action
0	12-19	IAD0 -7	Set to high impedance (Hi-Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IH}, MODE B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA0-3	Set term group address to 0h
5	12-19	IAD0-7	Set input line address to 00h
6	11	ALE/ERA	Set to V_{IH} (Latch address)
7 *[1]	9	SEC/OD	Set to V_{HH2} (Enable Security Mode)
8	4	PVP	Raise to V_{HH3}, then ramp to V_{HH2} at a 50u sec/V (See TRP and TWP), set to V_{IL}
9 *[1]	9	SEC/OD	Set to V_{IL}
10	12-19	IAD0-7	Set to high impedance (Hi-Z)
11	1	PVE	Set to V_{IL}, return to normal operation

Note 1: Pin 9 (SEC/OD may follow Pin 4 (PVP) as an alternative to steps 7 and 9.

6 PEEL™ 16CV8 Program/Verify (DC and AC) Parameters and Waveforms

Absolute Maximum Ratings

Voltages relative to ground (pin 1)…… +160V to -0.5V

(all other pins)…….. +6.0V to -0.5V

Table 15 DC Electrical Characteristics For Program/Verify Operation

Symbol	Parameter	Condition	Min.	Max	Unit
V_{CC}	Supply Voltage	-----	4.75	5.25	V
V_{HH1}	Program/Verify Volt. 1	-----	11.5	13	V
V_{HH2}	Program/Verify Volt. 2	-----	14.5	15	V
V_{HH3}	Program/Verify Volt.3	-----		10	V
I_{CC}	Supply Current	Program/Verify		100	mA
V_{IL}	Input Voltage Low	-----		0.8	V
V_{IH}	Input Voltage High	-----	2	V_{CC}+0.3	V
V_{OL}	Output Voltage Low	I_{OL} =+8.0Ma		0.4	V
V_{OH}	Output Voltage High	I_{OH} = -4 mA	2.4		V
I_{LI}	Input Leakage Current	GND<V_{IN}<V_{CC}MAX		10	µA
I_{LO}	Output Leakage Current	GND<V_{IN}<V_{CC}MAX		10	µA

Table 16 AC Electrical Characteristics For Program/Verify Operation

Symbol	Parameter	Diagram *[1]	Min *[2]	Max	Unit
t_{AZ1}, t_{AZ2}	AD0-7 HI-Z set-up to PVE	P, V, E, S	1		µS
t_{PS}	PVE set- up to VPP	P, V, E, S	4		µS
t_{MS}	MODE set-up to VPP	P, V, E, S	3		µS
t_{AL}	IAD Address set-up to ALE	P, V, E, S	1		µS
t_{LA}	IAD Address hold after ALE	P, V	1		µS
t_{DS}	IAD Data set-up to PVP	P	1		µS
t_{AZ3}	IAD Hi-Z before PVP	V	1		µS
t_{LS}	ALE set-up to PVP	E, S	1		µS
t_{AS}	TGA Address set-up to PVP	P, E	1		µS
t_{PL}	ALE hold after PVP	P, V	1		µS
t_{DE}	IAD Data Enable after PVP	V	0		µS
t_{LP}	ALE low set-up to PVP	P, V	1		µS
t_{SS}	SEC set-up to PVP	S	1		µS
t_{RP}	PVP rise time	P, E, S	50		µS/V
t_{WP}	PVP Program/Erase pulse width	P, E	10		µS
t_{SP}	PVP Security pulse width	S	300		µS
t_{VP}	PVP Verify pulse width	V	10		µS
t_{FP}	PVP fall time	P, V, E, S	1		µS
t_{DV}	IAD Data valid after PVP	V	1		µS
t_{DZ}	IAD Data HI-Z after PVP	V	1		µS
t_{DH}	IAD Data hold after PVP	P	1		µS
t_{AH}	IAD Address hold after PVP	P, V	1		µS
t_{HE}	ERA, SEC, IAD, TGA, Mode after PVP	E, S	1		µS
t_{MH}	MODE hold after PVP	P, V	1		µS
t_{PH}	PVE hold after PVP	P, V, E, S	1		µS
t_{SOD}	OD setup to output disable	V	2		µS
t_{HOD}	OD hold for output disable	V	1		µS

Note 1: Identifies the associated waveform timing diagram(s) to timing parameter:

P= Program Byte
V= Verify Byte
E= Erase All

Note 2: All timings are measured at 10% and 90% rise and fall points.

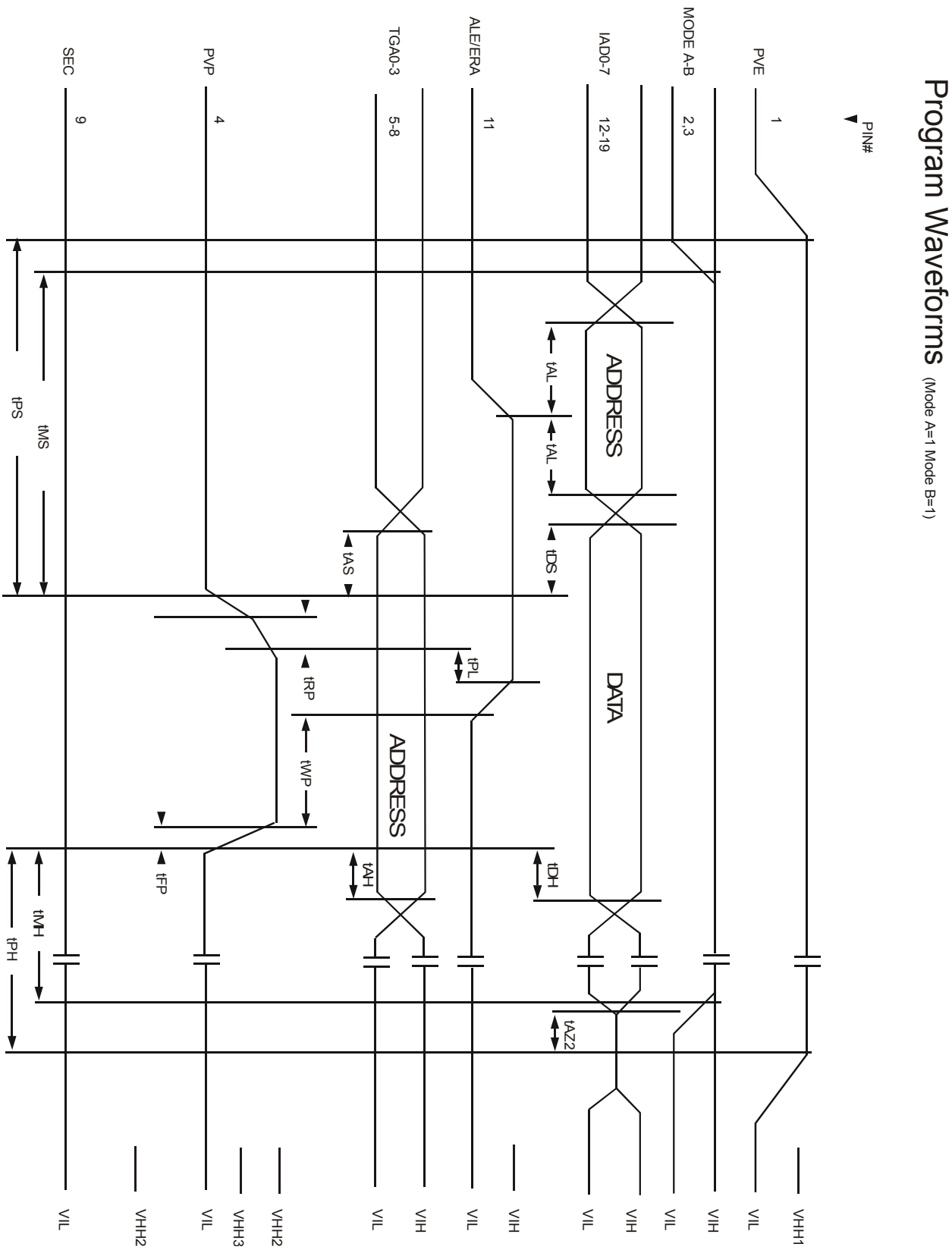

Figure 8 Program Waveforms (Mode A = 1, Mode B = 1)

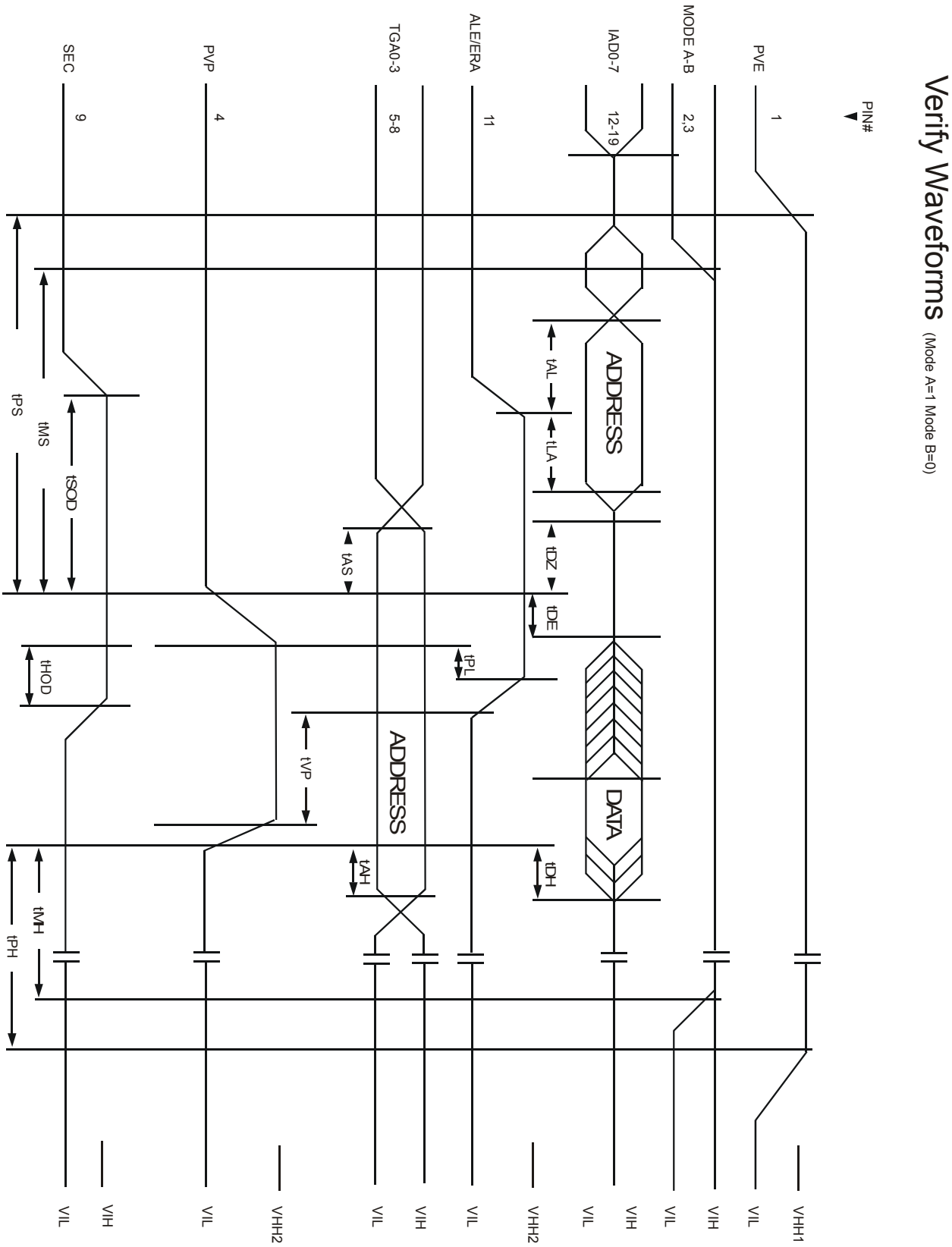

Figure 9 Verify Waveforms (Mode A = 1, Mode B = 0)

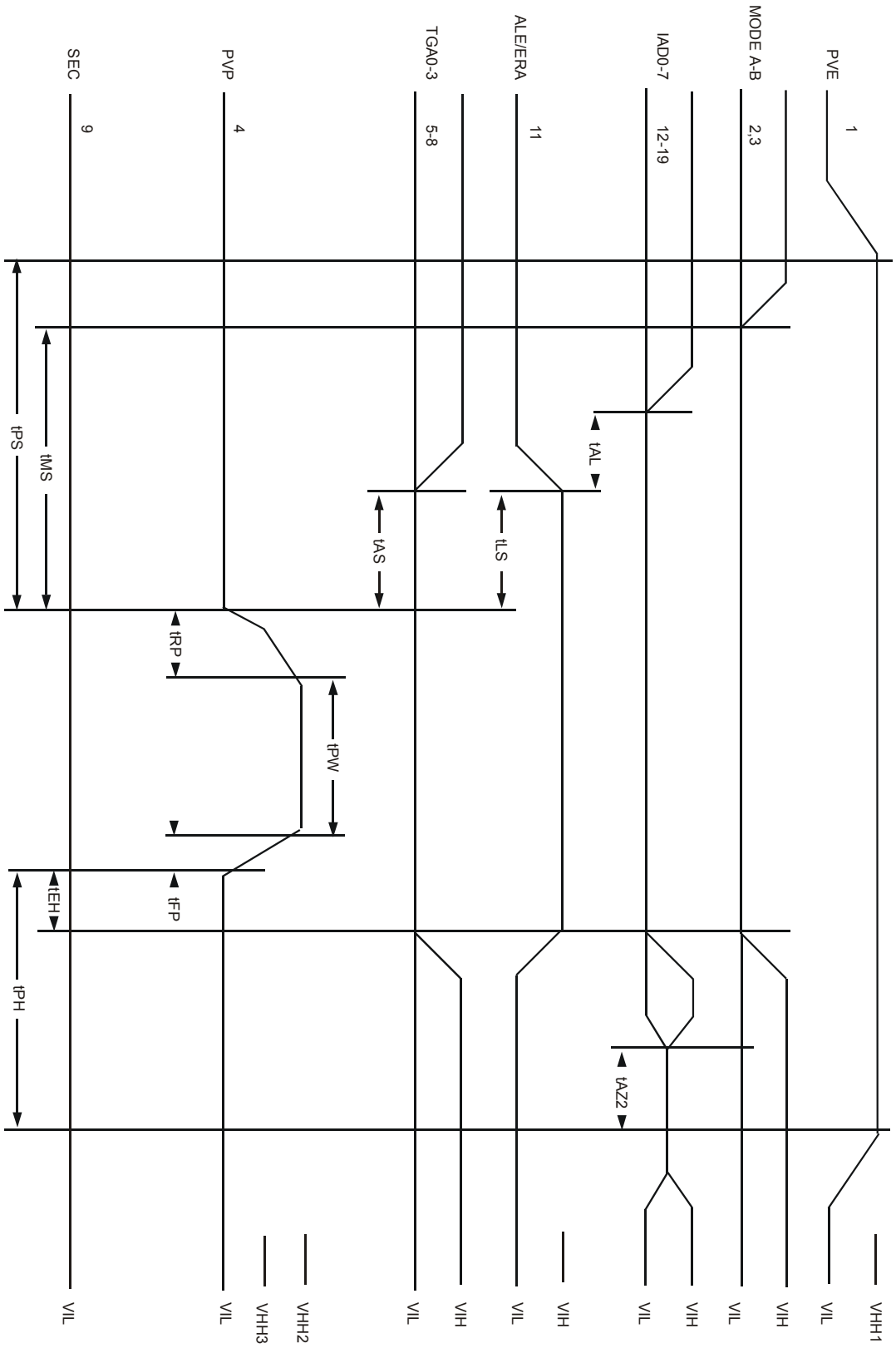

Figure 10 Erase All Waveforms (Mode A = 0, Mode B = 0)

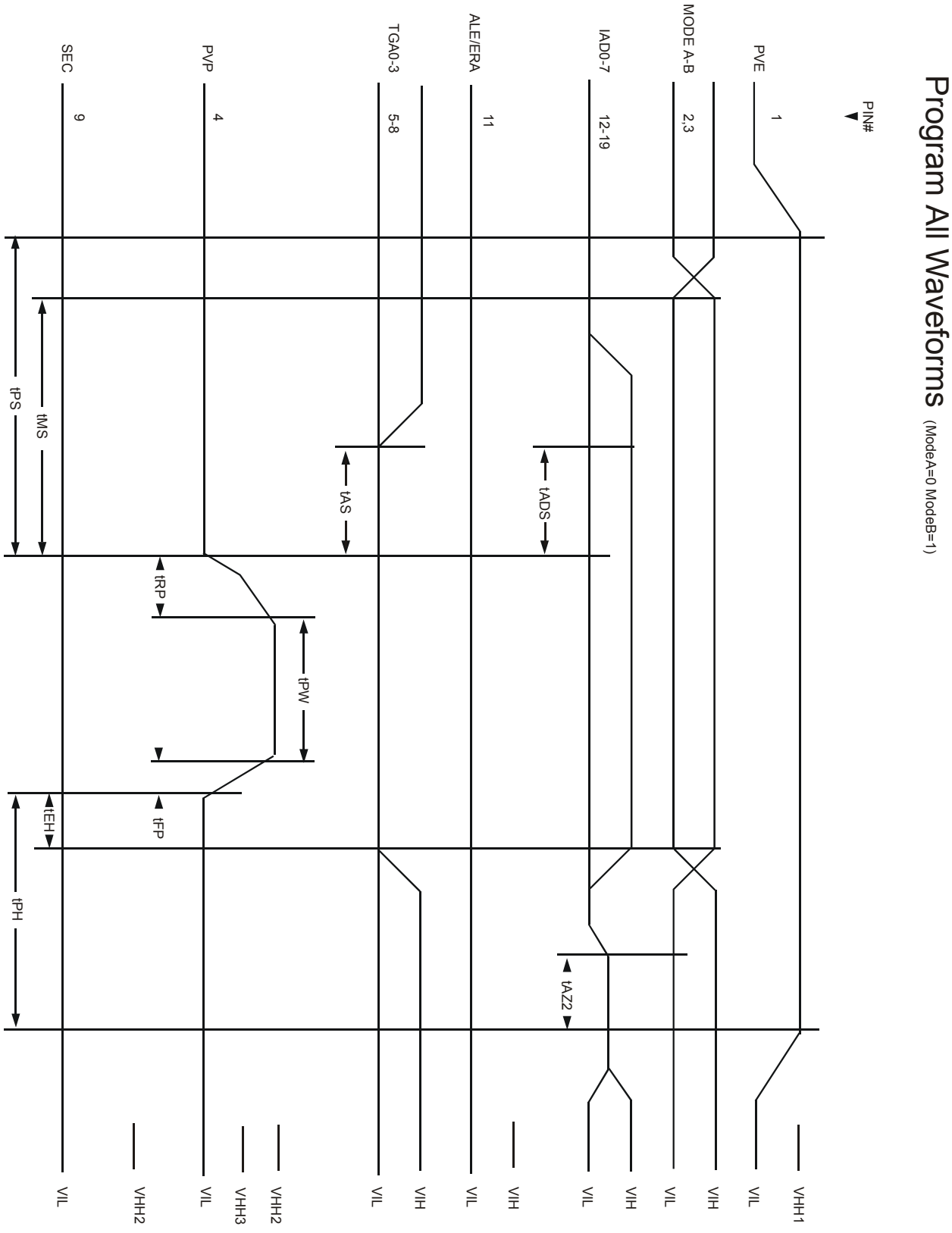

Figure 11 Program All Waveforms (Mode A = 0, Mode B = 1)

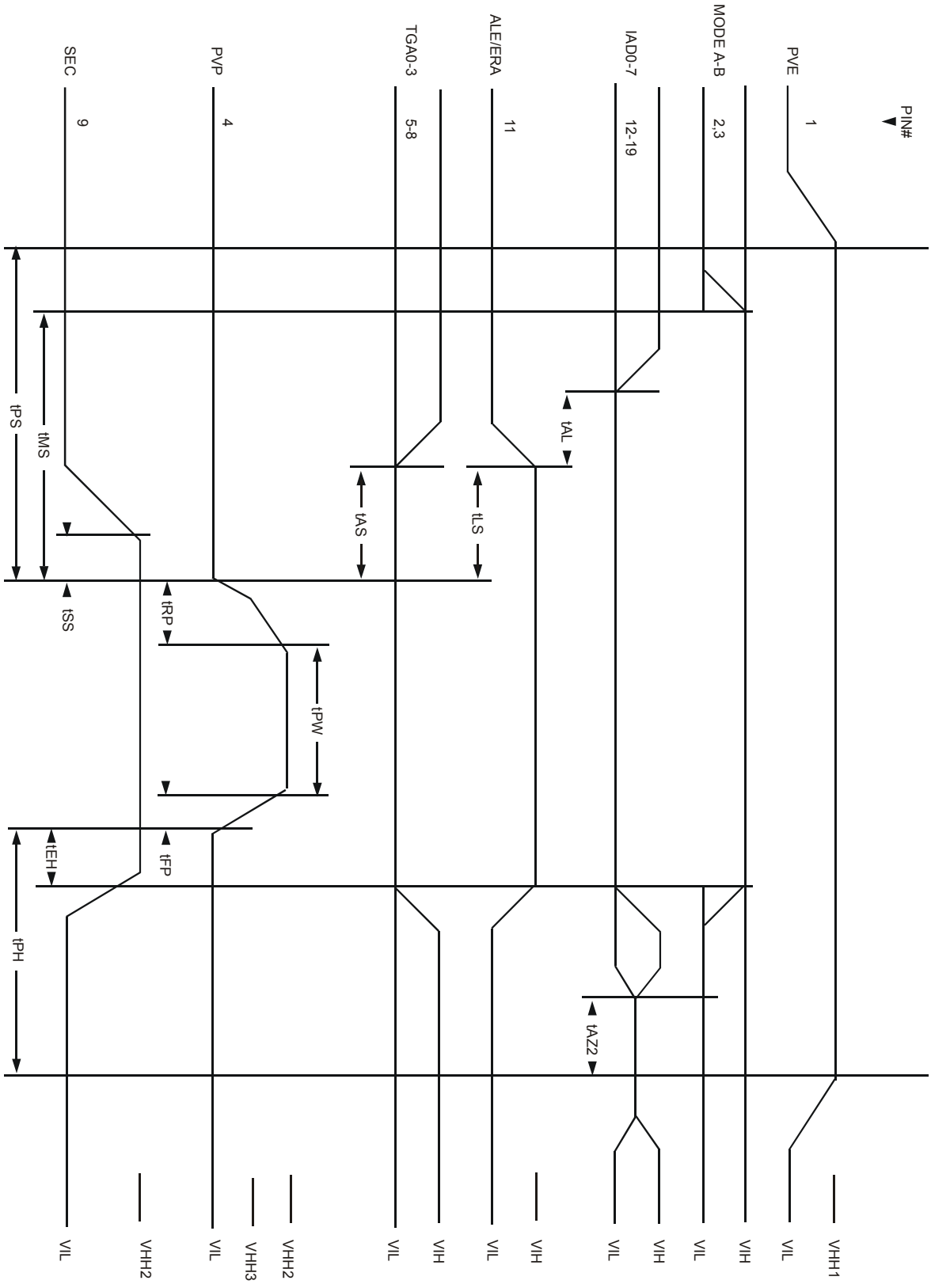

Figure 12 Security Bit Waveforms (Mode A = 1, Mode B = 1)