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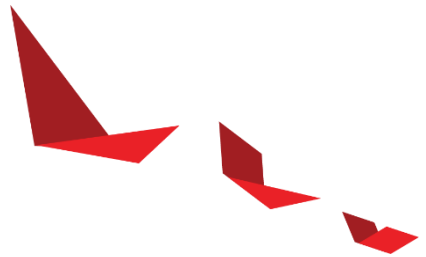
Artix® UltraScale+™ FPGA Webinar

Serial Throughput Meets Signal Compute Density in a Secure Cost-Optimized FPGA

Agenda



- Artix® UltraScale+™ FPGA Overview
- AU25P Development Platform
- Opal Kelly FrontPanel SDK
- Opal Kelly SYZYGY Peripheral Ecosystem

The New Artix® UltraScale+™ FPGA Family

Serial I/O Performance

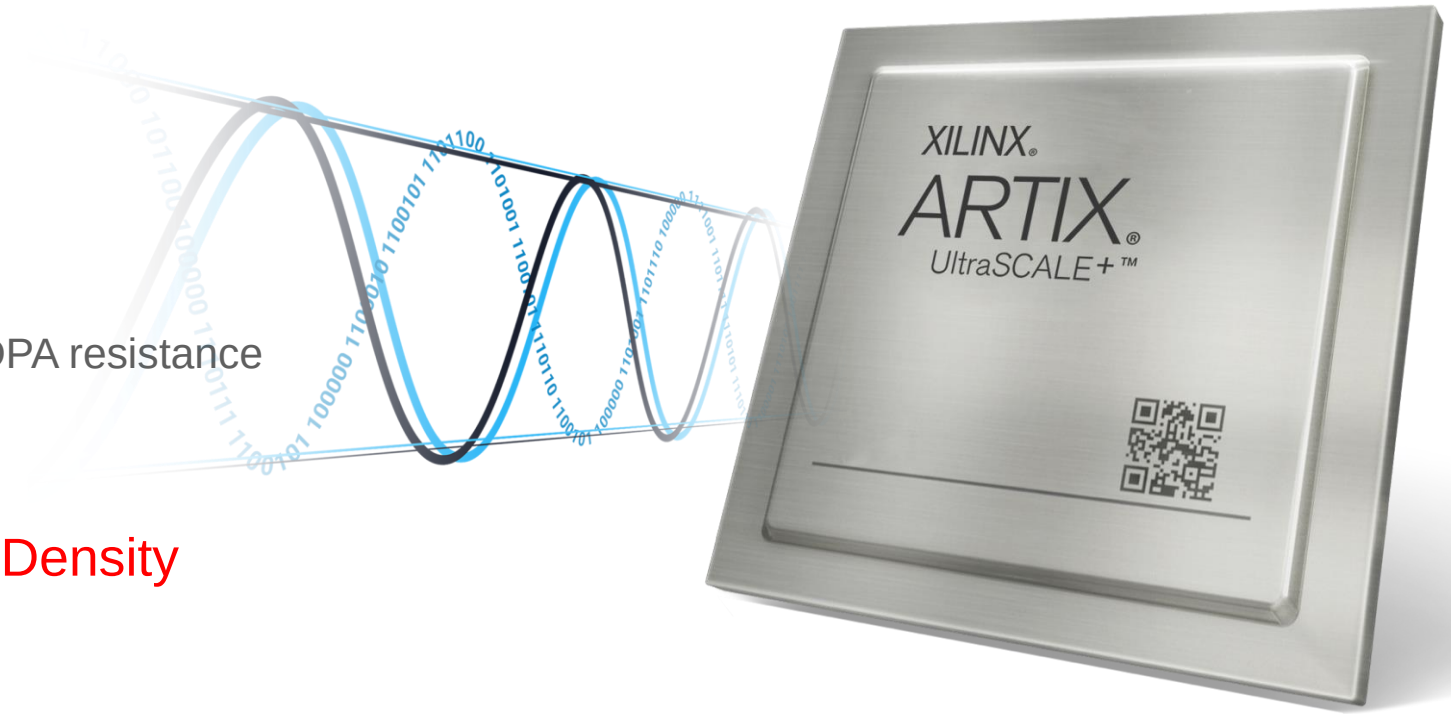
16Gb/s transceivers for advanced protocols in a cost-optimized family

Multi-Level Security

Cryptography, authentication, and DPA resistance for cybersecurity and IP protection

Signal Processing Compute Density

Best-in-class DSP bandwidth in small form-factor packaging



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Artix® UltraScale+™ Architecture Overview

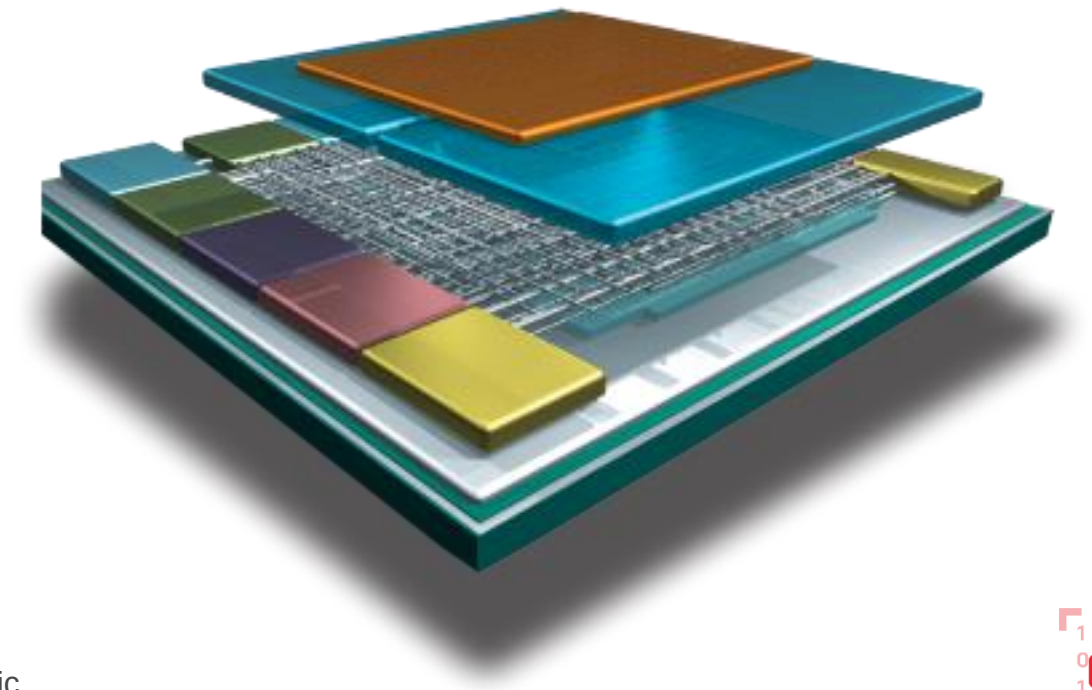
FinFET Perf/Watt
- Optimized Process
- Voltage Scaling

Transceivers
- 12G, 16G
- Fractional PLL

PCI Express®
- Gen3 x8
- Gen4 x2

Flexible I/O
- Power-Optimized I/O
- MIPI D-PHY Support

SmartConnect
- Addressing IP & Fabric Interconnect Bottlenecks



DSP
- Floating/Fixed Pt Enhanced
- 2.5X Bandwidth (vs. 28nm)

External Memory
- DDR4 support
- Up to 2,666 Mb/s

Block RAM
- Hardened Cascading
- Power-Optimized Silicon

Security & Reliability
- Decrypt/Auth/Anti-Tamper
- Improved SEU Performance

InFO Packaging
- Improved Signal Integrity, PCB Area, and Thermal Distribution

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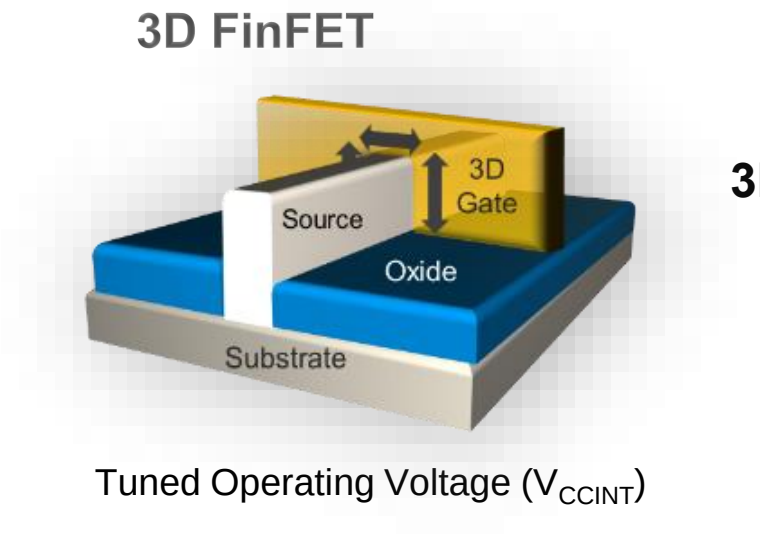
UltraScale+™ Performance/Watt Advantage



Tuned Operating Voltage (V_{CCINT})

3D Gate "wraps" around channel for more surface area, achieving

- ✓ Faster transistor on/off switching speeds for greater performance
- ✓ Lower leakage and operating voltage for lower power

	7 Series (28nm) V_{NOM}	UltraScale+ (16nm) V_{NOM}	UltraScale+ (16nm) V_{LOW}
Operating Voltage	1V	0.85V	0.72V
Fabric Performance	1X	1.6X	1.2X
Total Power	1X	0.8X	0.5X
Performance/Watt	1X	**2X**	**2.4X**

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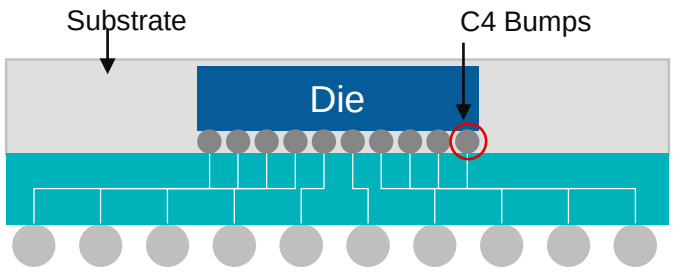
Ultra-Compact InFO (Integrated Fan-Out) Packaging

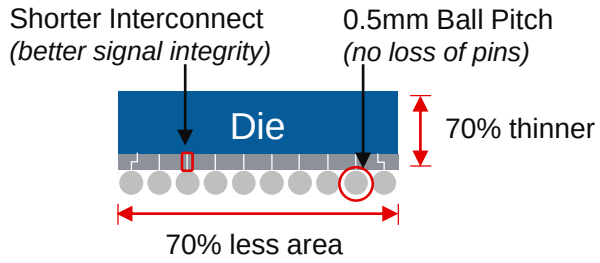
- Smaller and thinner package (no substrate or C4 bumps)
- “Near die size” ball pitch (0.5mm) for no loss of pins
- 70% less area for better thermal & power distribution
- Shorter interconnects for lower flight times and better signal integrity
- PCB and thermal guidelines available (EA)

	AU10P	AU15P
System Logic Cells (K)	96	170
Total Block RAM (Mb)	3.5	5.1
DSP Slices	400	576
Transceivers	12.5Gb/s (12)	12.5Gb/s (12)
Maximum I/O	144	144
InFO Package Size (mm)	9.5 x 11.5	9.5 x 11.5

Flip-Chip



InFO



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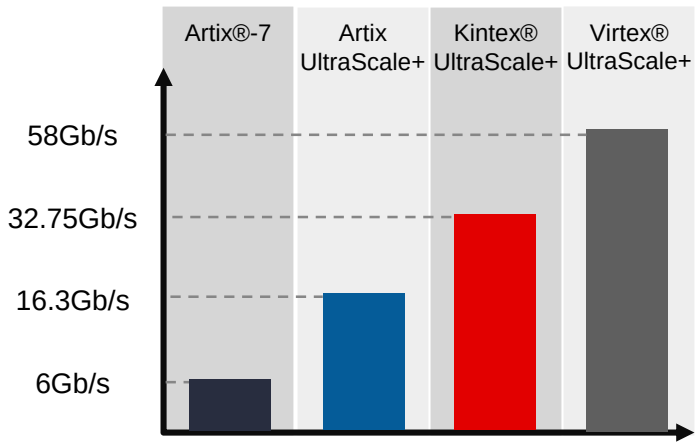
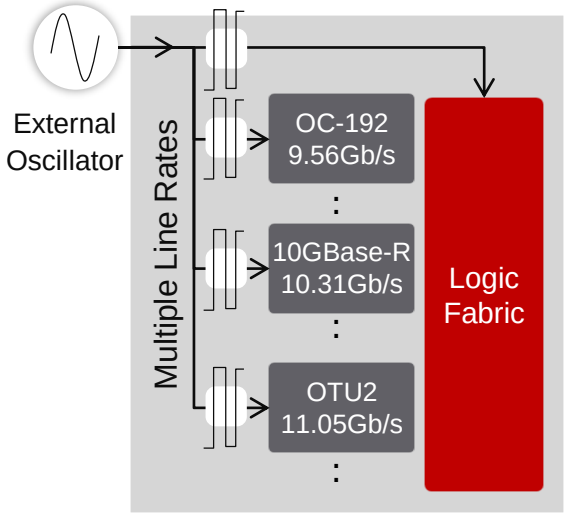
UltraScale+™ Enhanced Transceivers

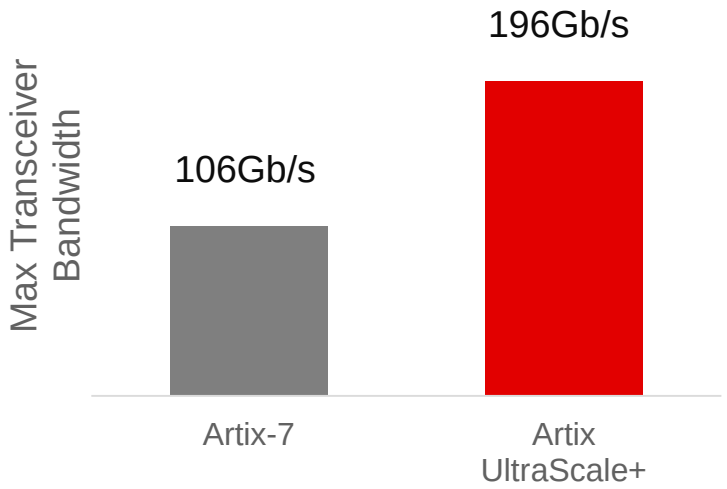
Feature	Benefit
Power Optimized	• GTH: ~10% power savings for backplane applications (DFE mode)
Fractional PLL in GTH Transceivers	• Single external oscillator generates GT & logic fabric clocks for multiple non-integer line rates • Reduced BOM cost • Matches fPLL functionality of GTY transceivers in UltraScale™ (20nm) FPGAs
Massive Total Effective Bandwidth	Up to 12 GTH @ 16Gb/s for more than 196Gb/s total bandwidth (almost 2x A7 (105.6Gb/s))
High GT bandwidth density	100Gb/s of aggregate GT bandwidth in smallest A360 110mm^2 package
Output Clocks	Ability to output from GTs into PL and onto the board
Hardened Burst CDR (BCDR)	Improves CDR lock time for greater link efficiency for NG-PON2 and 10G-EPON aggregation nodes

Transceiver Scalability



Fractional PLLs





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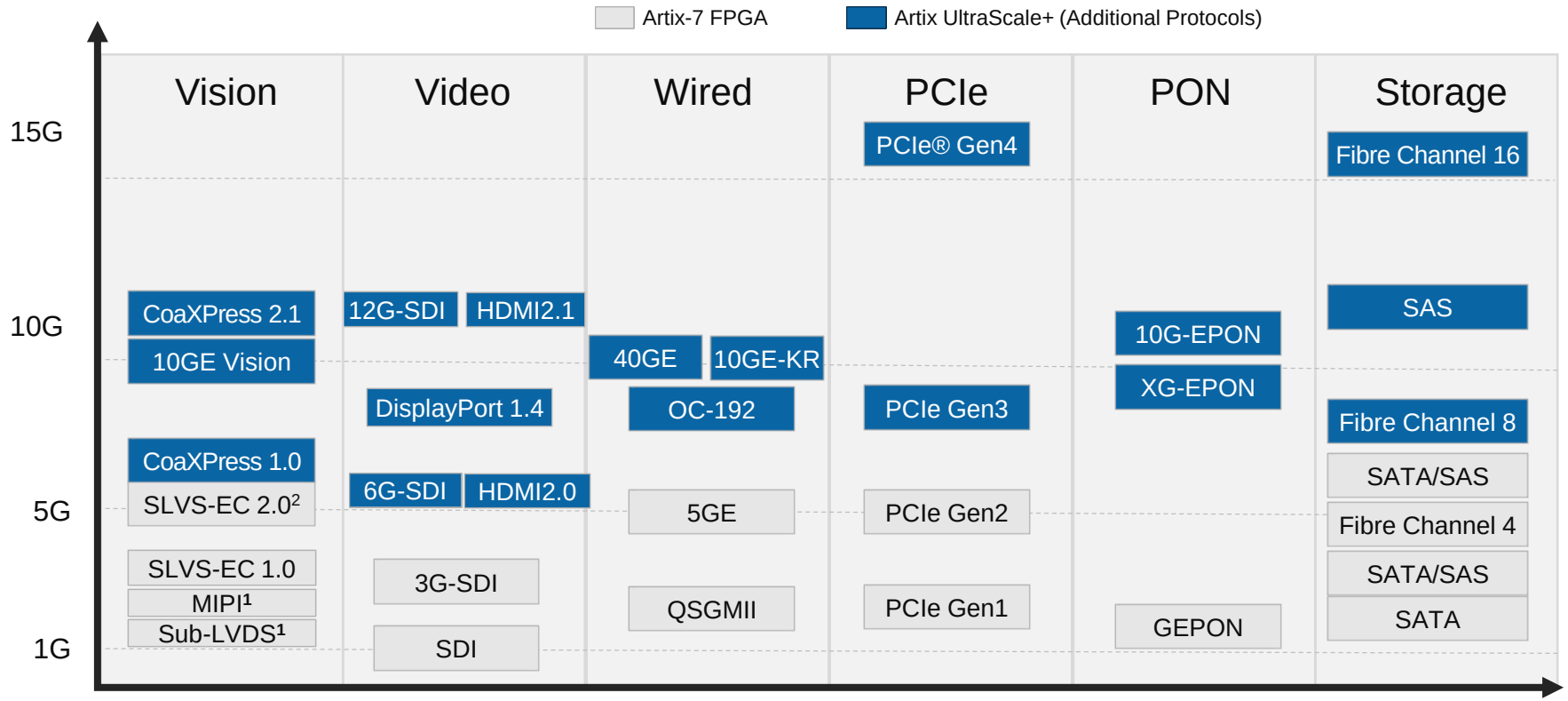
Target Artix UltraScale+ FPGA Applications and Protocols

- Up to 192 gigabits of aggregate bandwidth, including the smallest device!
- Supports emerging protocols in vision, video, networking, and storage



1: Artix® UltraScale+™ delivers 2500Mb/s LVDS/MIPI performance vs. Artix-7 at 1500MB/s
2: Artix UltraScale+ supports up to 12 lanes of SLVS-EC 2.0 in 19mm package

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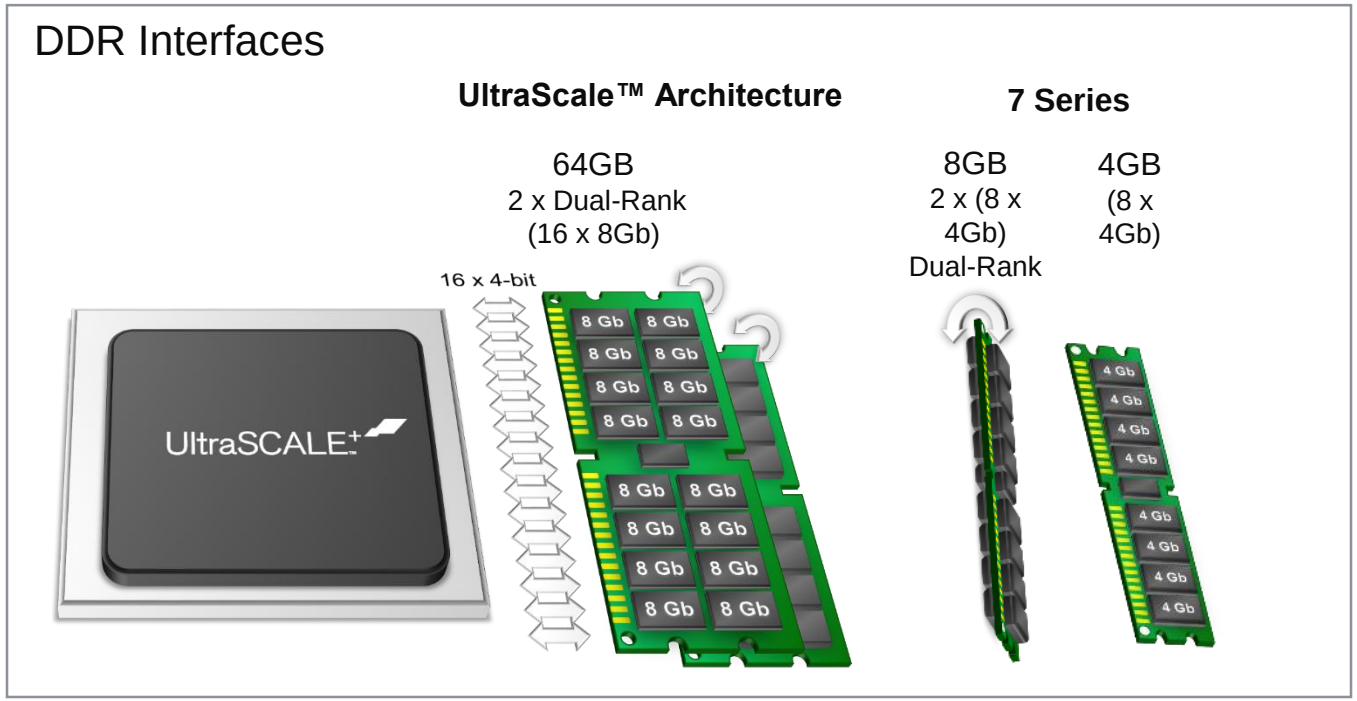
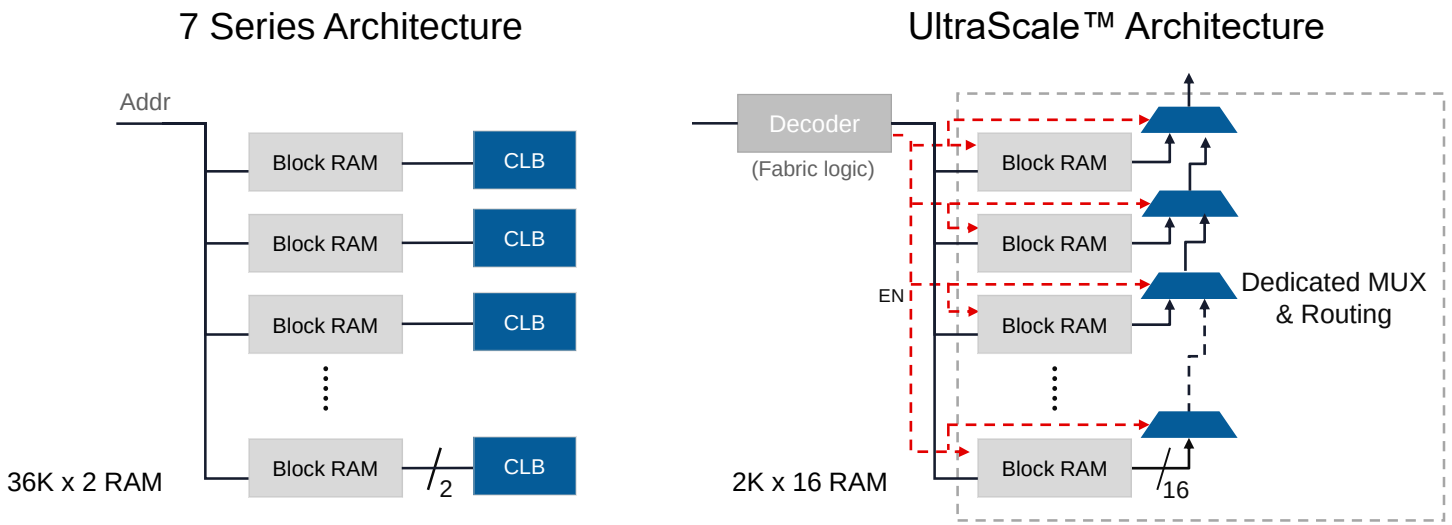
Memory Interface Enhancements

Feature	Benefits & Details
Building on Robustness at 28nm	• Production-proven at 16nm, delivering operating margin across varying PVT • New embedded calibration routine for greater intelligence and clock-centering at the eye
Supports up to DDR4-2666	Cost-effectively supports next-generation DDR4 memory line rates
DDR4-2133 at Low Operating Voltage (V_{LOW})	Voltage scaling enables high-performance DDR4 in low power operating mode
High-Density DIMM Support	• Quad-rank DIMM supported at 1600Mb/s with independent calibration points • Support for DIMMs based on 4-bit-wide DRAM components

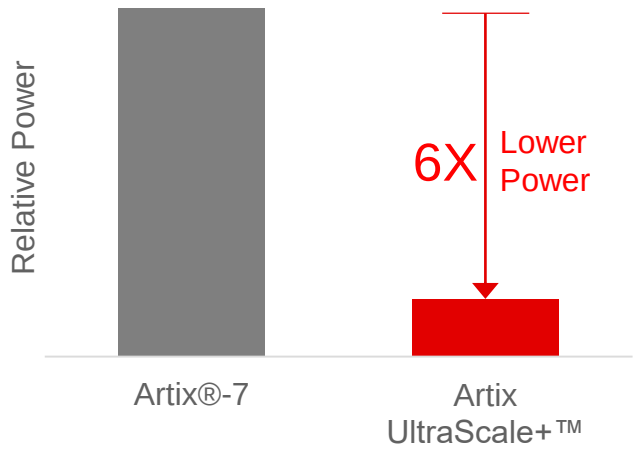


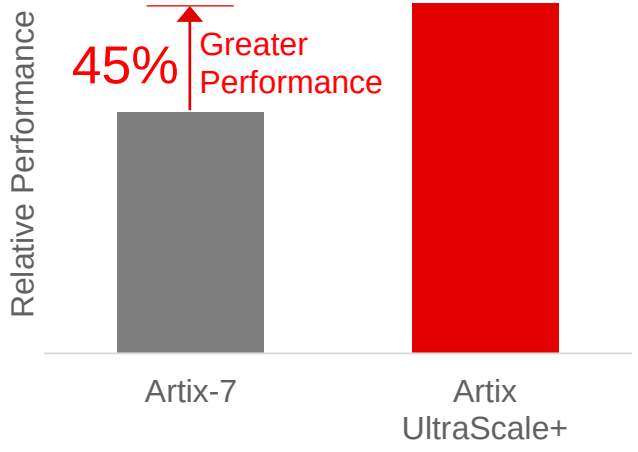
Protocol Support
DDR4-2666Mb/s
DDR3-2133Mb/s
DDR3L-1866Mb/s
LPDDR3-1600Mb/s
RLDRAM3-1200MHz
QDR IV-1066MHz

Enhanced Block RAM Power AND Performance



Built-in high-speed **Memory Cascading** eliminates CLB usage, reducing routing congestion and results in an average **60% power reduction**





Enhanced FIFO further lowers power and improves performance over Soft implementations

Based on Simple Dual Port Mode

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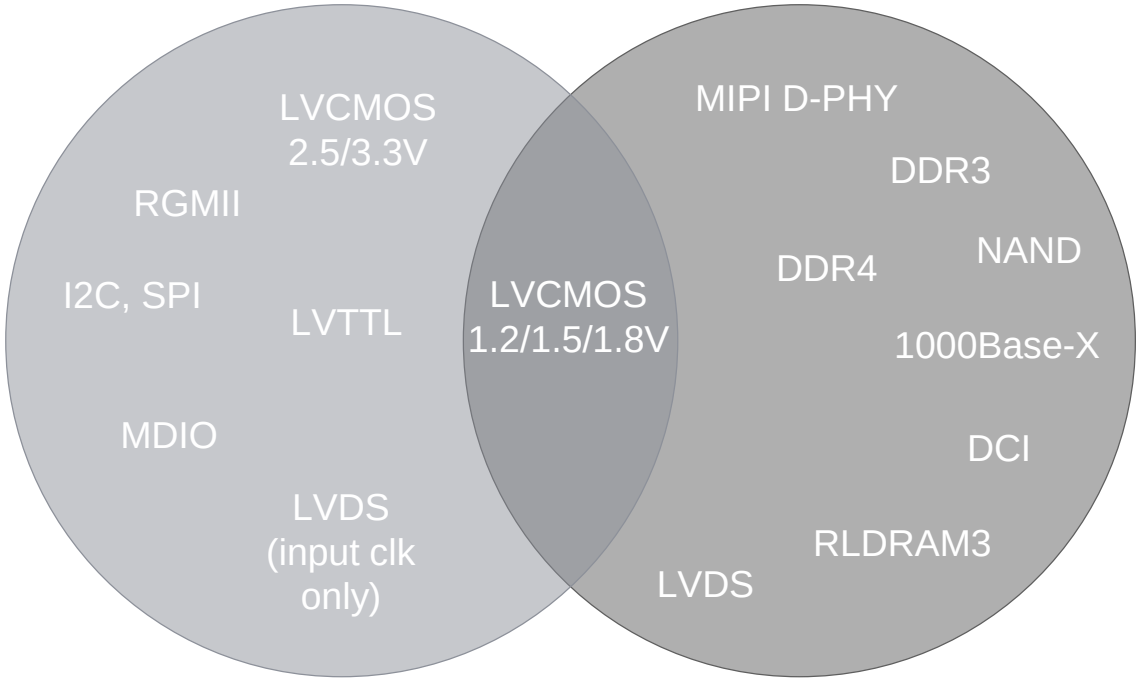
I/Os Optimized for Target Functions

Artix™ UltraScale+™ Adds HP I/O Support

- Power & area-efficient high-density (HD) & high-performance (HP) I/Os
  - Improved serialization & parallelization, bit-slicing, and input/output delay capability vs. Artix-7 FPGAs

HD I/O
Supports 3.3 & 2.5V legacy protocols, 1.2V – 1.8V single-ended support

HP I/O
Optimized for higher performance interfaces



Protocol	Artix-7 FPGA	Artix UltraScale+ FPGA
DDR	DDR3-1066 (-3)	DDR4-2666 (-2)
LVDS	1250Mb/s (-2)	1600Mb/s (-1)
MIPI	800Mb/s (requires external resistor network)	2500Mb/s (-1)

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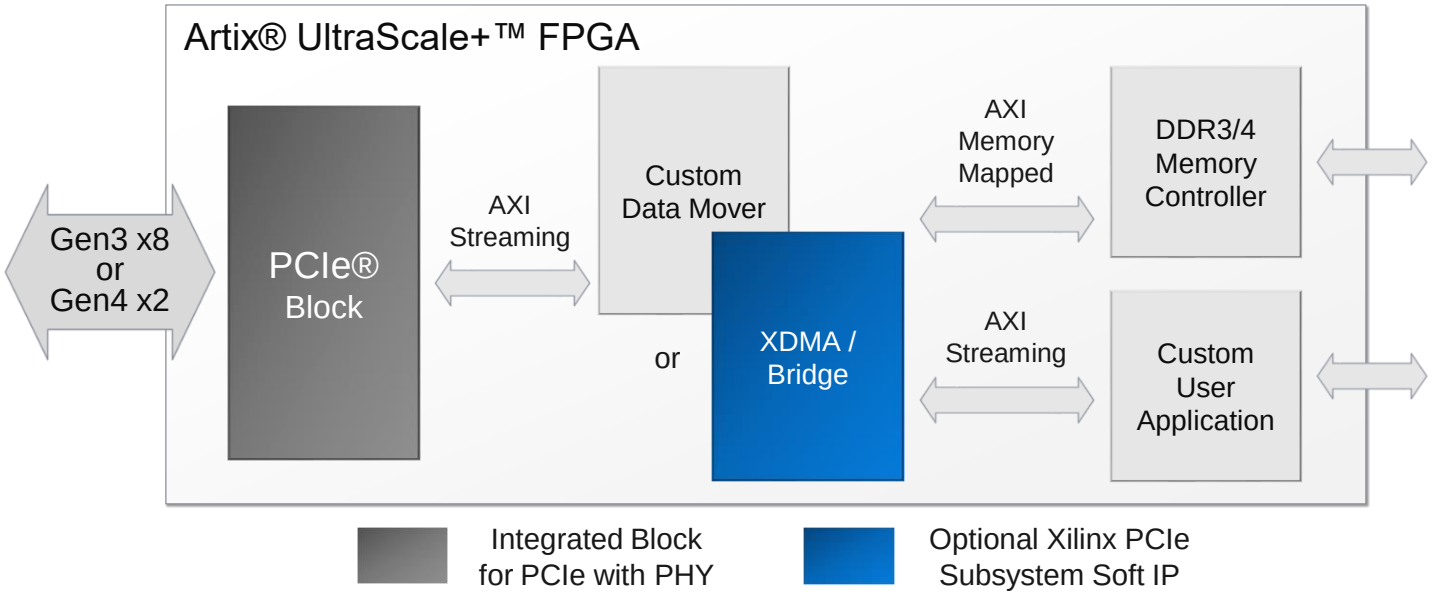
Integrated PCIe Gen3x8 and Gen4x2 Block

Features	Benefits
Gen3 x8 (8Gb/s per lane)	Performance for today's high-end systems, e.g., 100G data center
Gen4 x2 (16Gb/s per lane)	Highly interoperable with next-generation system topologies
Available Hardened SR-IOV (4 Physical, 252 Virtual Functions)	Expanded virtualization for demanding applications
Increased Number of Tags	• 128 managed tags and 256 user managed tags • Enables more outstanding RD requests for greater system performance
New DMA IP	Complete end-to-end solution



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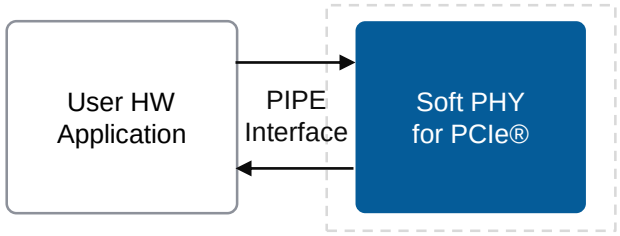
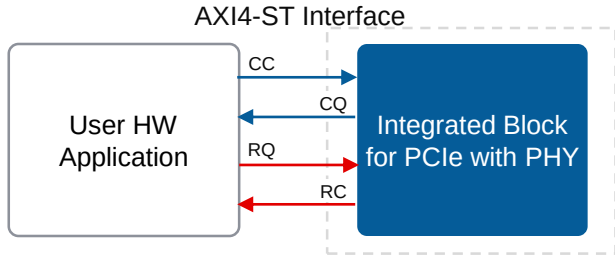
Multiple PCIe Configuration Options

Soft PHY for PCIe



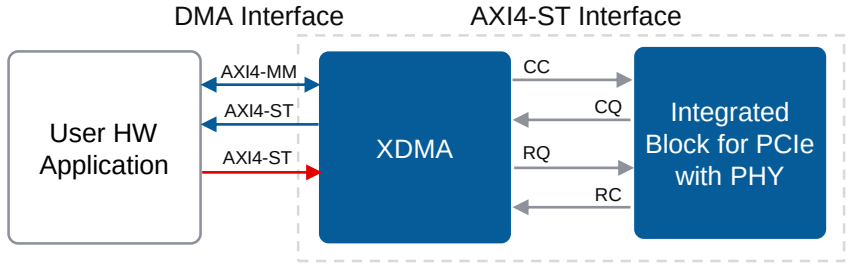
- PCIe PHY/PCS
- Use 3rd Party or In-House Soft IP for PCIe
- Custom PCIe Test Equipment

AXI4 Streaming



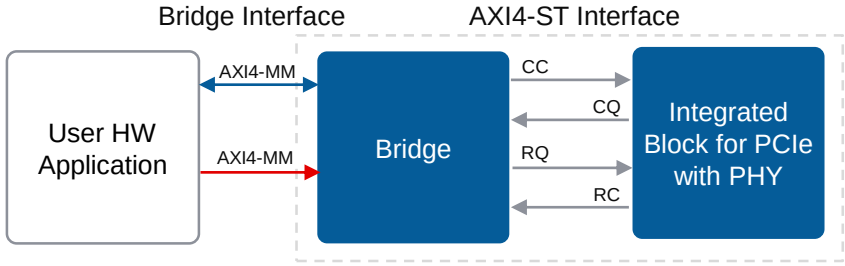
- Base IP for all Xilinx PCIe Subsystems
- Highest Performance Potential
- All Features Supported

XDMA



- High Data Throughput; Multiple Channels
- AXI Streaming or AXI MM Interfaces Available
- Good for Endpoint Data Plane Applications

Bridge



- Bridges AXI Memory and PCIe Memory Maps
- High Level Abstractions, Easy to Use
- Good for Control Plane Applications

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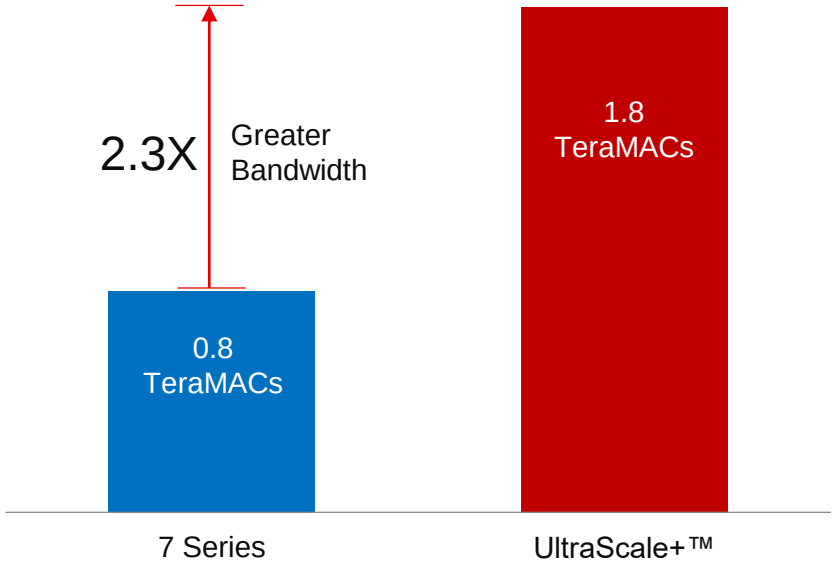
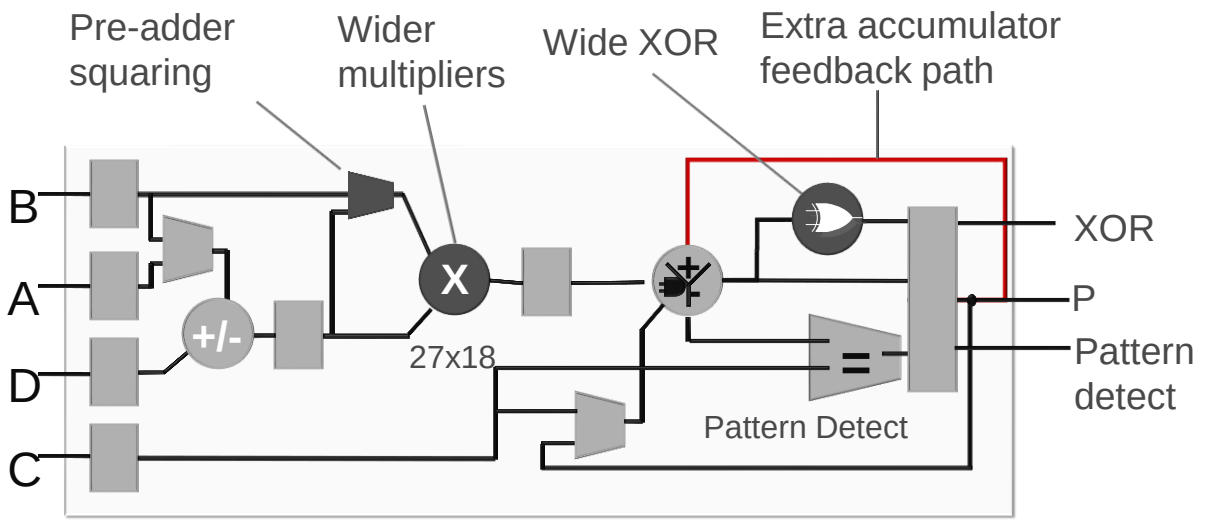
Massive DSP Bandwidth for Diverse Applications

Feature	Benefit
27x18 multiplier in a DSP slice 35x28 support in a DSP tile (2 slices)	• Optimal performance per block • Implement double-precision floating point in 30% less fabric (vs. 7 series)
Pre-adder squaring	• Perform “sum-of-square-difference” calculations in 50% fewer resources • More efficient motion estimation in video applications
Extra accumulator feedback path	Implement complex multiply-accumulate in half the resources
Wide XOR	Implement EFEC, CRC, ECC functionality
White box modeling	Full visibility with accurate simulation and debug





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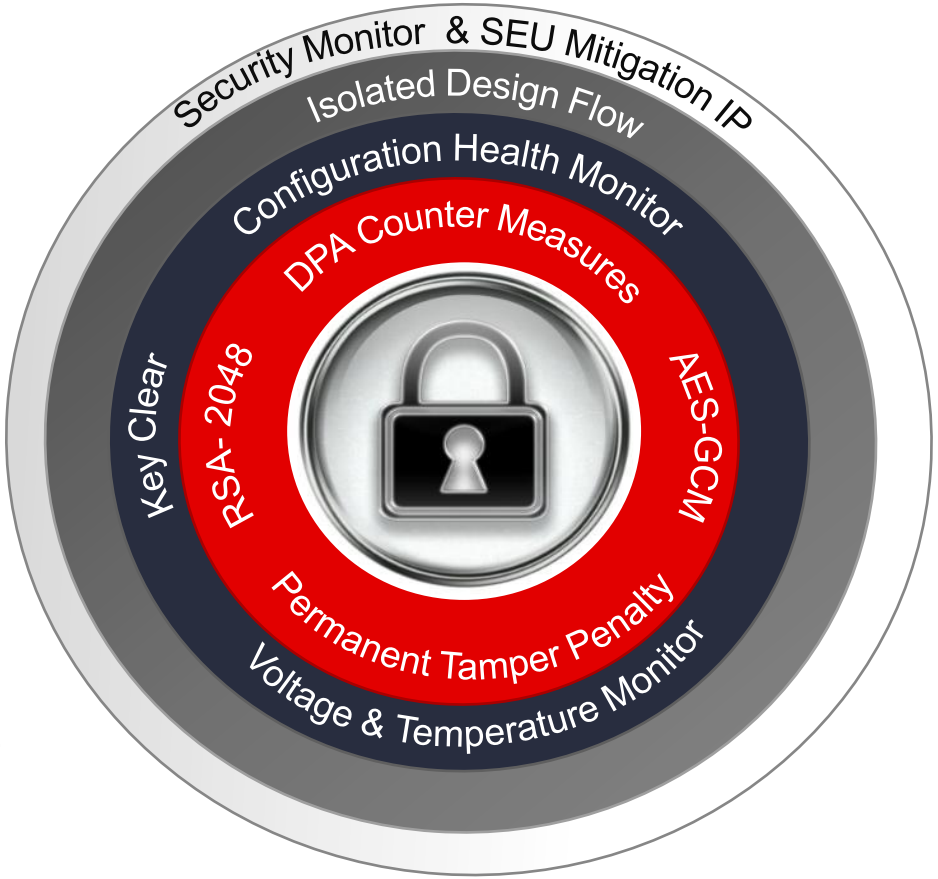
Adaptable to Security Threats across the Product Life Cycle

RSA-2048 Authentication
- Verify Design Source
- RSA Public Key Revocation

Key Agility
Update BBRAM Key from within the device w/o JTAG

Enhanced SEU Performance
Increased reliability availability and elimination of silent data corruption



Silicon Passive Features (pre-configuration)
Silicon Active Features (post-configuration)
Design Flow
IP

FPGA Design Security Hub

Permanent Tamper Penalty
- Prevents adversary from using security features of the device

AES-CGM Decryption
- NIST ✓
- Faster Configuration

DPA Counter Measure
Prevents the use of power or EM monitoring to extract keys

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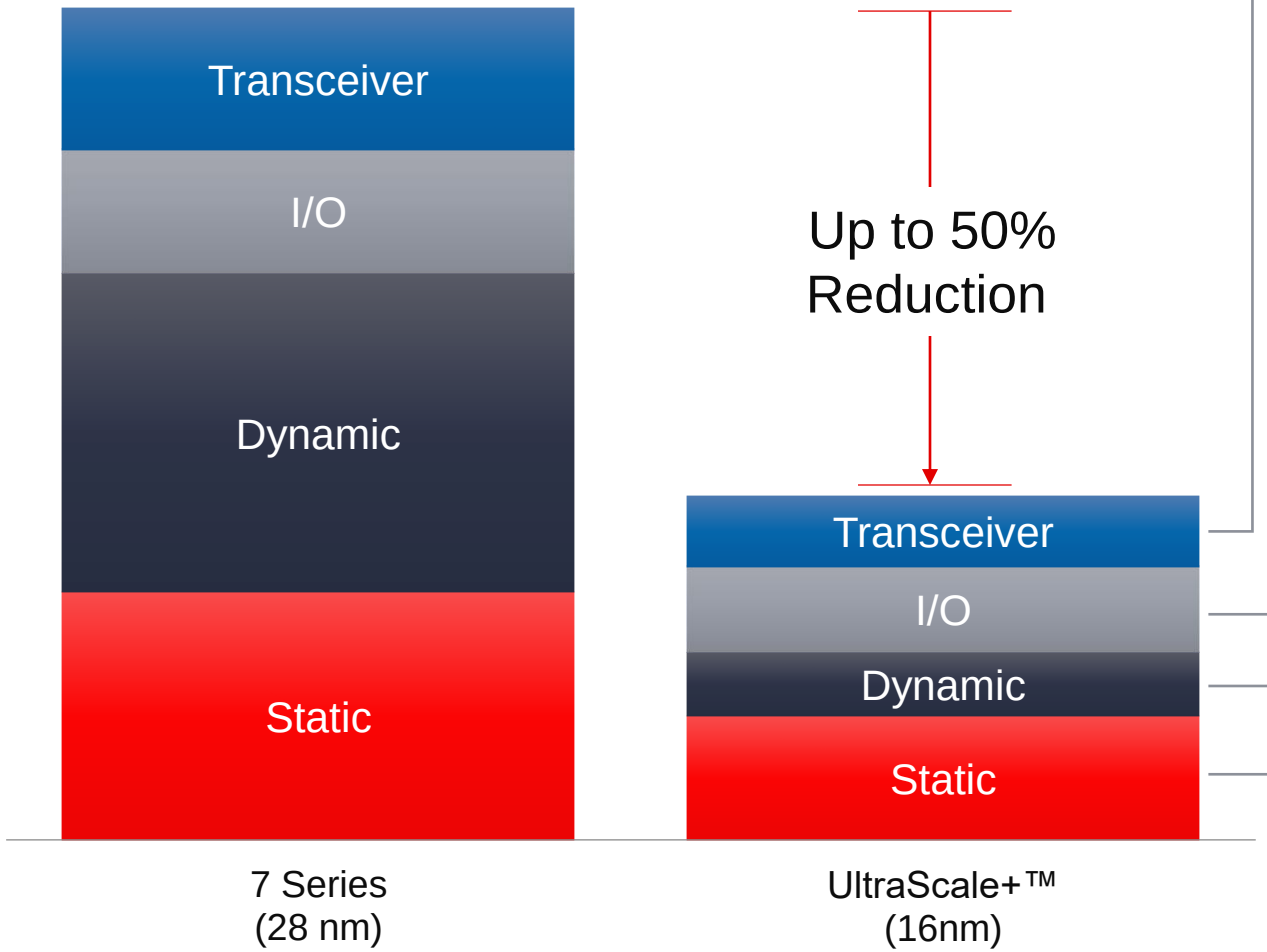
Power Optimizations at Every Level



- Architectural optimizations
- Low power mode

- I/O multi-mode control (cont'd from 28nm)
- DDR4 voltage reduction

- CLB packing & reduced wire length
- HW-based clock gating on leaf cells
- Block RAM hardened data cascading
- Block RAM dynamic power gating
- DSP hardened features
- MMCM & PLL lower supply voltage

- Process node
- 16nm FinFET power characteristics
- Power binning & lower voltage scaling
- Max process @100ºC

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Artix® UltraScale+™ vs. Artix-7

Blocks	Details	7A75T	AU10P	7A100T	AU15P	AU20P	7A200T	AU25P
Programmable Functionality	System Logic Cells (K)	75	96	101	170	238	215	308
	CLB Flip-Flops (K)	94	88	126	156	218	269	282
	CLB LUTs (K)	47	44	63	78	109	135	141
Memory and DSP	Max. Distributed RAM (Mb)	0.9	1.0	1.2	2.5	3.2	2.9	4.7
	Total Block RAM (Mb)	3.8	3.7	4.9	5.1	7.0	13.1	10.5
	36K Block RAM Blocks	105	100	135	144	200	365	300
	DSP Slices	180	400	240	576	900	740	1200
Clocking	Clock Management Tiles (CMTs)	6	3	6	3	3	10	4
Integrated IP	PCI Express®	PCIe Gen2	PCIe Gen4	PCIe Gen2	PCIe Gen4	PCIe Gen3	PCIe Gen2	PCIe Gen3
	AMS - System Monitor	1	1	1	1	1	1	1
I/O and GT	HD I/O (1.2 – 3.3V)	300	72	300	72	72	500	96
	HPIO	-	156	-	156	156	-	208
	GT @ 6.6Gb/s	8	-	8	-	-	16	
	GT @ 12-16.3 Gb/s	-	12	-	12	12	-	12

4:1
DSP:kSLC Ratio

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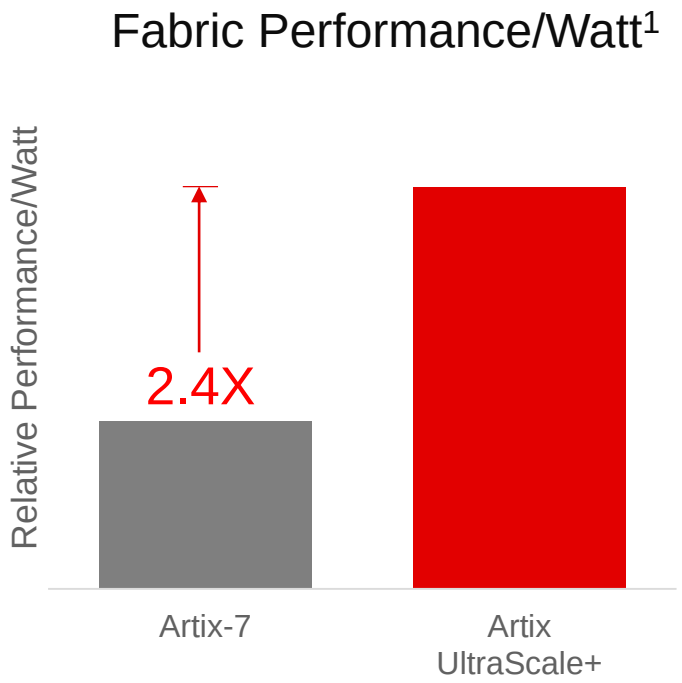
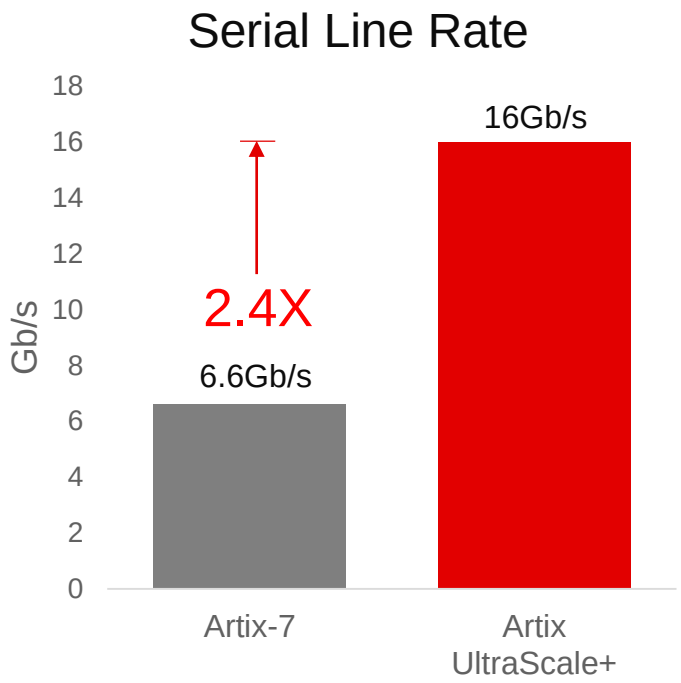
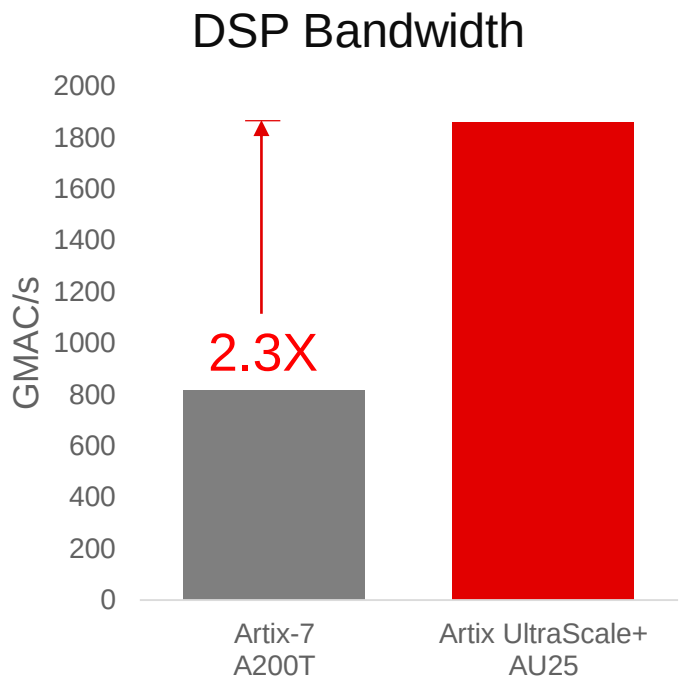
Doubles the Bandwidth and Performance/Watt vs. Artix-7

- Uniquely tunable operating voltage for adjustable fabric power/performance (up to 2.5X perf/watt)[1]
- 2.4X SerDes line rate, power-optimized, and next-generation equalization for optimal signal integrity
- Greater DSP performance and more efficient compute per DSP tile







1: Artix® UltraScale+™ FPGA delivers 1.6X performance at .8X power at V_{NOM} (0.85V) or 1.2X performance and .5X power at V_{LOW} (0.72V); Artix-7 FPGA at V_{NOM} = 1V

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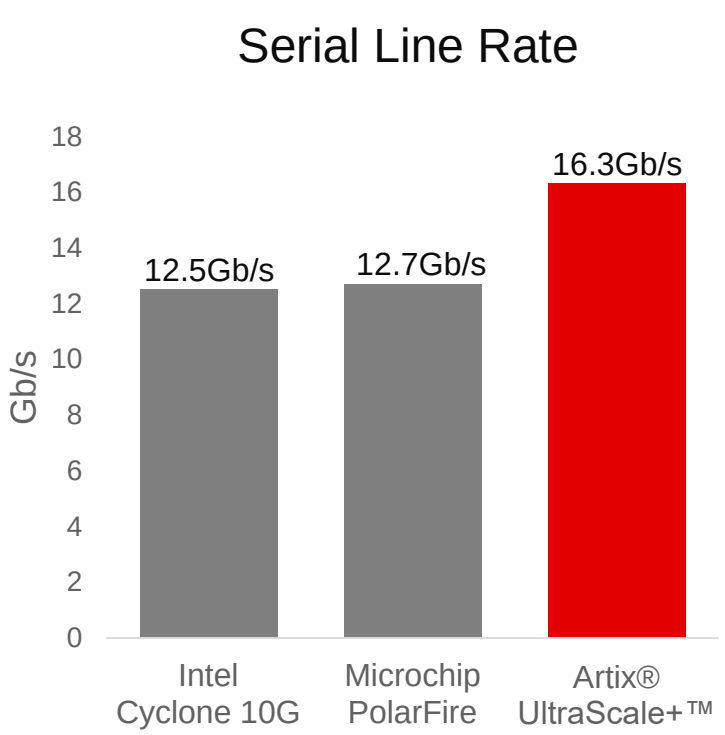
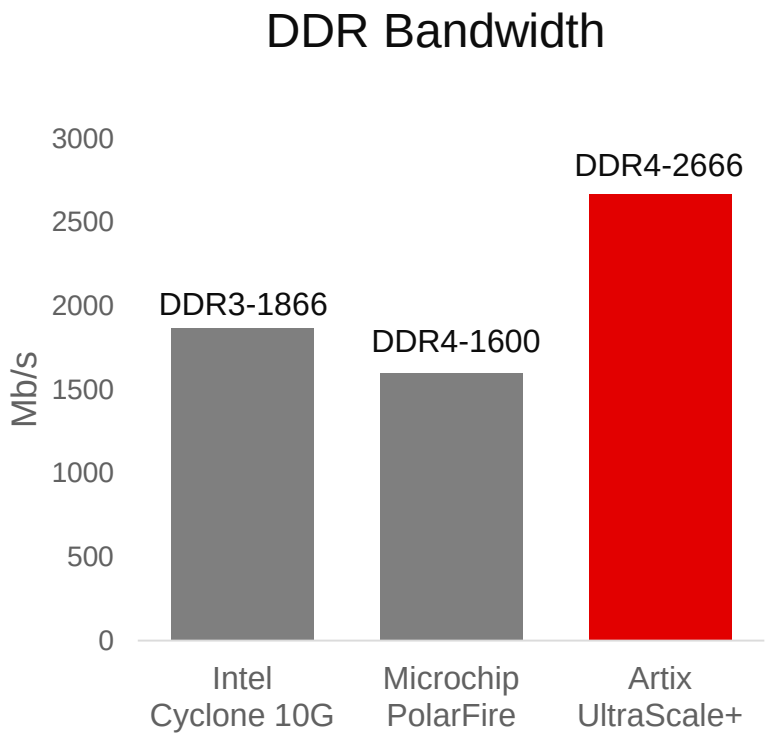
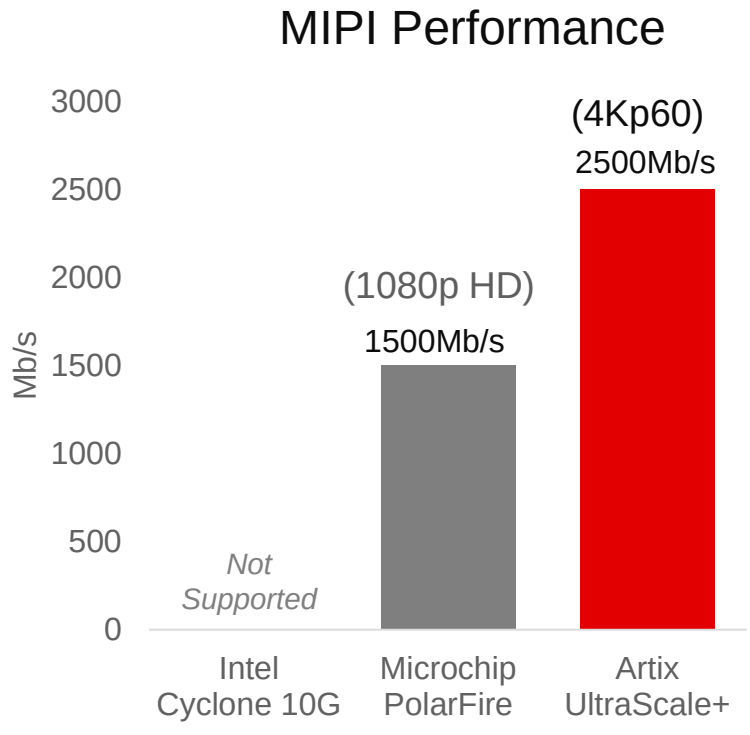
Best-in-Class FPGA I/O Performance (vs. Competition)

- Highest SerDes rates for advanced protocols (including PCIe® Gen4) in a cost-optimized device
- Highest DDR memory performance
- Highest MIPI performance for latest vision sensors (“4K/8K Ready”)







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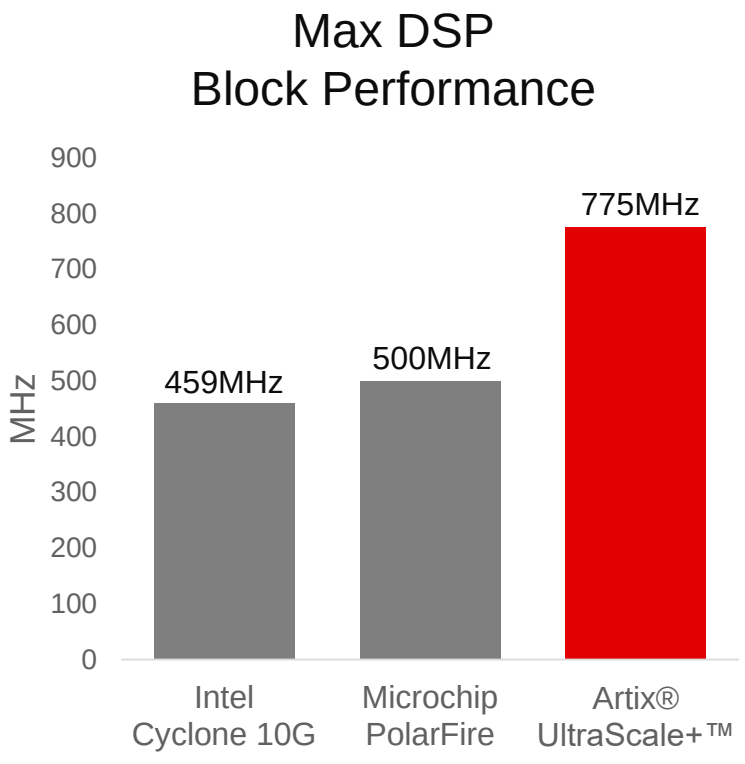
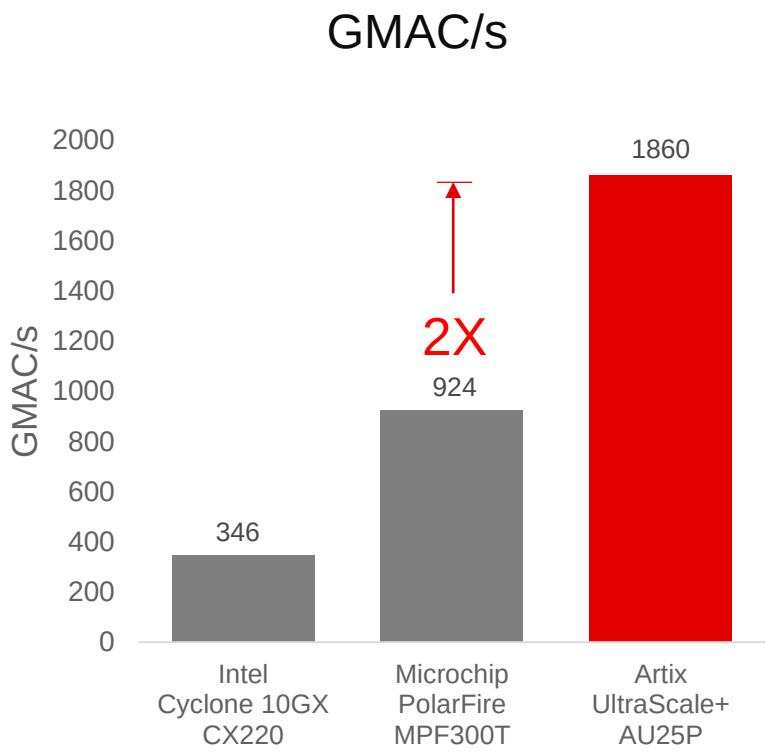
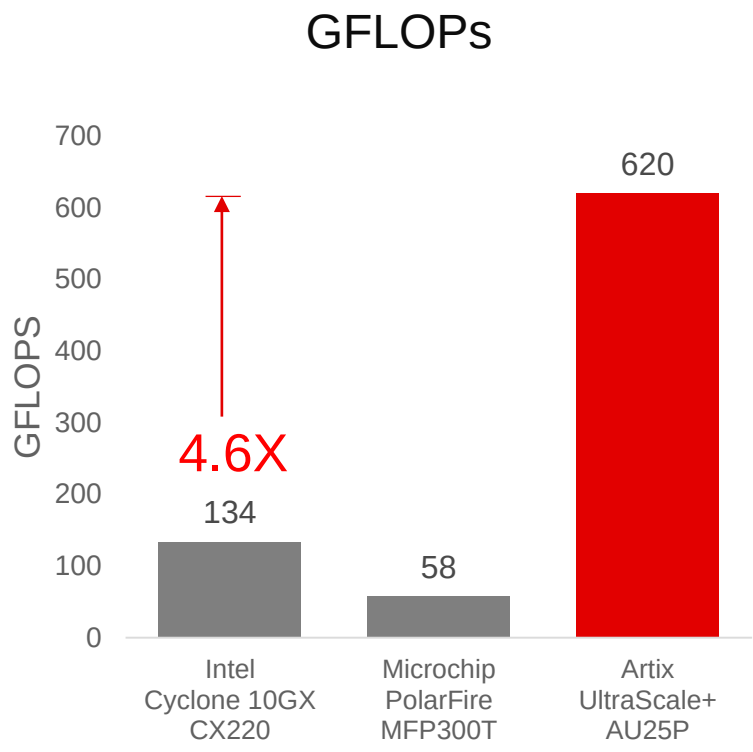
Best-in-Class FPGA Signal Processing & Compute

- Highest performance DSP, optimized for fixed-point and floating point
- Flexible for diverse forms of compute for image & video processing, real-time control, and AI inference



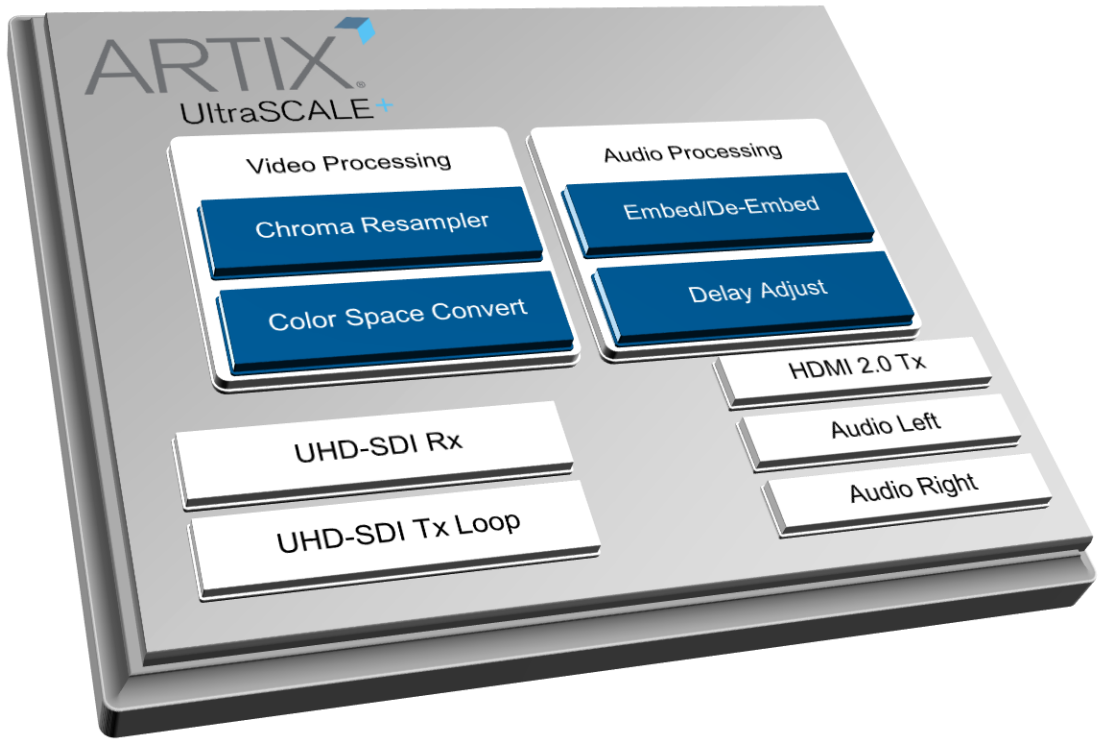




Source for Intel Cylcone10GX: Intel Cyclone 10 GX FPGAs Product Table
Source for Microsemi PolarFire: MicroSemi PolarFire FPGA Data Sheet, CoreFPU v2.0 Handbook,

Artix UltraScale+ FPGAs for 4K UHD Video Converters

SDI to HDMI Converter



Video Converter Requirements

- Support any 4Kp60 video interface
- Integrate real-time UHD video processing pipelines
- Small PCB with fan-less enclosure

Artix® UltraScale+™ Capabilities

- Xilinx-developed IP for SDI, HDMI, DisplayPort, and AES
- Video processing handles resampling and color space conversion
- Add real-time scaling, deinterlacing, and mixing if required
- Low power eases thermal design
- Scalability to support multiple AV channels in a single device
- Bridge to Ethernet (1GbE or 10GbE) for AV-over-IP and streaming

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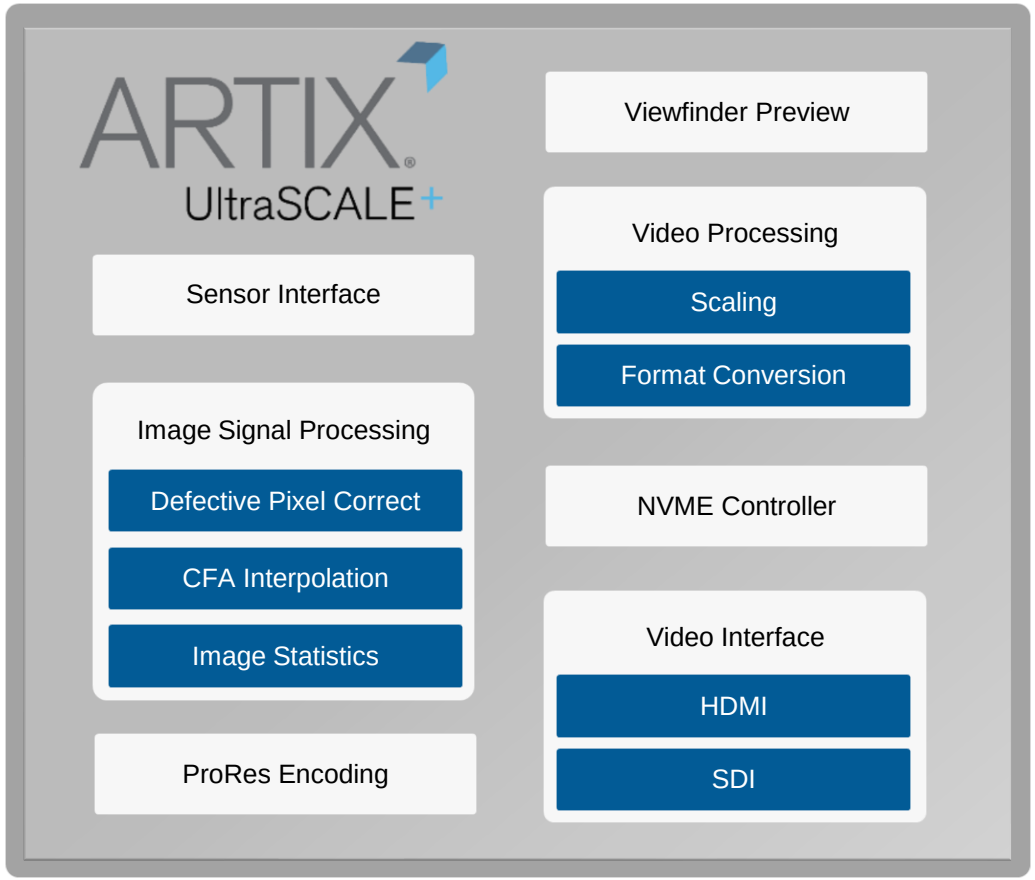
Artix UltraScale+ FPGAs with InFO for 8K Camcorders

Camcorder Requirements

- Tunable image signal processing (ISP) to match sensor characteristics
- Selectable codec for local storage and playback
- Real-time 8K video processing (including image stitching from 360° cameras)
- Space constrained and battery powered

Artix® UltraScale+™ Capabilities

- High-performance transceivers supporting HDMI, DisplayPort, and SDI
- High-speed logic and parallel DSP for video processing and compression
- Integration of multiple interfaces/chips into a single device
- Low power for battery use
- InFO packaging to reduce PCB area



XILINX

How Customers Can Get Started

- Documentation Available Now
- Tools Available
  - AU25P in Vivado® Design Suite 2021.1.1 Now
  - AU20P in Vivado Design Suite 2021.2 (Oct'21)
  - AU15P, AU10P EA in Vivado Design Suite 2021.2 (Oct'21)
- Silicon Available
  - AU25P, AU20P Production Now
  - AU15P, AU10P Early Access Q1'22
  - AU15P, AU10P Production in Q2'22

Opal Kelly XEM8320

Artix® UltraScale+™ FPGA Development Platform

Opal Kelly XILINX

Opal Kelly Incorporated

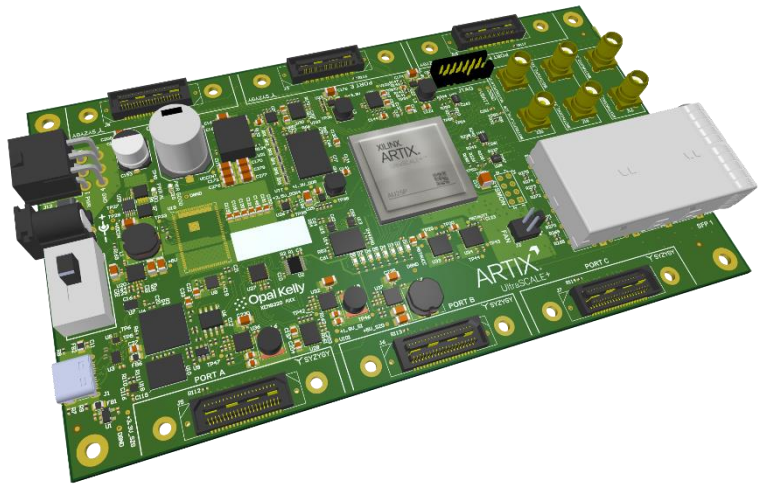
Company Overview

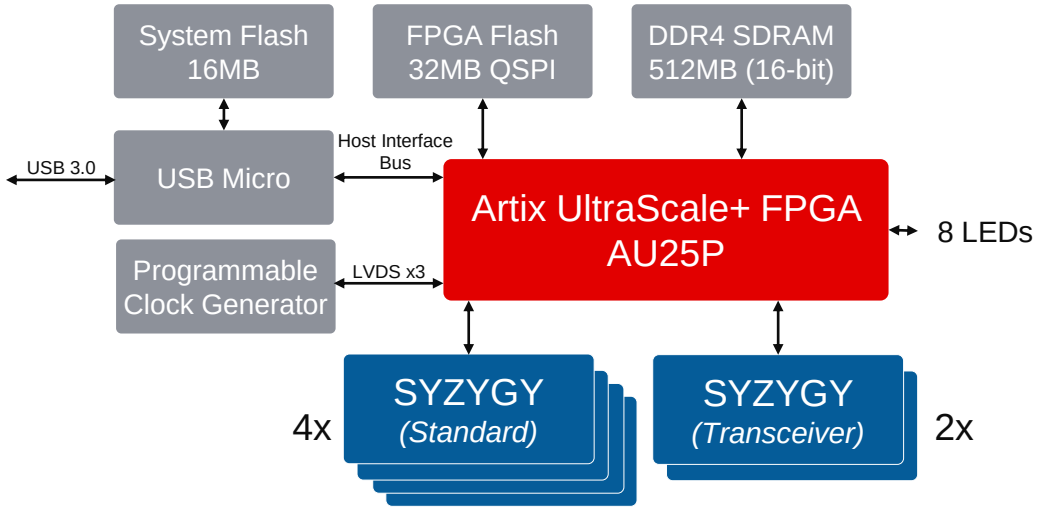
- Founded in 2004 with the introduction of FrontPanel USB 2.0
- FrontPanel SDK for rapid prototyping and proof-of-concept
- Robust API and life cycle managed modules for low- to mid-volume production
- Introduced SYZYGY connectivity standard in 2017
- ISO 9001:2015 QMS; certified 2019
- Markets
  - Data acquisition • machine vision • software-defined radio • university labs • test & measurement • research-grade scientific instrumentation • radar • LiDAR • satellite imaging • remote sensing • HW/SW simulation

Opal Kelly XILINX

XEM8320-AU25P FPGA Development Platform

Featuring the Artix® UltraScale+™ AU25P device



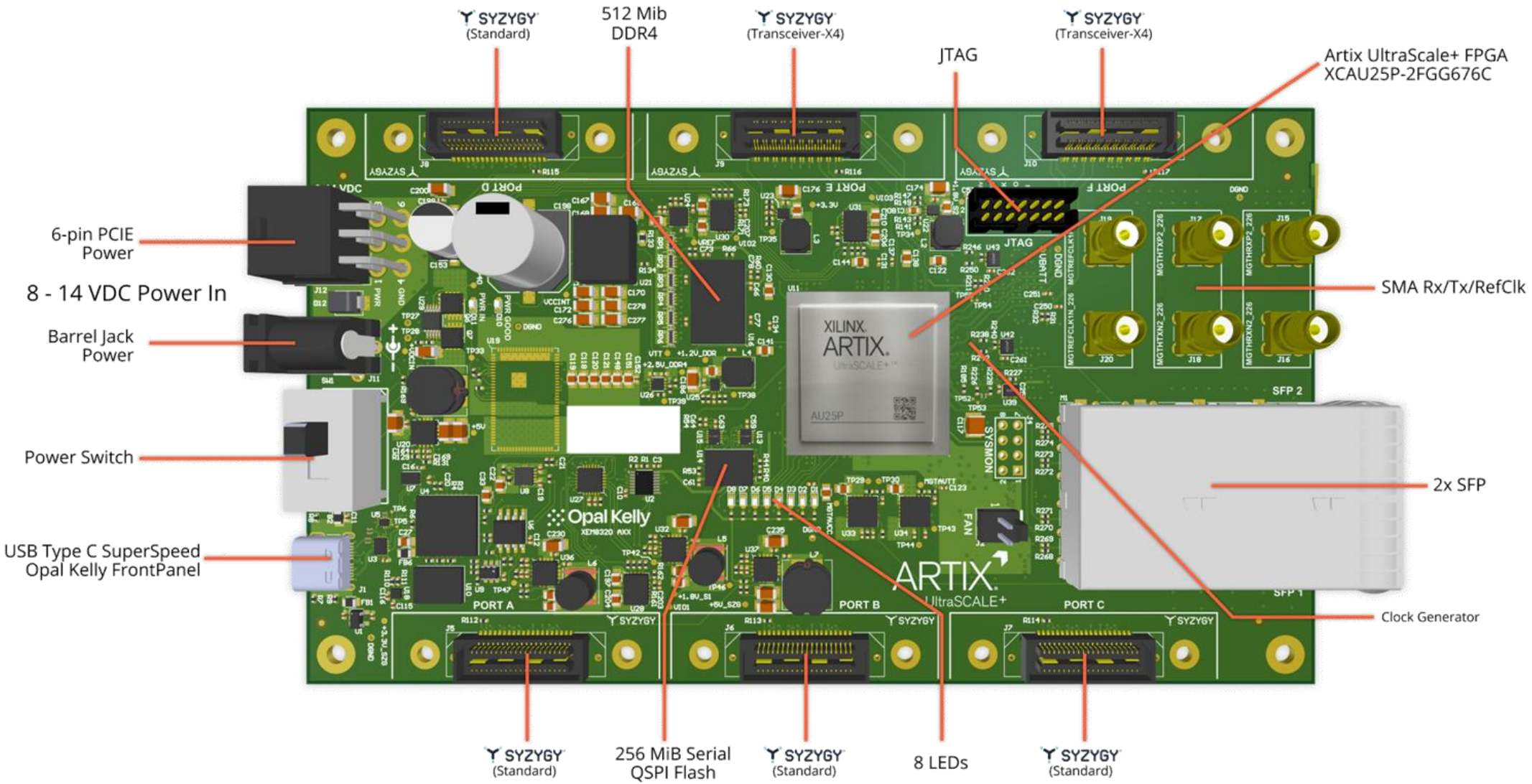


Host Interface	USB 3.0 Type C, SuperSpeed FrontPanel Support
FPGA	XCAU25P-2FGG676C
Memory	512 MiByte DDR4, 16-bit wide data
NV Memory	16 MiB System Flash 32 MiB FPGA QSPI Flash
Oscillator	3-output programmable
FPGA I/O Voltage	Up to +3.3V

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC Input	+8.0		+14.0	VDC
DC Input Ripple	-	-	50	mVp-p
Operating Temperature	0	-	+70	°C
Storage Temperature	-50	-	+100	°C
Weight		73		grams
Clock Frequency		1 - 350		MHz
Clock Jitter		0.5		ps RMS

Opal Kelly XILINX

XEM8320 Board Features



FrontPanel SDK

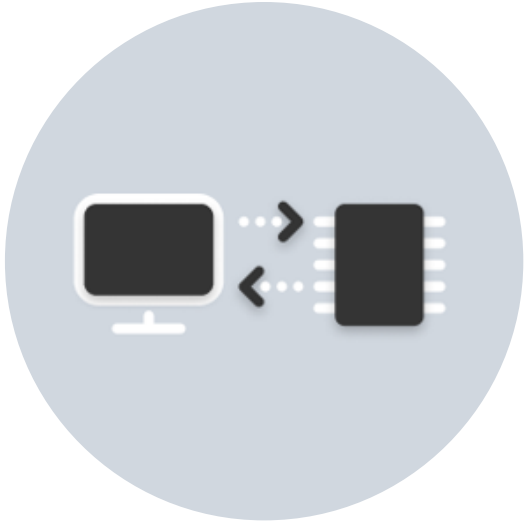
Build high-performance software connected FPGA applications for prototypes, proof-of-concept, and production

- Turnkey high-performance SW/HW integration
- Ideal for rapid development of prototypes and proof-of-concept
- Production-ready with thousands of customer deployments
- Stand-alone desktop app or API for custom integration
- Lightweight FPGA footprint
- Behavioral simulation

FrontPanel

Opal Kelly XILINX

FrontPanel System Components

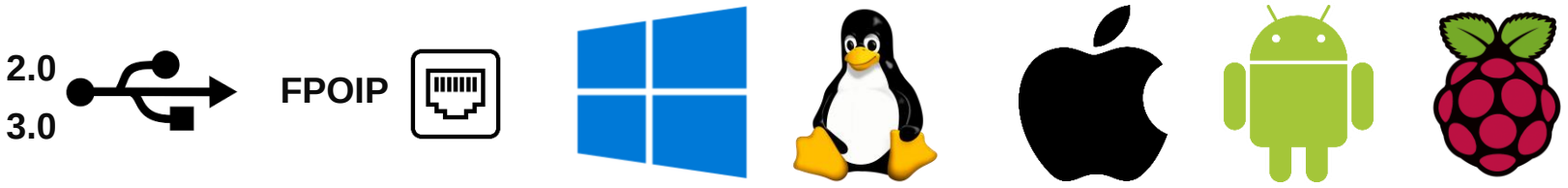


Software API and a robust driver to communicate with your device over USB, PCIe®, or the Internet

Proprietary device firmware to manage FPGA configuration and communication as well as other device management and monitoring

Lightweight FPGA IP blocks that integrate with your HDL to make host communication simple and easy

FrontPanel API Platform Support



C++ C# Python Java JavaScript

3rd-party Library (e.g., MATLAB®, LabVIEW)

FrontPanel

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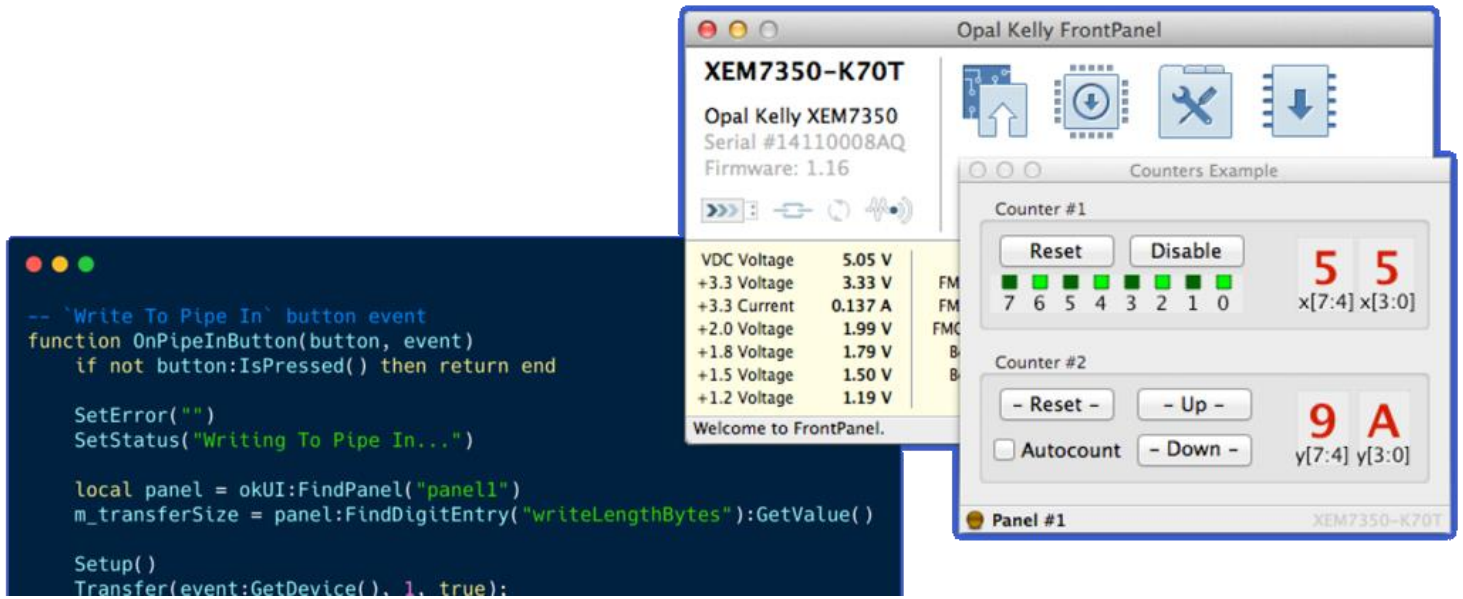
FrontPanel Desktop App

- Rapid user interface prototyping with virtual UI elements
- Text-based XML UI description file
- Supports wire, trigger, and pipe endpoints
- Business logic implemented in Lua scripts



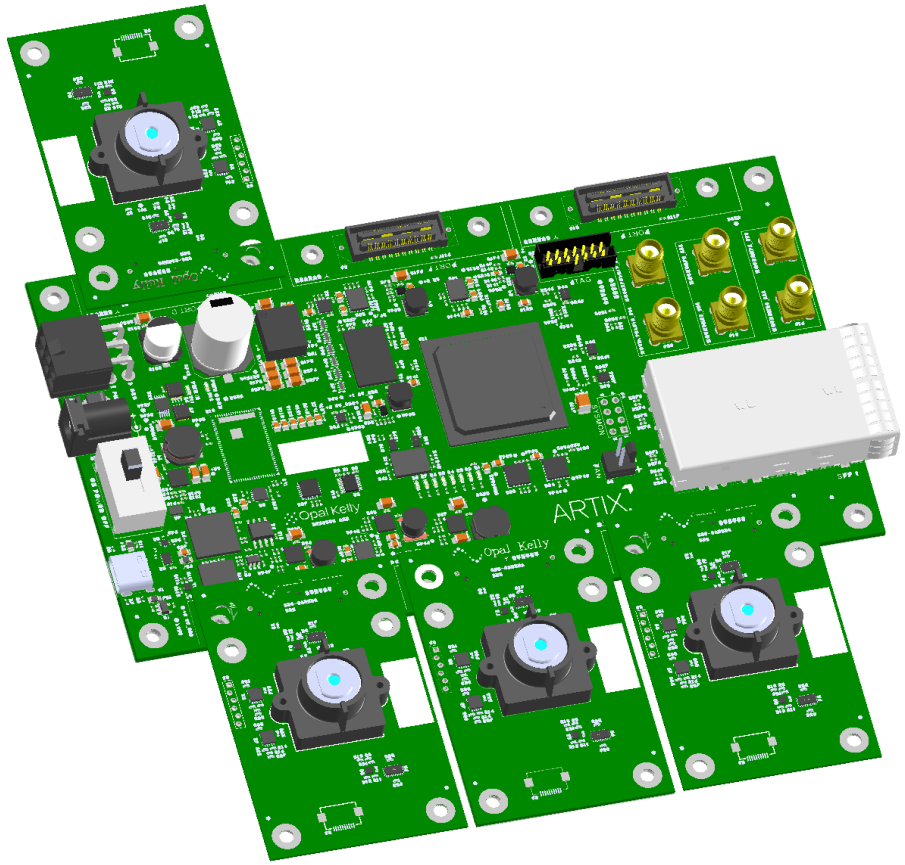
- LEDs
- Hexadecimal displays
- Sliders
- Pushbuttons
- Checkboxes
- Toggle buttons
- Numerical Entry

FrontPanel

Opal Kelly XILINX

Camera Reference Design

- Color image sensor – 3.4Mpixel, 60fps, global shutter
- SDRAM-based multi-buffer image capture pipeline and memory controller
- Cross-platform C++ GUI Desktop App
- Browser-based JavaScript built on FrontPanel-over-IP
- Free download
- SZG-CAMERA sold separately



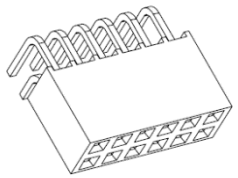
Reference design supports up to four cameras

FrontPanel

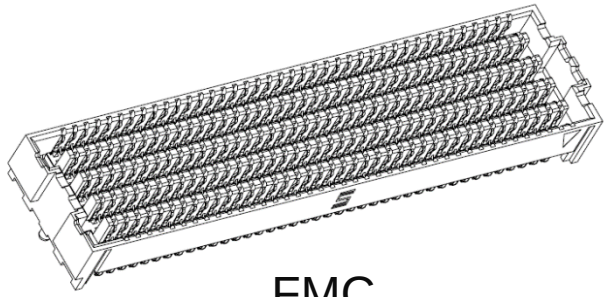
Opal Kelly XILINX

SYZYGY Overview

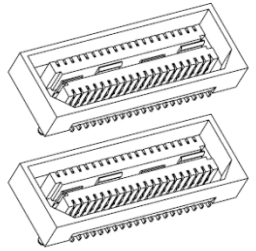
- High-performance standardized FPGA / peripheral connectivity
- Higher performance than Pmod
- Less “pin greedy” than FMC
- SmartVIO is compatible with FPGA I/O architectures
- Cable-capable and impedance controlled



Pmod



FMC



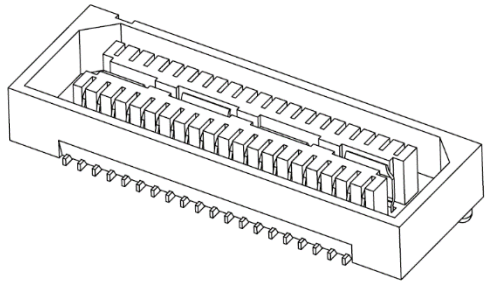
SYZYGY

SYZYGY® by Opal Kelly

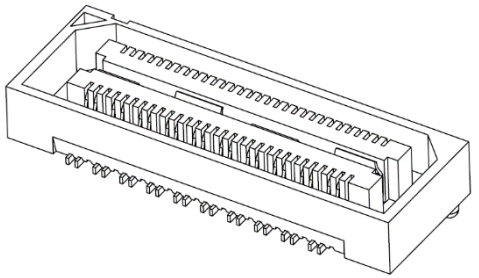
Opal Kelly XILINX

SYZYGY Benefits

- Modern connectivity for data acquisition, instrumentation, and sensing
- Modular, adaptable, expandable
- Customers get further, faster
- Longer useful life of the development platform
- Learn more at SYZYGYFPGA.IO



Standard
40-pin, 0.8mm pitch



Transceiver
40-pin, 0.5mm pitch

SYZYGY® by Opal Kelly

Opal Kelly XILINX

SYZYGY Peripherals

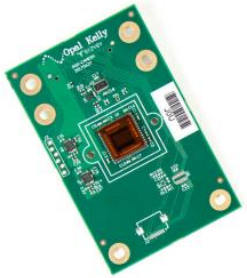
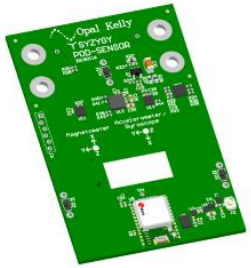


Image Sensor
3.4 Mpx, 60fps

Analog-to-Digital
Dual 40 MSPS, 12-bit



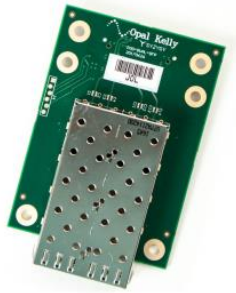
Multi-Sensor
GPS, motion, light

Digital-to-Analog
Dual 125 MSPS, 12-bit

Breakout
(Standard)

Breakout
(Transceiver)

Digilent PMOD
x4



Networking
Dual SFP

Also Available...

Test Board (Standard)
Test Board (Transceiver)
6” Standard Cable
6” Transceiver Cable

From Digilent...

Zmod AWG 1411
Zmod Scope 1410

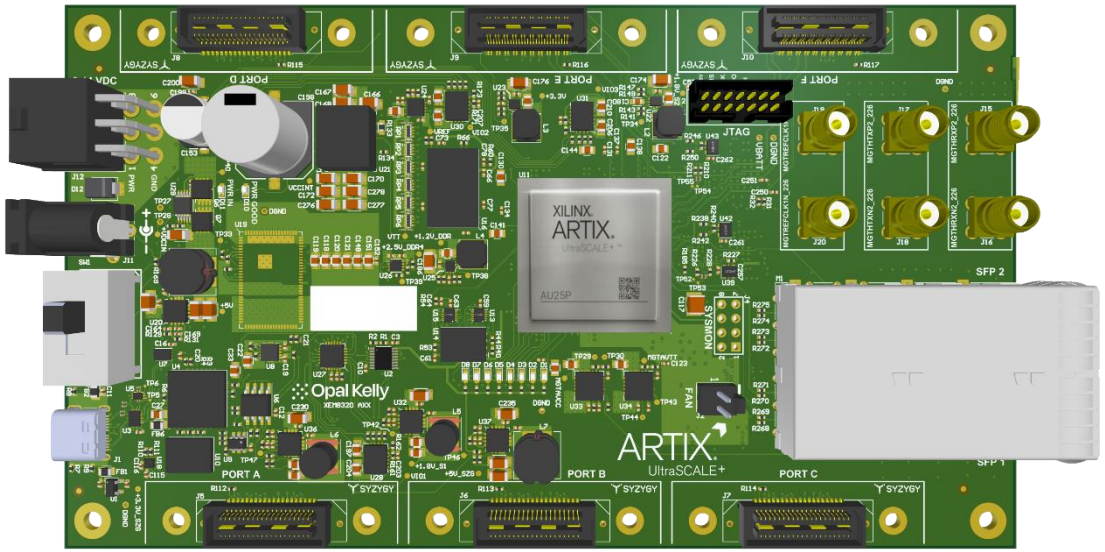
Coming Soon...

PCI Express (x4)
1 Gb Ethernet PHY
Instrumentation DAC+ADC

SYZYGY® by Opal Kelly

Opal Kelly XILINX

XEM8320-AU25P Price and Availability



$1,299.95

opalkelly.com

xilinx.com

Pre-order now
Shipping October 2021

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XEM8310-AU25P SOM

COMING SOON

opalkelly.com

XILINX

Useful Links

- Xilinx.com
  - https://www.xilinx.com/products/silicon-devices/fpga/artix-ultrascale-plus.html
- Opal Kelly XEM8320-AU25P Evaluation Kit
  - https://www.xilinx.com/products/boards-and-kits/1-1ihf3st.html
- Xilinx Vivado®/Vitis™ Tool Downloads
  - https://www.xilinx.com/downloads
- Opal Kelly FrontPanel SDK
  - https://opalkelly.com/products/frontpanel/
- Syzygy Ecosystem
  - https://syzygyfpga.io/

Q & A