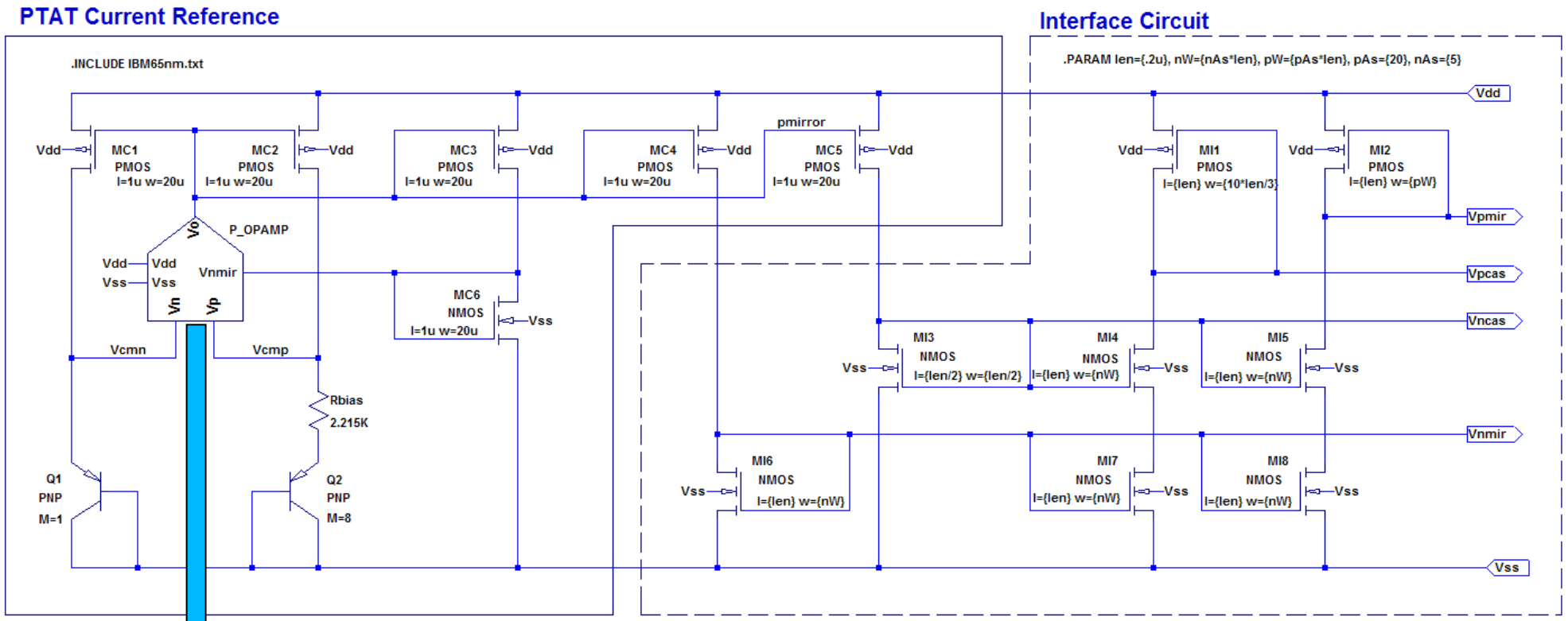
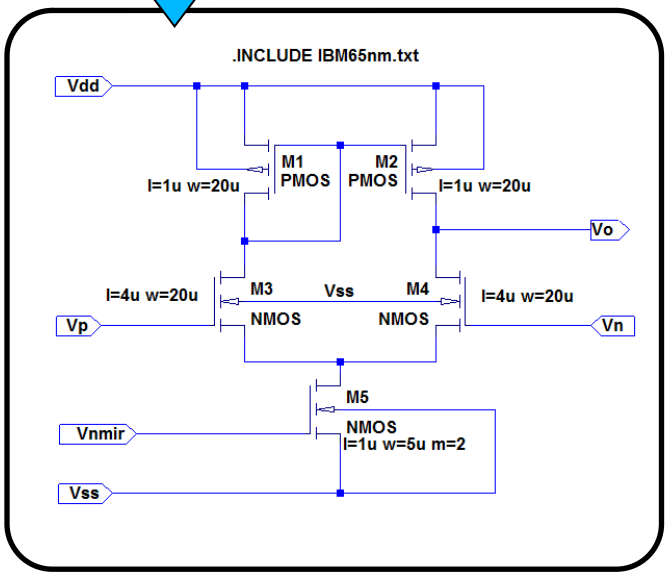
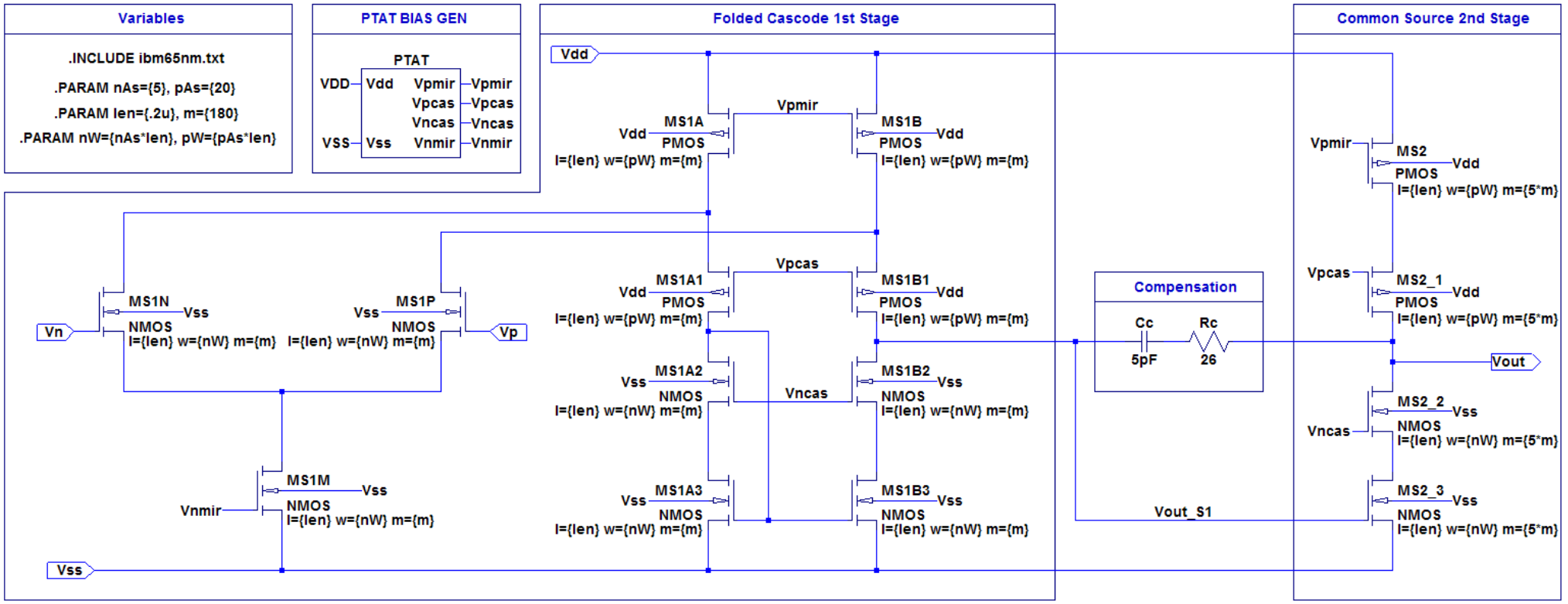
PTAT Circuit





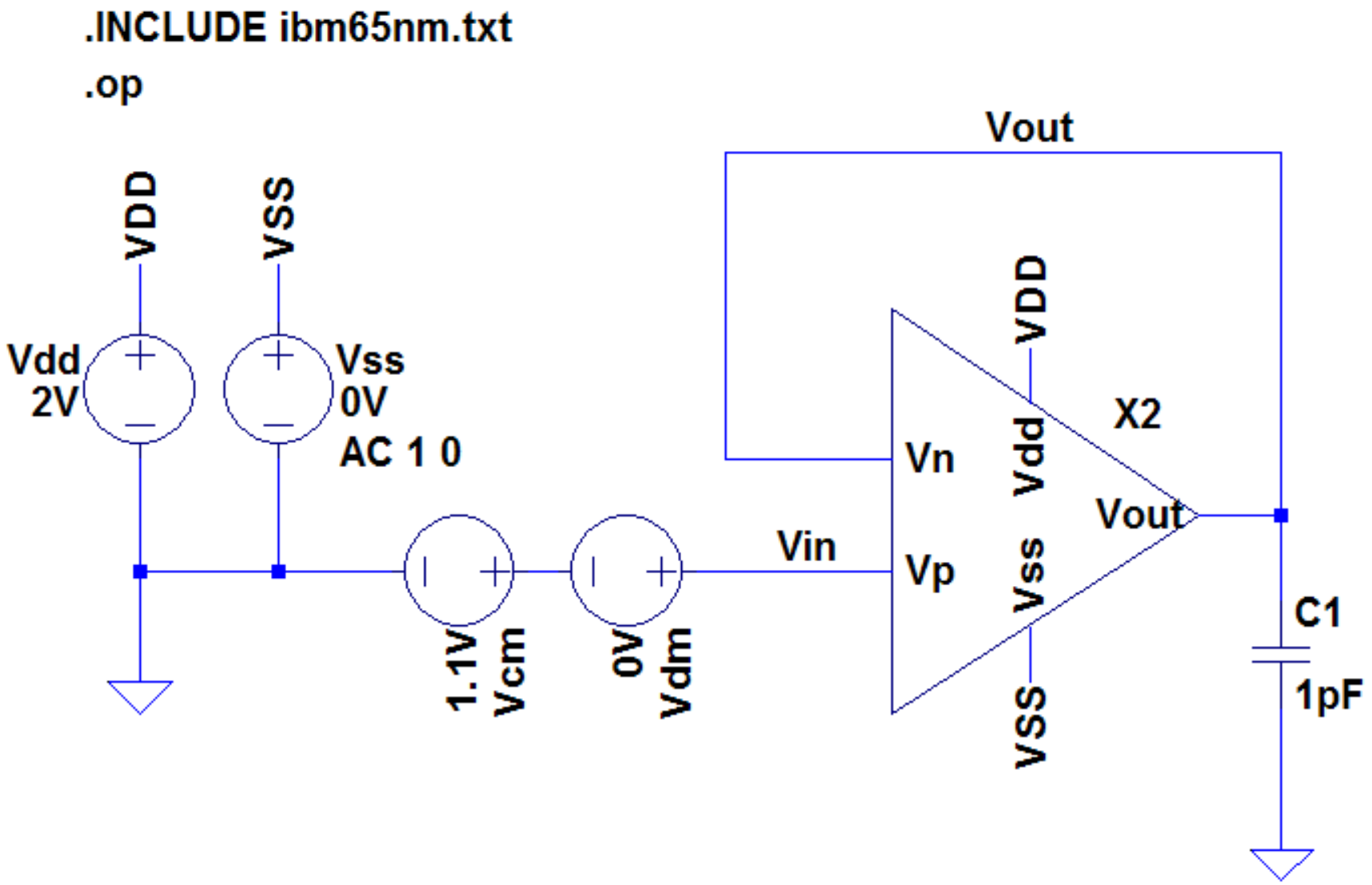
The following PTAT circuit shall be used for this project. This circuit shall derive all bias voltage for the opamp current sources. The reference current is now set to

2 Stage Folded Cascode Opamp

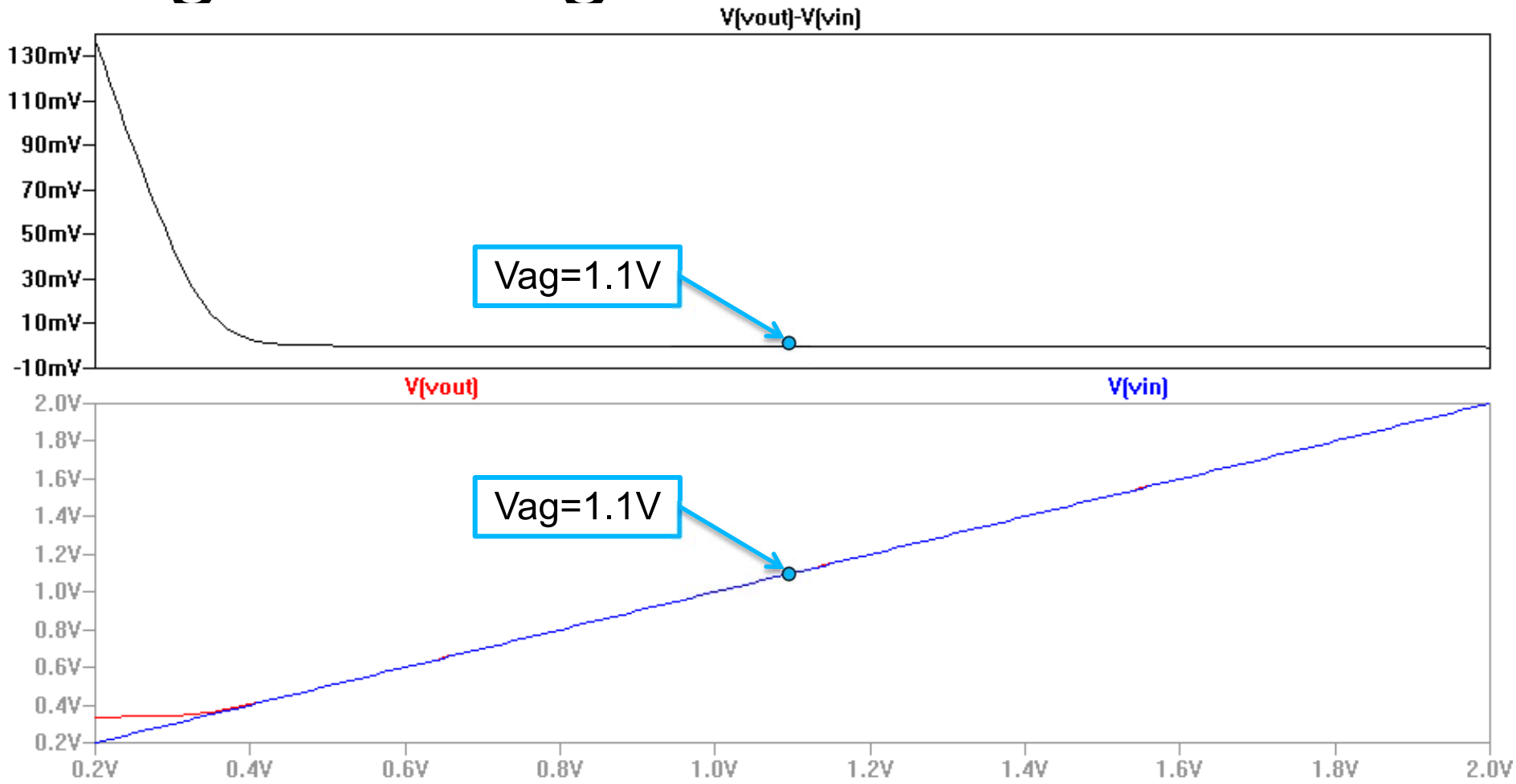


The following schematic is for a 2-stage opamp that uses the folded cascode topology for the first stage and a cascoded common source amplifier for the second stages. These amplifiers should get ~60dB and ~40dB of gain respectively. When combined the cumulative gain should be >100 dB

Unity Gain Test Bench



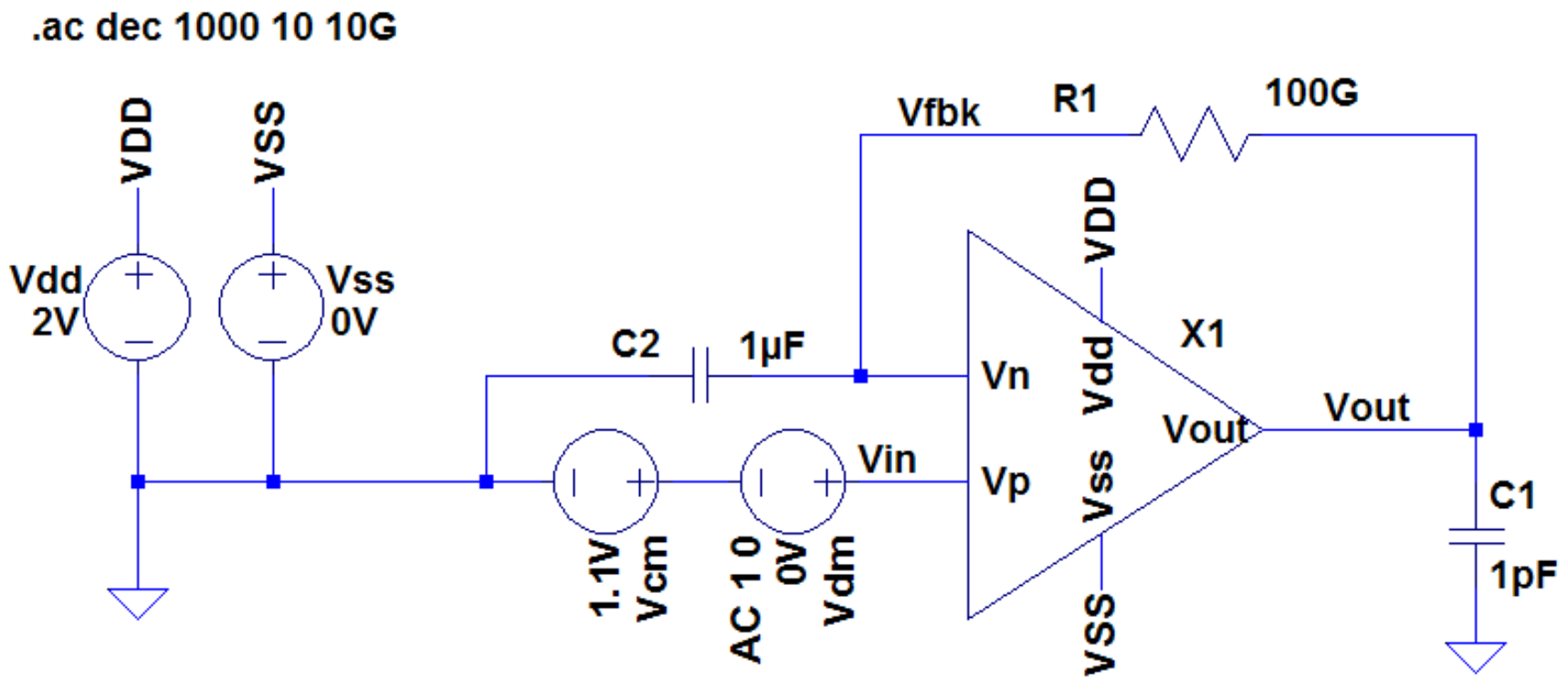
Vag – Analog Reference Ground



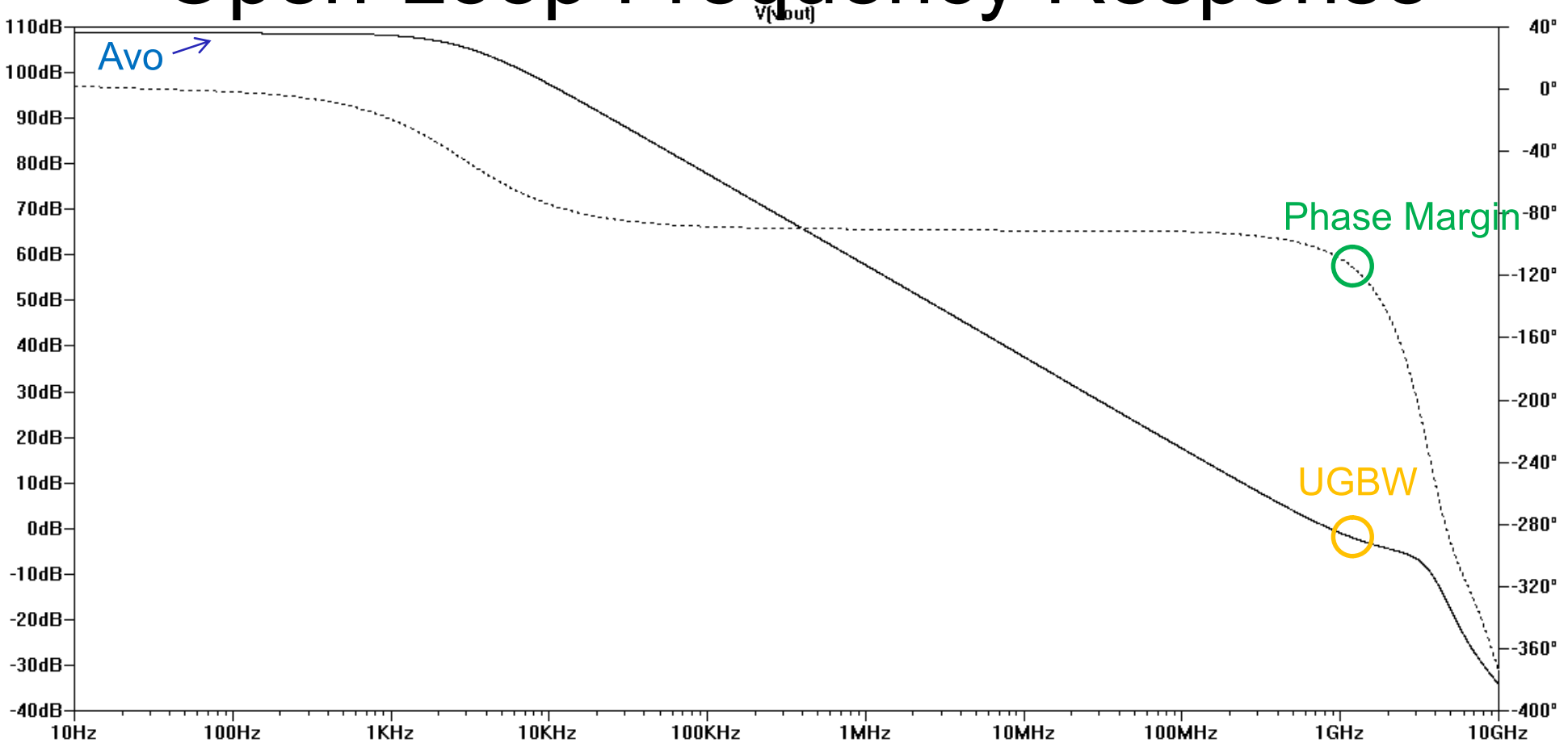
.dc vcm 0.2V 2V 0.01V

Vag Analog Reference Ground
1.1V

Open Loop Test Bench

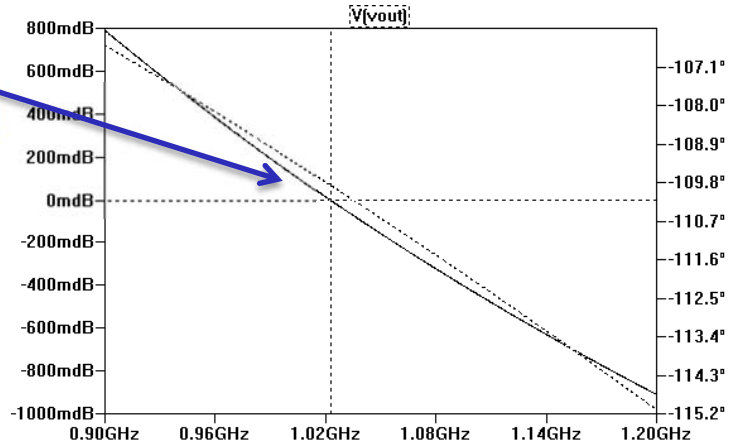


Open-Loop Frequency Response



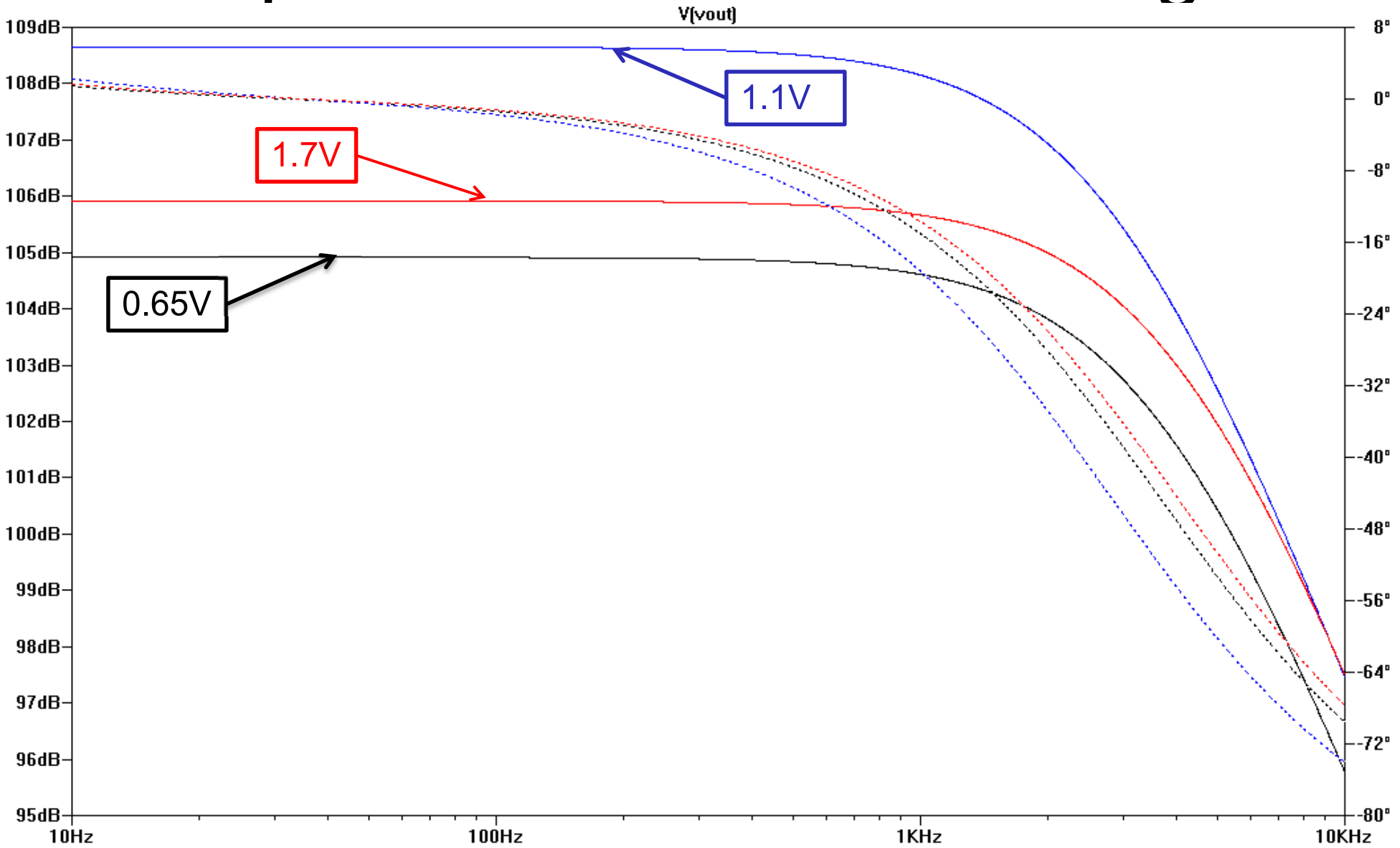
.ac dec 1000 10 10G

Linear Scale close to UGBW



DC Gain (Avo)	Phase Margin (PM)	Unity Gain Bandwidth (UGBW)
108.6 dB	180º-109.9°=70.1º	1.0229GHz

Input Common-mode Range

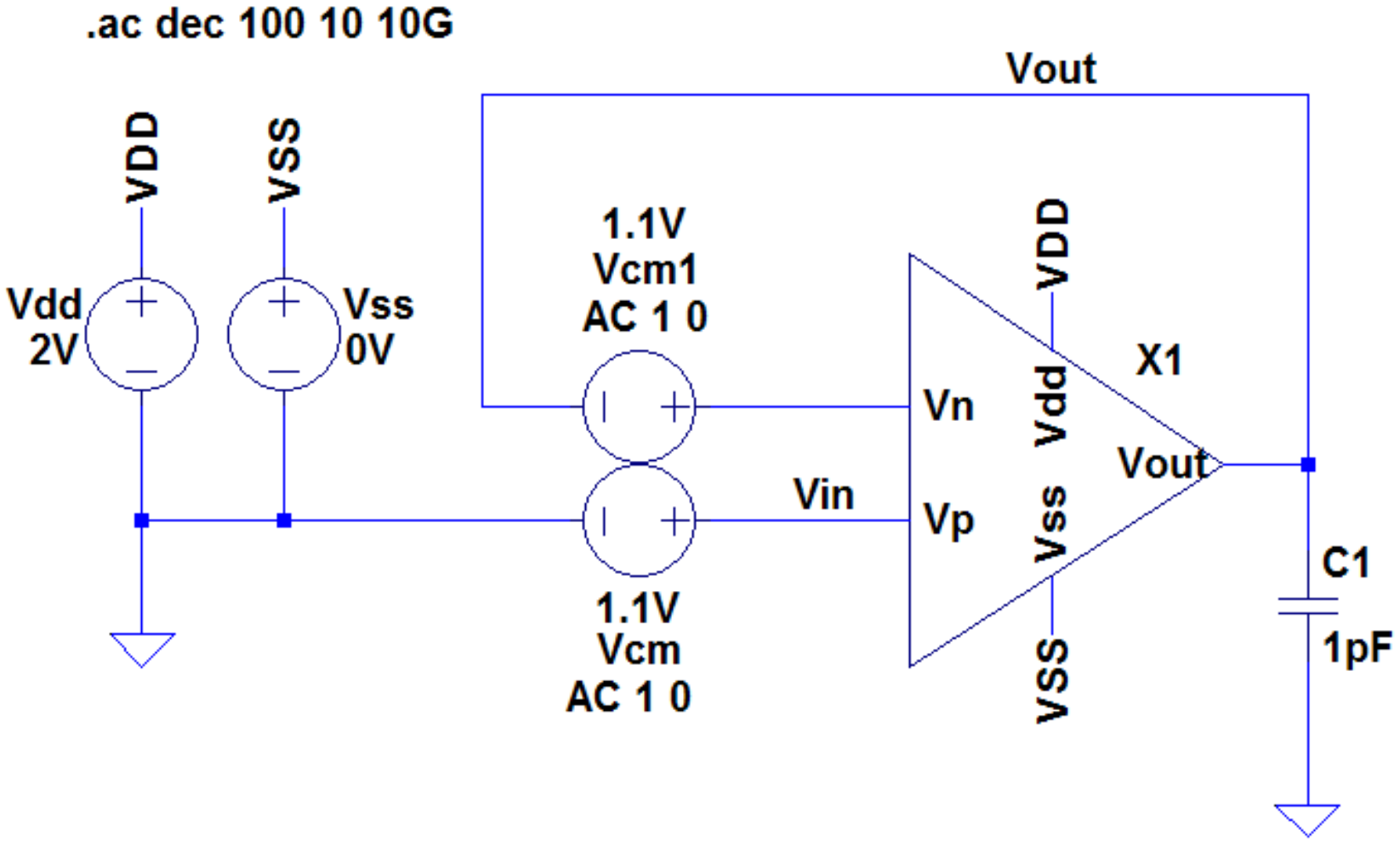


.ac dec 1000 10 10K

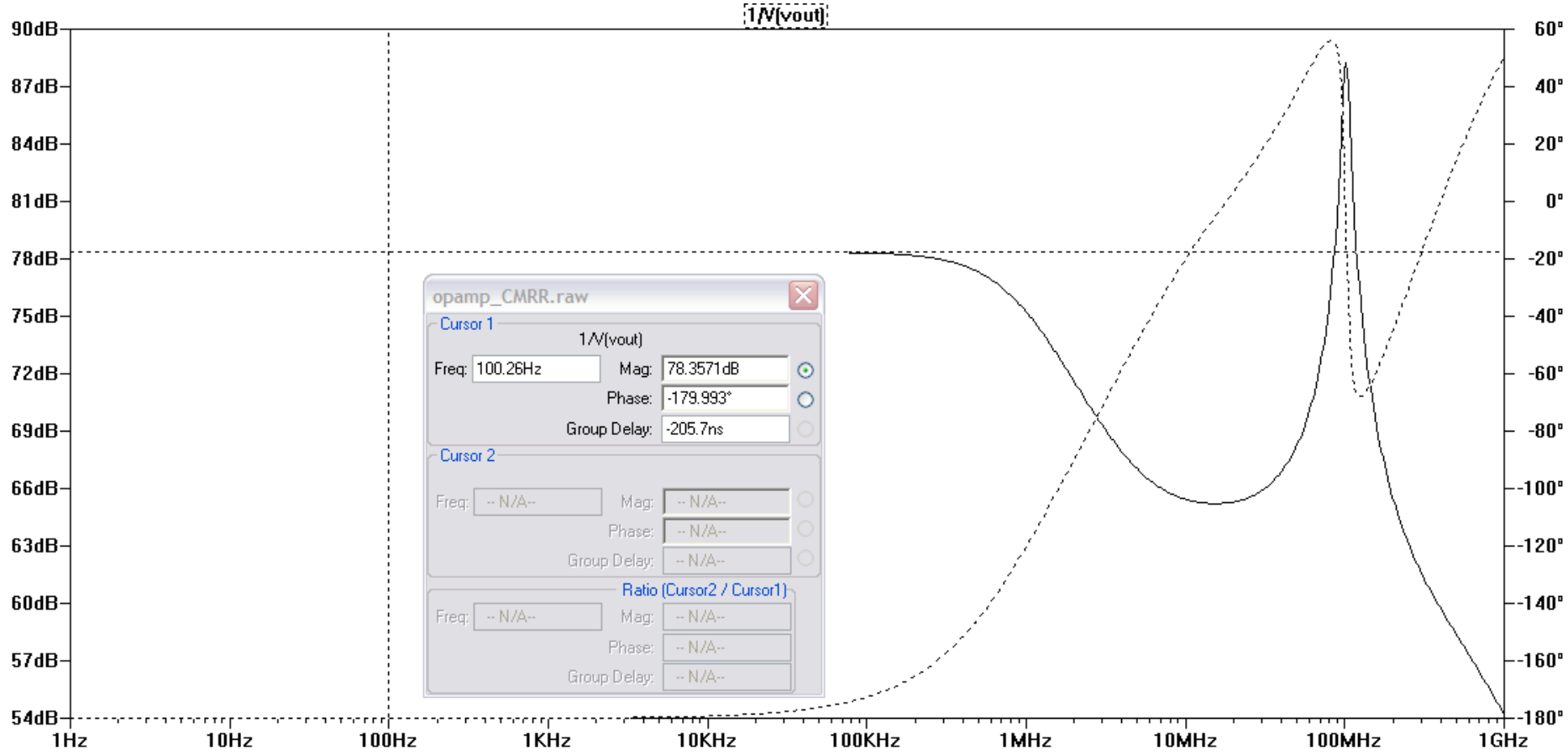
.STEP VCM LIST 0.65V 1.1V 1.7V

ICMR
0.65 V to 1.7V

CMRR Test Bench



Common Mode Rejection Ratio - CMRR

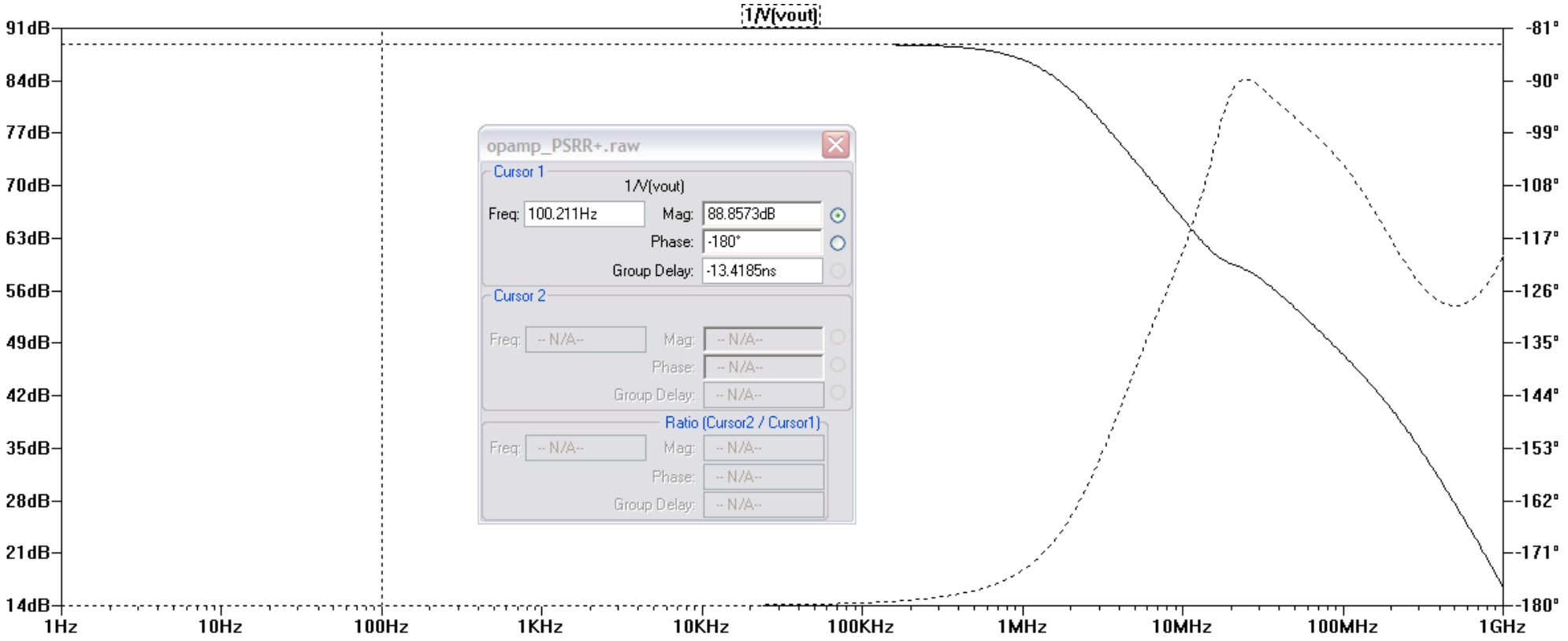


.ac dec 1000 1 1G

In order to find the Common Mode Rejection Ratio or CMRR, an AC analysis is performed on the CMRR test bench using the SPICE directive shown with “AC 1 0” stimuli applied to both Vcm sources. After simulation, the 1/Vout is analyzed to find the rejection ratio.

Common Mode Rejection Ratio (CMRR)
78.4 dB

PSRR+

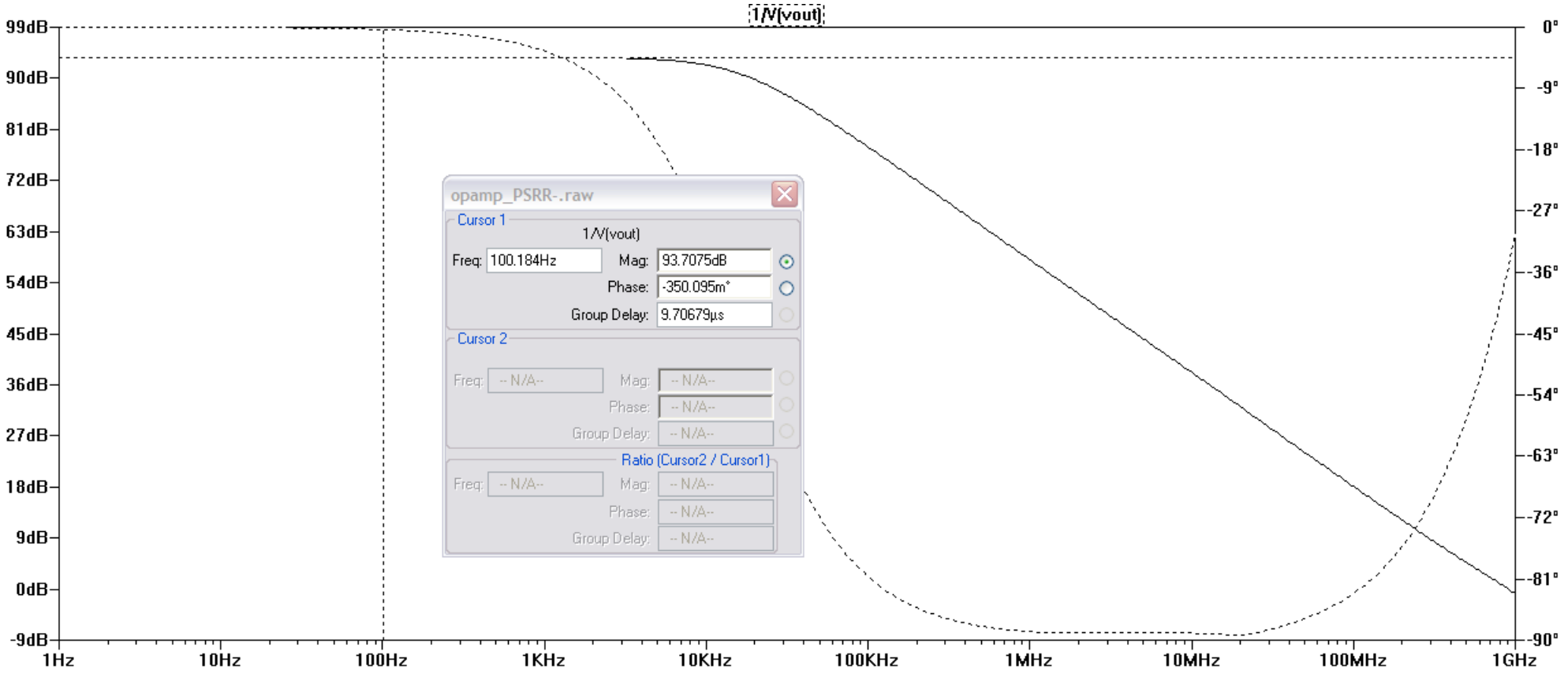


.ac dec 1000 1 1G

In order to find the Positive Power Supply Rejection Ratio or PSRR+, an AC analysis is performed using the SPICE directive shown with a “AC 1 0” stimulus applied to the VDD rail. This test is performed using the Unity Gain Buffer Test Bench. After simulation, the 1/Vout is analyzed to find the rejection ratio.

Positive Power Supply Rejection Ratio (PSRR+)
88.9 dB

PSRR-

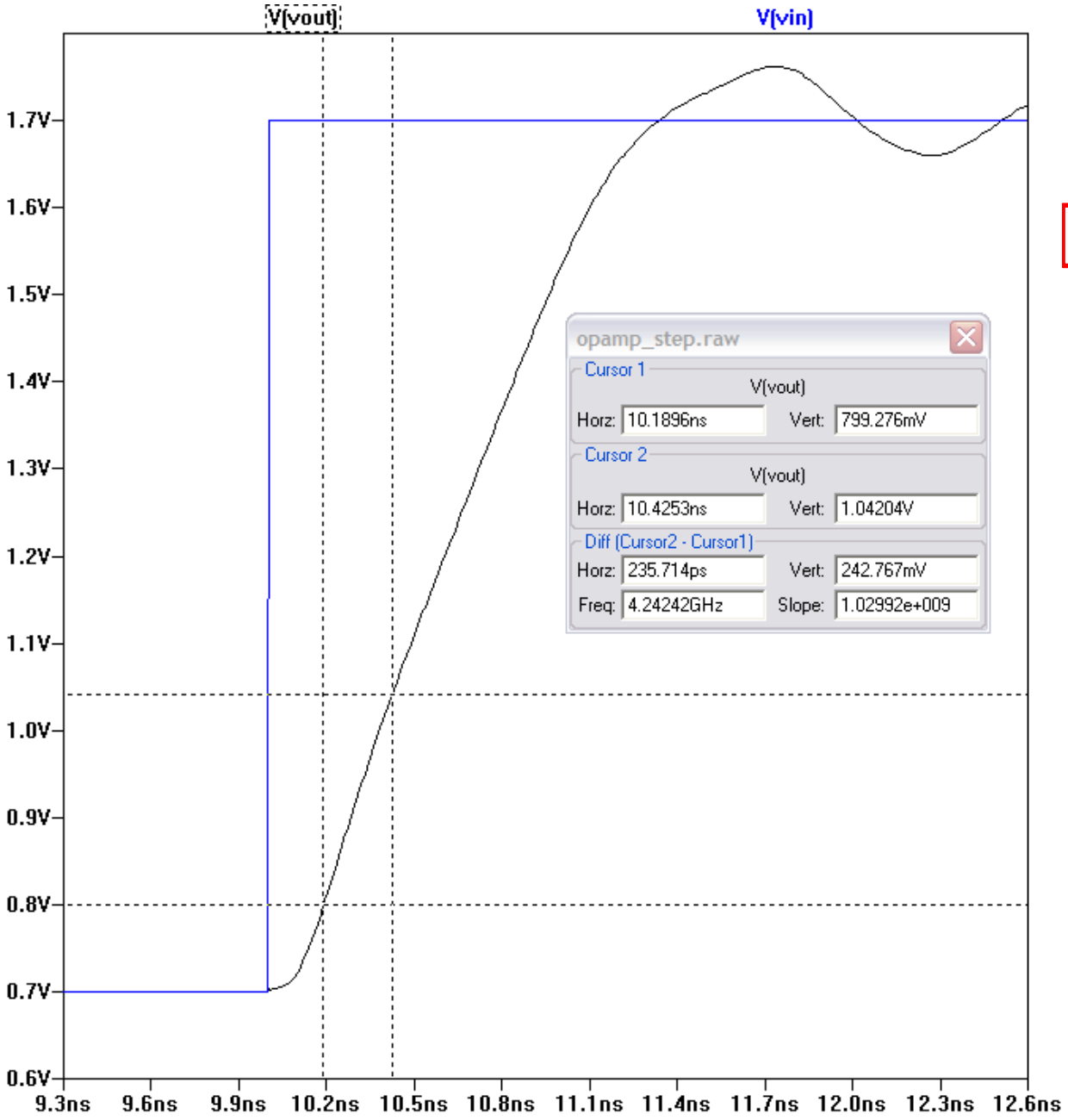


.ac dec 1000 1 1G

In order to find the Negative Power Supply Rejection Ratio or PSRR-, an AC analysis is performed using the SPICE directive shown with a “AC 1 0” stimulus applied to the VSS rail. This test is performed using the Unity Gain Buffer Test Bench. After simulation, the 1/Vout is analyzed to find the rejection ratio.

Negative Power Supply Rejection Ratio (PSRR-)
93.7 dB

Slew Rate - Positive Pulse



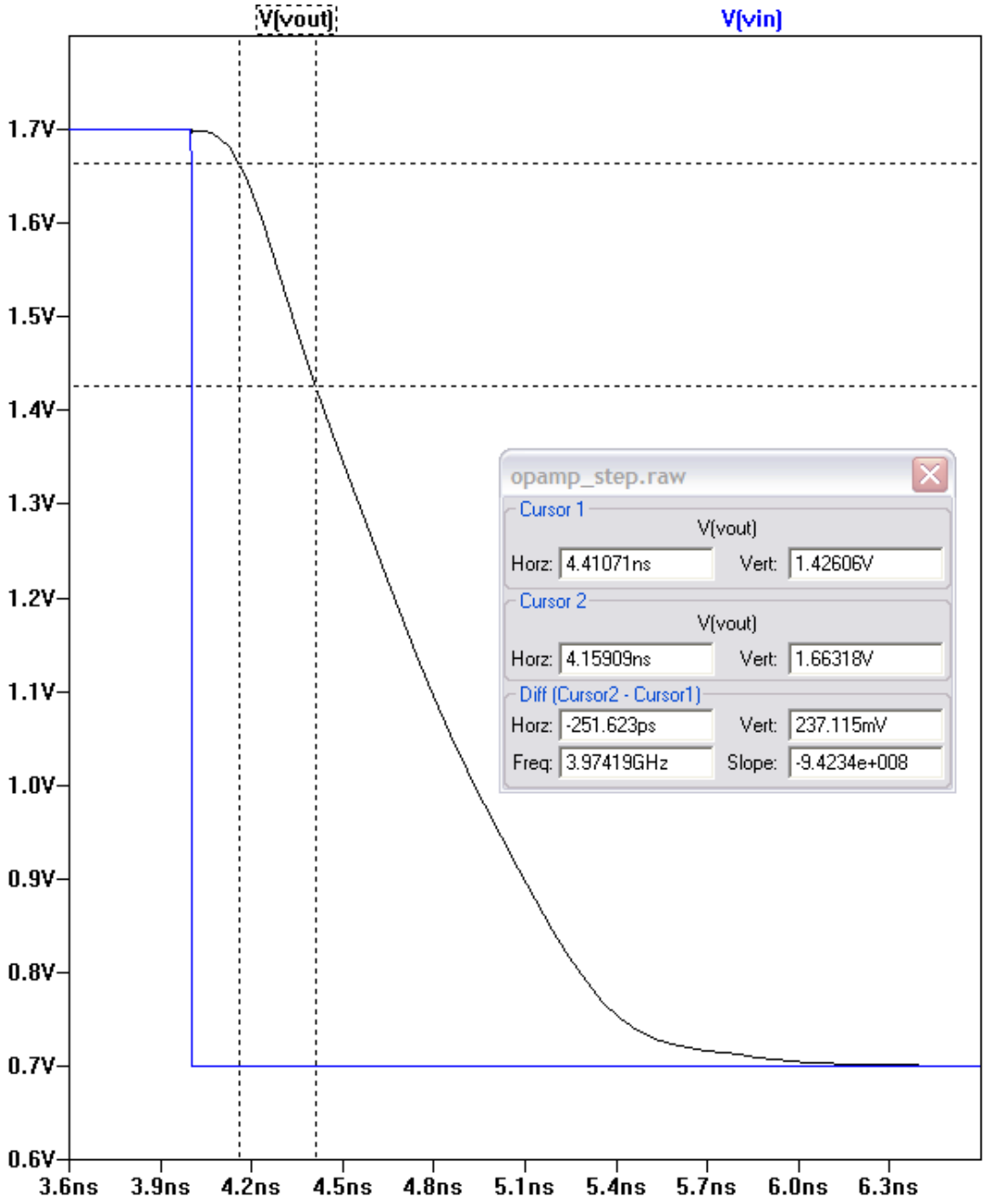
.tran 0 25n 0 10p

PULSE(0.7 1.7 10ns 1p 1p 100ns 2u)

The positive slew rate is simulated by applying a 1 volt pulse to the input of the amplifier and measuring the time domain performance of the rising edge of Vout with the transient SPICE directive shown above. Measurement cursers are then used to extract data points and a Positive Slew rate is calculated as shown below:

Positive Slew Rate
242.767mV/235.7ps=1.03V/us

Slew Rate – Negative Pulse



.tran 0 120n 106n 10p

PULSE(.7 1.7 10ns 1p 1p 100ns 2u)

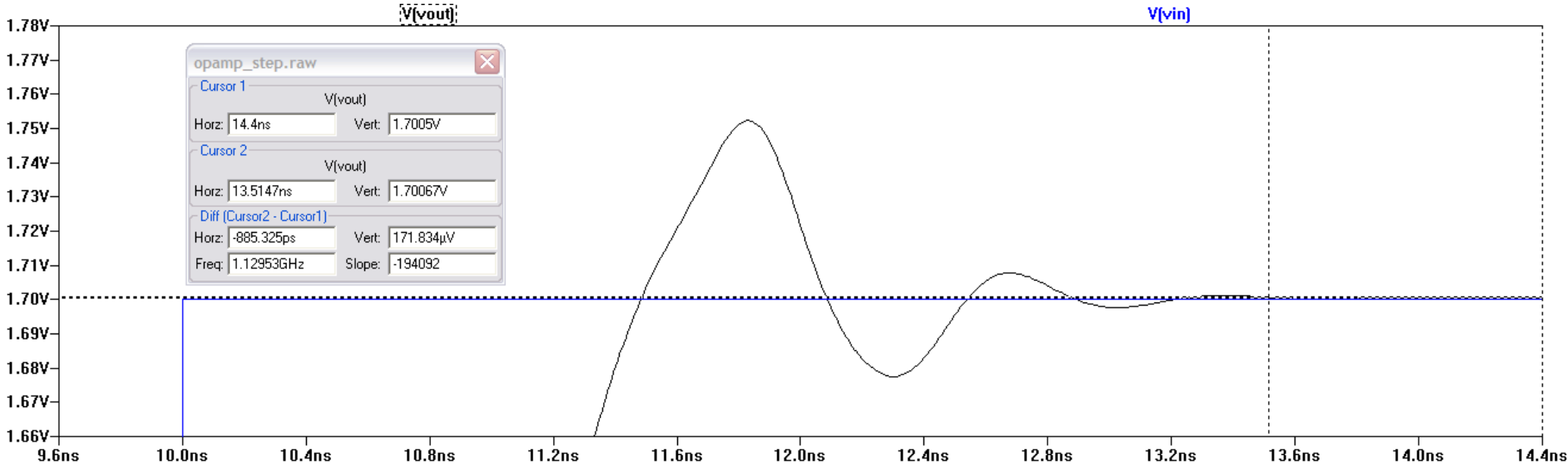
The negative slew rate is simulated by applying a 1 volt pulse to the input of the opamp and measuring the time domain performance of the falling edge of Vout with the transient SPICE directive shown above. Measurement cursers are then used to extract data points and a Negative Slew rate is calculated as shown below:

Negative Slew Rate
237.1mV/251.6s=0.94V/us

Positive Settling Time

PULSE(.7 1.7 10ns 1p 1p 100ns 2u)

.tran 0 25n 0 10p



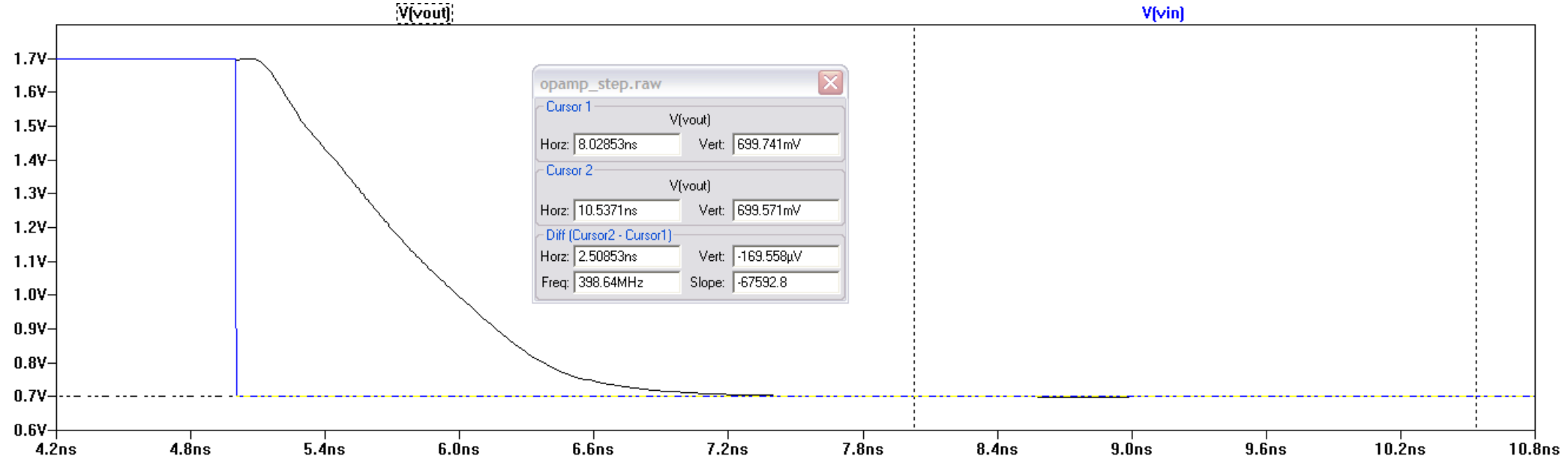
The Positive settling time is found by looking at Vout as it settles onto the value for Vin. A curser is used to identify the steady state value of Vout and then a second curser is used to find the point where the signal is absolutely within the settling envelope. Since we are designing for 0.001% envelope, the value needed here is 170uV. The settling time is then calculated as the time between 10ns when Vin rises and the first point within the envelope. This is measured to be 3.51ns.

Positive Settling Time
3.51ns

Negative Settling Time

PULSE(.7 1.7 10ns 1p 1p 100ns 2u)

.tran 0 120n 105n 10p



Similar to the Positive settling time, the negative settling time is found by looking at Vout as it settles onto the value for Vin. A curser is used to identify the steady state value of Vout and then a second curser is used to find the point where the signal is absolutely within the settling envelope. Since we are designing for 0.001% envelope, the value needed here is 170uV. The settling time is then calculated as the time between 5ns when Vin rises and the first point within the envelope.

Negative Settling Time
4.03ns

Individual Device Performance - PTAT

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Name:	Model:	W (um)	L (um)	M (#)	Id: (uA)	Gm: (uS)	Ro: (KΩ)	Vgs: (mV)	Vds: (mV)	Vdsat: (mV)	Vds-Vdsat (mV)	Saturation?
m:x1:ptat:c1	pmos	20.0	1.0	1.0	-24.5	346	371.75	-517	-1230	-160	-1070	Yes
m:x1:ptat:c2	pmos	20.0	1.0	1.0	-24.5	346	371.75	-517	-1230	-160	-1070	Yes
m:x1:ptat:c3	pmos	20.0	1.0	1.0	-25	351	380.23	-517	-1430	-160	-1270	Yes
m:x1:ptat:c4	pmos	20.0	1.0	1.0	-24.5	346	371.75	-517	-1230	-160	-1070	Yes
m:x1:ptat:c5	pmos	20.0	1.0	1.0	-23.1	332	332.23	-517	-723	-160	-563	Yes
m:x1:ptat:c6	nmos	5.0	1.0	1.0	25	391	236.97	574	574	95.7	478.3	Yes
m:x1:ptat:i1	pmos	6.6	0.2	1.0	-22.6	76.4	204.92	-809	-809	-360	-449	Yes
m:x1:ptat:i2	pmos	6.0	0.2	1.0	-22.6	323	136.43	-558	-558	-159	-399	Yes
m:x1:ptat:i3	nmos	0.66	0.1	1.0	23.1	51.6	294.99	1280	1280	339	941	Yes
m:x1:ptat:i4	nmos	6.0	0.2	1.0	22.6	207	197.24	833	747	161	586	Yes
m:x1:ptat:i5	nmos	6.0	0.2	1.0	22.6	210	225.73	829	994	159	835	Yes
m:x1:ptat:i6	nmos	6.0	0.2	1.0	24.5	213	192.68	769	769	164	605	Yes
m:x1:ptat:i7	nmos	6.0	0.2	1.0	22.6	199	137.74	769	444	164	280	Yes
m:x1:ptat:i8	nmos	6.0	0.2	1.0	22.6	199	139.08	769	449	164	285	Yes
m:x1:ptat:p_opamp:1	pmos	20.0	1.0	1.0	-4.81	114	934.58	-438	-438	-85.4	-352.6	Yes
m:x1:ptat:p_opamp:2	pmos	20.0	1.0	1.0	-4.9	116	961.54	-438	-517	-85.4	-431.6	Yes
m:x1:ptat:p_opamp:3	nmos	20.0	4.0	1.0	4.81	81.3	1457.73	578	1370	84.7	1285.3	Yes
m:x1:ptat:p_opamp:4	nmos	20.0	4.0	1.0	4.9	82.3	1426.53	580	1290	85.6	1204.4	Yes
m:x1:ptat:p_opamp:5	nmos	5.0	1.0	2.0	9.71	162	258.40	574	190	90.1	99.9	Yes

Individual Device Performance - Amp

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Name:	Model:	W (um)	L (um)	M (#)	Id: (uA)	Gm: (uS)	Ro: (KΩ)	Vgs: (mV)	Vds: (mV)	Vdsat: (mV)	Vds-Vdsat (mV)
m:x1:s1a	pmos	0.2	6.0	180.0	-3600	51600	0.49	-558	-264	-158	-106
m:x1:s1a1	pmos	0.2	6.0	180.0	-1710	34000	2.20	-545	-1050	-104	-946
m:x1:s1a2	nmos	0.2	1.0	180.0	1710	21700	0.63	781	192	122	70
m:x1:s1a3	nmos	0.2	1.0	180.0	1710	23000	1.75	689	497	114	383
m:x1:s1b	pmos	0.2	6.0	180.0	-3600	51600	0.49	-558	-263	-158	-105
m:x1:s1b1	pmos	0.2	6.0	180.0	-1710	34100	2.14	-546	-984	-105	-879
m:x1:s1b2	nmos	0.2	1.0	180.0	1710	22300	0.97	778	254	120	134
m:x1:s1b3	nmos	0.2	1.0	180.0	1710	23000	1.75	689	500	114	386
m:x1:s1m	nmos	0.2	1.0	180.0	3780	33200	0.45	769	275	163	112
m:x1:s1n	nmos	0.2	1.0	180.0	1890	25300	2.41	726	1460	112	1348
m:x1:s1p	nmos	0.2	1.0	180.0	1890	25300	2.41	725	1460	112	1348
m:x1:s2	pmos	0.2	6.0	900.0	-17600	251000	0.09	-558	-225	-158	-67
m:x1:s2_1	pmos	0.2	6.0	900.0	-17600	274000	0.21	-584	-775	-145	-630
m:x1:s2_2	nmos	0.2	1.0	900.0	17600	171000	0.20	825	547	154	393
m:x1:s2_3	nmos	0.2	1.0	900.0	17600	168000	0.18	753	453	154	299

Total Current Consumption

--- Operating Point ---

Node	Value	Type
V(vin):	1.2	voltage
V(vdd):	1.2	voltage
V(vout):	1.20015	voltage
V(vss):	0	voltage
I(C1):	1.2002e-24	device_current
I(Vss):	0.0249	device_current
I(Vdd):	-0.0249	device_current
I(Vin):	0	device_current
Ix(x2:VDD):	0.0249	subckt_current
Ix(x2:VN):	0	subckt_current
Ix(x2:VP):	0	subckt_current
Ix(x2:VSS):	-0.0249	subckt_current
Ix(x2:VOUT):	-4.37e-15	subckt_current

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In order to calculate the power consumption for this design, a DC operating point is simulated using the unity gain test bench and the current into the VDD port of the opamp is observed in the SPICE operating point output.

Total Current Consumption*
24.5 mA

Total Power*
50 mW

*Assuming 25C Ambient

Opamp Performance Summary

Parameter Description	Desired	Achieved	Value	Priority
Power Supply Voltage (VDD)	2.0	2.0	V	-----
Temperature (Room)	25	25	ºC	-----
IBM65nm Process Corner	Typical	Typical	-----	-----
Output Load Capacitor	1	1	pF	-----
Open Loop DC Gain (Avo)	>100	108.6	dB	1
Unity Gain-=Bandwidth Product (GBW)	>1000	1022.9	MHz	1
Open Loop	>65	70.1	Degrees	1
Positive Settling Time (0.01% of 1V input step)	<5	3.51	ns	1
Negative Settling Time (0.01% of 1V input step)	<5	4.03	ns	1
Power Supply Current Consumption (Idd)	<25	24.5	mA	2
Positive Slew Rate (SR+)	<1	1.03	V/ns	2
Negative Slew Rate (SR-)	<1	0.94	V/ns	2
Input Common-Mode Range (ICMR)	>1	0.65 to 1.7	V	2
Analog Signal (reference) Ground Voltage	-----	1.2V	V	2
Positive Power Supply Rejection Ratio (at 100Hz)	>60	88.9	dB	3
Negative Power Supply Rejection Ratio (at 100Hz)	>60	93.7	dB	3
Common Mode Rejection Ratio (at 100Hz)	>60	78.4	dB	3