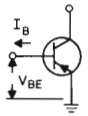
BASE INPUT CHARACTERISTICS



for $I_C = 0$

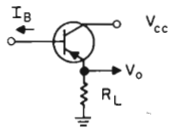
$$V_{BE} = I_B (R_E + R_B) + \frac{1}{\Lambda} \ln \left(\frac{I_B}{I_{EO}} + 1 \right) \qquad (3u)$$

for $V_{CE} > -.1$ volt

$$V_{BE} = I_B \left(R_B + \frac{R_E}{1 - \alpha_N} \right) + \frac{1}{\Lambda} \ln \left[\frac{I_B (1-\alpha_N\alpha_I)}{I_{EO} (1-\alpha_N)} + 1 + \frac{\alpha_N (1-\alpha_I)}{\alpha_I(1-\alpha_N)} \right] \qquad (3v)$$

A comparison of equations (3u) and (3v) indicates that they are approximately equal if R_E is small and α_N is smaller than α_I. For this condition, the base input characteristic will be the same whether the collector is reverse biased or open-circuited.

VOLTAGE COMPARATOR CIRCUIT



for $V_o = V_{CC}$

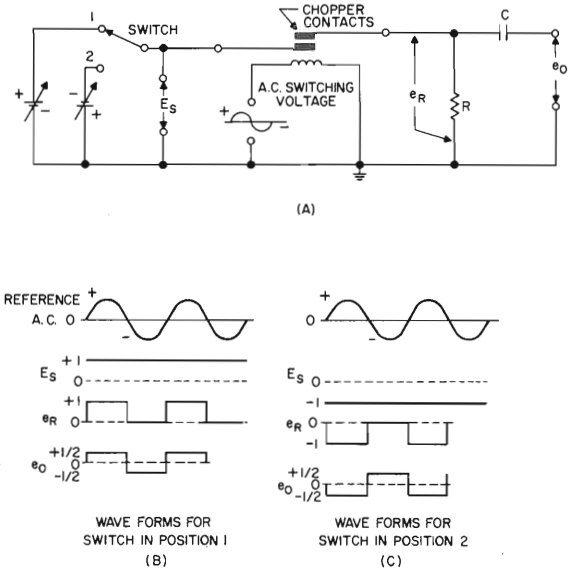
$$I_B = \frac{V_{CC}}{R_L} \left[1 + \left(\frac{\alpha_N}{\alpha_I} \right) \left(\frac{1 - \alpha_I}{1 - \alpha_N} \right) \right] \qquad (3w)$$

If an emitter follower is overdriven such that the base current exceeds the emitter current, the emitter voltage can be made exactly equal to the collector voltage. For example, if a square wave with an amplitude greater than V_{CC} is applied to the base of the transistor, the output voltage V_o will be a square wave exactly equal to V_{CC}. Equation (3w) gives the base current required for this condition and indicates that the transistor should be used in the inverted connection if the required base current is to be minimized. This circuit is useful in voltage comparators and similar circuits where a precise setting of voltage is necessary.

JUNCTION TRANSISTOR CHOPPERS

Transistor choppers are used in the amplification of low level d.c. signals, as well as in the conversion of d.c. signals to a synchronous a.c. voltage for driving the control phase of two phase servo motors. The chopper converts the d.c. signal to a synchronous a.c. voltage whose magnitude is proportional to that of the d.c. signal, and whose phase relationship to the reference a.c. voltage is either zero or 180°, depending upon the polarity of the d.c. voltage. This can best be seen by referring to Figure 3.7(A). The chopper contacts close during the positive half cycle of the a.c. reference and open during the negative half cycle. With the switch in position 1, the positive voltage E_S is tied to the resistor R as shown in Figure 3.7(B) during the positive half cycle of the reference. During the negative half cycle of the reference, the chopper contacts are open and the voltage across R is zero. The capacitor removes the d.c. level such that e_o is now an a.c. square wave which in phase with the reference a.c. If the switch is in position 2, the negative voltage E_S is applied to R during the positive half cycle of the reference voltage, and as can be seen in Figure 3.7(C), the output is 180° out of phase with the reference a.c.

Figure 3.8 shows a single transistor replacing the mechanical chopper. When the base voltage is made positive with respect to the collector (NPN transistor), the transistor behaves as a closed switch, and the d.c. input voltage is connected to R. During the half cycle of the reference voltage when the base is made negative with the supply,



HALF-WAVE CHOPPER

Figure 3.7

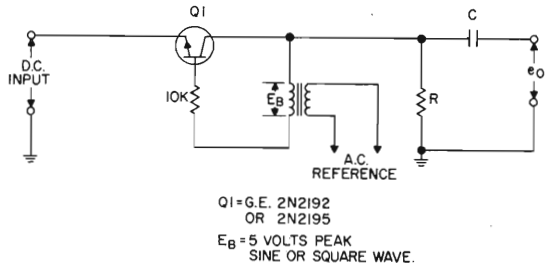
the transistor behaves as an open switch, and the voltage across R is zero. However, the transistor is not a perfect switch, and an error voltage and current are respectively superimposed on the d.c. source. During the half cycle that the switch is closed, the error voltage introduced by the transistor is

$$V_{EC} = .026 \ln \alpha_N + I_B r_C' \qquad (3x)$$

where α_N is the normal alpha as defined at the beginning of this chapter and r_C' is the collector bulk or body resistance. The error current which is introduced when the transistor is an open switch is

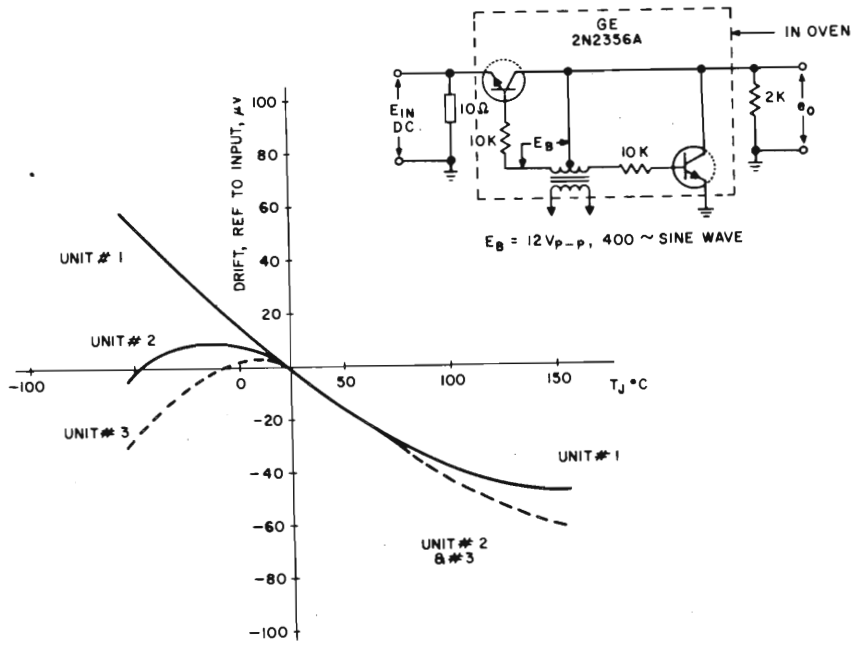
$$I_{PI} = \frac{I_{CBO} \alpha_I (1 - \alpha_N)}{\alpha_N (1 - \alpha_N \alpha_I)} \qquad (3y)$$

where α_I is the inverse alpha and I_{CBO} is the leakage current as defined earlier in this chapter.



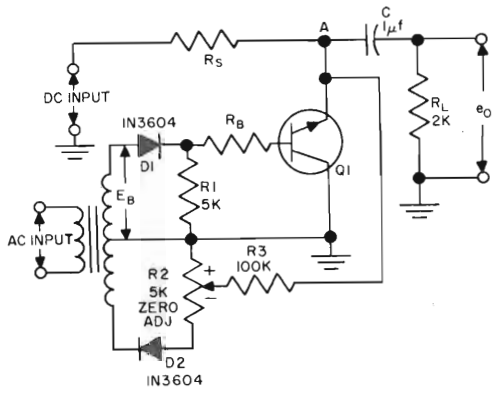
SIMPLE SERIES TRANSISTOR CHOPPER

Figure 3.8



TYPICAL TEMPERATURE DRIFT OF SERIES — SHUNT CHOPPER USING GE 2N2356A

Figure 3.11



NOTES:

1. R_S CAN BE SOURCE IMPEDANCE OF 50K TO SEVERAL MEGOHMS.
2. E_B = 10 VOLT PEAK SINE WAVE FOR GE 2N2195, R_B = 10K.
3. R_B = 100K FOR 12X1111, E_B = 10 VOLT PEAK SQUARE WAVE.

SHUNT CHOPPER FOR HIGH IMPEDANCE SOURCES

Figure 3.12

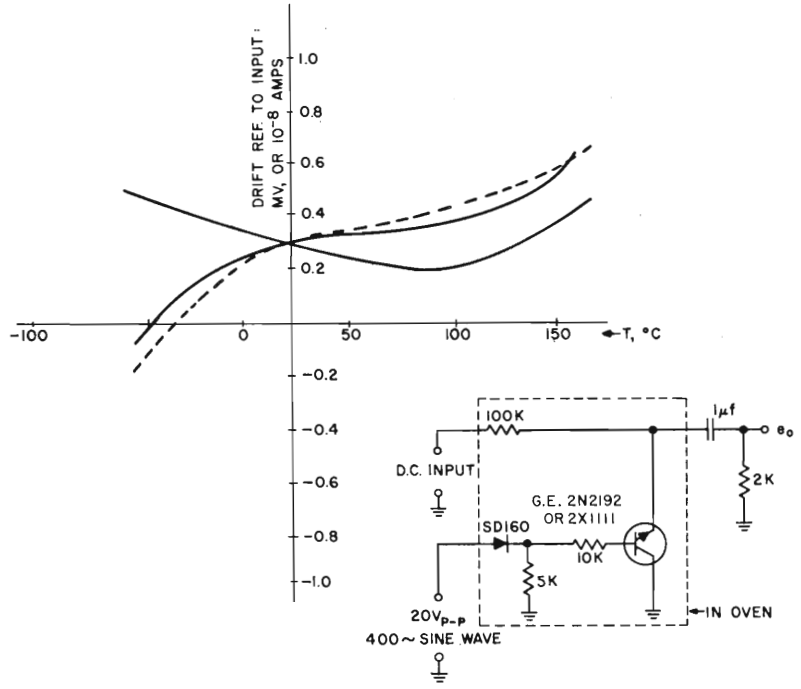
Figure 3.12 shows a transistor chopper used for high source impedance applications or those where the d.c. input cannot be loaded. Although R_S is shown as part of the chopper circuit, it can be the d.c. source impedance.

Operation of this chopper is basically one of shorting node A to ground each half cycle when the base of the transistor is made positive with respect to ground (the collector). A zeroing adjustment for removing the transistor's offset voltage is provided by D_1, R_2, and R_3 which causes a current to flow during the half cycle from collector to emitter [see equation (3g)]. In some applications where the 12X1111 and 2N2192 are used, the offset voltage is small enough (less than a millivolt) so that the balance network can be eliminated.

On the half cycle of the supply which would normally reverse bias the collector-base junction of Q, the diode D_1 prevents this from occurring. The collector-base potential is then zero; however, Chaplin and Owens[7] have shown that the emitter-collector impedance is given by

$$r_{EC} = \frac{0.026}{I_{CBO}} (1 + \alpha_N/\alpha_I - 2\,\alpha_N) \qquad (3z)$$

Thus the dynamic impedance is approximately 26 mv. divided by the I_{CBO}. For silicon transistors (even at high temperatures) this impedance can be made larger than the load impedance so that the current at node A due to the input d.c. voltage flows into the load during this half cycle. The maximum value of the load is then determined by the minimum value of r_{EC} obtained from equation (3z). Also, any drifts which normally



CHOPPER DRIFT WITH 2N2192

Figure 3.13

The error voltage introduced by the transistor during the "on" half cycle can be minimized by using two transistors whose offset voltages cancel one another as shown in Figure 3.9. The transistors must not only be matched at room temperature but must track over the required ambient temperature extremes. This is no problem with transistors such as the 2N2356 and the 2N3082 where two transistor pellets are mounted in one header. The initial offset voltages are matched to 50 and 75 microvolts respectively. Drifts of less than ±100 microvolts over an ambient temperature of −55 to 125°C are easily obtainable. The low drift results primarily from the low initial offsets of each transistor (due to the very high α_N and low r_c') and to the negligible temperature difference between the transistor pellets. Some of the important parameters of these chopper transistors is given in Table 3.1.

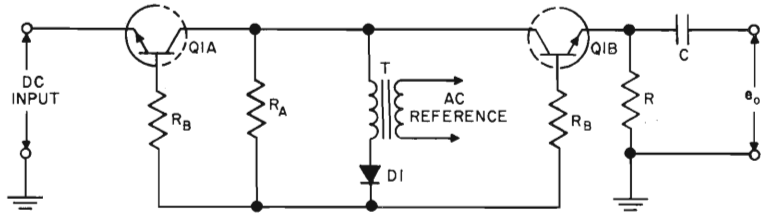
TYPE NUMBER	G.E. 2N2356	G.E. 2N2356A	G.E. 2N3082	G.E. 2N3083	UNITS
BV_{CBO}	25	25	25	25	volts, min
BV_{CEO}	–	–	20	20	volts, min
BV_{EBO}	7	7	10	10	volts, min
Differential Offset Voltage, 25°C	50	–	75	–	μ volts, max
Differential Offset Voltage change with temperature					
−55 to 25°C	100	–	100	–	μ volts, max
25 to 50°C	100	–	100	–	μ volts, max
Differential Offset Voltage, −55 to 125°C	–	50	–	75	μ volts, max
Differential Offset Current, 25°C	2	2	5	2	n amp, max
"On" Dynamic Resistance, $I_{B1} = I_{B2} = 1$ ma	40	40	40	40	ohm, max
Collector Capacitance ($V_{CB} = 0$ V)	–	–	8	8	pf, max
Emitter Capacitance ($V_{EB} = 0$ V)	–	–	8	8	pf, max

PARAMETERS OF CHOPPER TRANSISTORS

Table 3.1

A chopper configuration[4, 5] which can be used to advantage for a low source impedance input is shown in Figure 3.10. During the half cycle when Q_1 is "on," Q_2 is turned "off" because its collector-base junction is reverse biased, and R is tied to the d.c. input. On the next half cycle when Q_1 is turned "off," Q_2 is turned "on," shorting R, The leakage current due to Q_1 does not flow through R during this half cycle since Q_2 essentially short circuits R. During the alternate half cycle when Q_2 is turned "off," its leakage current will flow primarily through Q_1 (its turned "on") and the input circuit

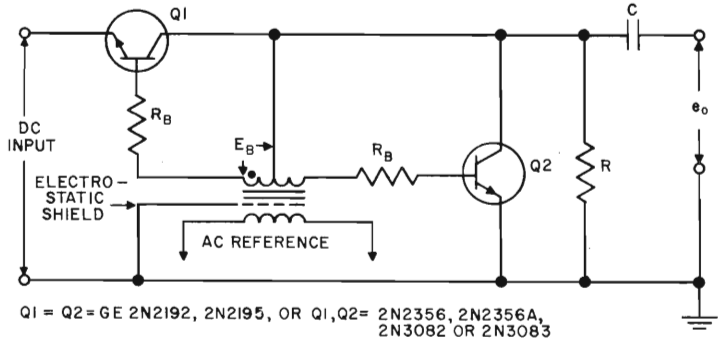
if R is made much larger than the source impedance. Thus, the drift due to leakage current is minimized. In addition, the offset voltages of the two transistors effectively cancel, even though they occur on separate half cycles. The reason for this is that they form a d.c. voltage which is not chopped and which is not passed by the capacitor, C. An advantage this circuit has over the chopper circuits discussed above is that it is less sensitive to noise pickup because the load always looks back into a low impedance.



NOTE:
1. QIA QIB – GE 2N2356, 2N2356A, 2N3082 OR 2N3083 (TWO MATCHED TRANSISTORS IN ONE PACKAGE)
2. ELECTROSTATIC SHIELDING BETWEEN PRIMARY AND SECONDARY WINDINGS OF TRANSFORMER T MAY BE REQUIRED.
3. R_B = 10K, E_B = 10 VOLT PEAK (SINE OR SQUARE WAVE).
4. DI = IN3604

AN IMPROVED SERIES TRANSISTOR CHOPPER

Figure 3.9



QI = Q2 = GE 2N2192, 2N2195, OR QI, Q2 = 2N2356, 2N2356A, 2N3082 OR 2N3083

NOTES:
1. R_B = 10K, E_B = 7.5 V SINE OR SQUARE WAVE FOR 2N2195, 2N2192, 2N2356, 2N2356A
2. R_B = 50K, E_B = 5V SQUARE WAVE FOR 2N3082, 2N3083

SERIES-SHUNT CHOPPER

Figure 3.10

Figure 3.11 shows actual drift performance obtained with this circuit using the 2N2356A as the chopper transistor[6]. The chopper drift was less than ±60 μv from −55 to 150°C.

would have been caused by the transistor leakage currents have been eliminated.

For the condition that $r_{EC} >> R_L$, the peak to peak load current is given by

$$I_{P\text{-}P} = \frac{2\,E_{D.C.}}{R_S + 2\,R_L} \qquad (3aa)$$

The equivalent input current drift due to drift in transistor offset voltage (ΔV) is shown to be

$$I_o = \frac{\Delta V}{R_S} \text{ for } R_S >> R_L \qquad (3bb)$$

A second component of the chopper drift is due to transient current spikes which occur when the transistor switches "on" and "off." The net area (charge) of the transients develops a potential on the capacitor C which, to the circuit, appears as an input signal. In order to zero the output, a d.c. input current (integrated over one-half cycle) must be provided. The 12X1111 is ideal for this application because of its low junction capacitances (< 8 pf at 0 volts) and low initial offset ($< 250\ \mu$V at $I_B = .1$ ma).

Temperature drift tests made using 2N2192's show that with the entire chopper of Figure 3.12 exposed to temperature, the required d.c. input necessary to zero the output is less than 10^{-8} amperes from -55 to 125°C. This is equivalent to 1 mv of drift referred to the input for $R_S = 100$ K.

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(2) Pritchard, R. C., "Advances in the Understanding of the P-N Junction Triode," *Proceedings of the IRE*, Vol. 46, June 1958.

(3) Giorgis, J., "Some Large Signal Properties of Planar and Planar Epitaxial Transistors," G. E. Application Note 90.13.

(4) Kruper, A., "Switching Transistors used as a Substitute for Mechanical Low Level Choppers," *AIEE Transactions*, Vol. 74, part I, March 1955.

(5) Giorgis, J., and Thompson, C. C., "Silicon Transistor Performance in a Chopper Application," *Applications and Industry*, #37, July 1958.

(6) Giorgis, J., "Silicon Transistor Choppers for Low Impedance Sources," *Solid State Design*, Vol. 4, No. 5, May 1963.

(7) Chaplin, G. B., and Owens, A. R., "Some Transistor Input Stages for High-Gain D.C. Amplifiers," *The Proceedings of the IEE*, Vol. 105, part B, No. 21, May 1958.

(8) Giorgis, J., "A Transistor Chopper for High Impedance Sources," *Electronic Equipment Engineering*, Vol. 11, No. 1, January 1963.

NOTES

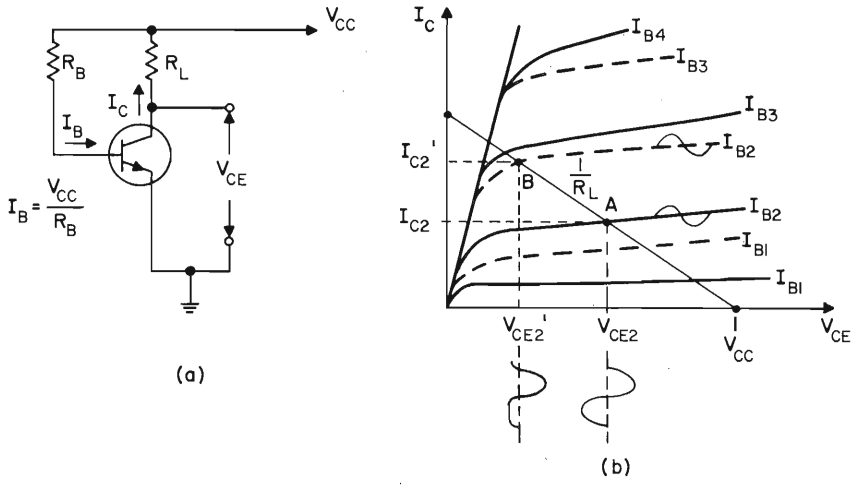
BIASING AND DC AMPLIFIERS

CHAPTER 4

BIASING

INTRODUCTION

One of the basic problems encountered in the design of transistor amplifiers is that of establishing and maintaining the proper dc emitter current and collector to emitter voltage (called the *bias conditions of the circuit*). The biasing problem is due primarily to the change of transistor parameters (h_{FE}, I_{CO}, V_{BE}) with temperature and the variation of these parameters between transistors of the same type. This can readily be seen by referring to Figure 4.1(a) where the transistor is operated in the common emitter mode and is biased by a constant base current, I_B. Figure 4.1(b) shows the common emitter collector characteristics of two different transistors with the same collector load line superimposed on them. For the transistor characteristic shown with solid lines and a base current I_{B2}, the operating point is at A. On the other hand, if a higher gain transistor is used, or the original transistor's gain and leakage current are increased due to an increase in temperature, the transistor characteristic shown with dashed lines could result. For the same base current, I_{B2}, the bias point is at B and distortion would result since the transistor begins to saturate during the positive half cycle of the signal base current.



SIMPLE BIAS CIRCUIT
Figure 4.1

The factors which must be considered in the design of transistor bias circuits, whether operating class A or class B, and single or multi stage include

1. *The specified maximum and minimum values of current gain (h_{FE}) at the operating point* for the type of transistor used.

FUNCTIONAL DEVICES (ACTIVE DISCRETE)

CHOPPERS — NPN Five-terminal Packages Containing Two Matched Pellets

Type	Dwg. No.	MAXIMUM V_O (Offset Voltage) $I_{B1}=I_{B2}=1$ ma $I_{E1}=I_{E2}=0$ μ volts	MINIMUM V_{EEO} $I_{E1E2}=1$ ma $I_{B1}=I_{B2}$ volts	MAXIMUM r_s $I_{B1}=1$ ma $I_{EE}=0.1$ ma ohms	MAXIMUM I_{CBO} or I_{CBO2} V_{CB1} or $V_{CB2}=25$v na
2N2356	32	(1) 300 @ −55°C to +125°C	20	40	10
2N2356A	32	(1) 50 @ −55°C to +125°C	20	40	10
2N3082	33	(2) 350 @ −55°C to +125°C	20	40	10
2N3083	33	(2) 75 @ −55°C to +125°C	20	40	10
4JD12X013	Special	Dual (Four transistor) version of 2N2356			
4JD12X070	Special	Dual (Four transistor) version of 2N2356A			

NOTES: (1) $I_{B1} = I_{B2} = 1$ma (2) $I_{B1} = I_{B2} = 0.25$ma

DARLINGTONS — NPN Four-terminal Package Containing Two Pellets Connected in Darlington Configuration

(See Outline Drawing No. 5)

Types	V_{CEO} MINIMUM I_C=30 ma volts	h_{FE} MIN. MAX. I_C=100 ma		h_{FE} MIN. MAX. I_C=10 ma		h_{FE} MINIMUM I_C=1 ma	I_{CBO}@PV$_{CB}$ MAXIMUM na	volts
2N997	40	7000	70,000	4000	—	—	10	60
2N998	60(1)	2000	—	1600	8000	800	10	90
2N999	60	7000	70,000	4000	—	—	10	60
2N2785	40(1)	2000	20,000	1200	—	600	50	30

NOTES: (1) V_{CEO} at 20 ma.

DIFFERENTIAL AMPLIFIERS — NPN Six-terminal Packages Containing Two Isolated Pellets

TYPE Dwg. No. 21	Dwg. No. 34	Dwg. No. 35	Dwg. No. 36	V_{CEO} Min. volts	h_{FE}@100 μa Min.	Max.	h_{FE1}/h_{FE2} @I_C=100 μa	h_{FE}@1 ma Min.	Max.	h_{FE1}/h_{FE2} I_C=1 ma	ΔV_{BE} 10 μa	1 ma	MAXIMUM I_{CBO}@V_{CB} na	volts
2N2060	—	—	—	60(1)	30	—	0.9-1.0	30	—	—	—	5	2	80
2N2223	—	—	—	60	25	—	0.8-1.0	—	—	—	—	15(3)	10	80
2N2480	—	—	—	40	20	—	0.8-1.0	30	250	0.8-1.0	—	10	50	60
2N2480A	2N3513	2N3514	2N3515	40	35	—	0.8-1.0	50	200	0.8-1.0	—	5	20	60
2N2652	—	—	—	60	35	—	.85-1.0	50	200	0.85-1.0	—	3	10	60
2N2652A	2N3516	2N3517	2N3518	60	35	—	0.9-1.0	50	200	0.9-1.0	—	3	2	60
12A8	—	—	—	30	30	—	0.6-1.0	—	—	—	—	15(3)	25	30
2N2453	—	2N3519	2N3520	30	80(1)	—	—	150	600	0.9-1.0	3	5	5	30
2N2910	—	—	—	25	70	—	0.8-1.0	80	—	0.8-1.0	10	10	—	—
2N2913	—	—	—	45	100	—	—	150	—	—	—	—	10	45
2N2914	—	—	—	45	225	—	—	300	—	—	—	—	10	45
2N2915	—	—	—	45	100	—	0.9-1.0	150	—	—	5	5	10	45
2N2916	—	—	—	45	225	—	0.9-1.0	300	—	—	5	5	10	45
2N2917	—	—	—	45	100	—	0.8-1.0	150	—	—	10	10	10	45
2N2918	—	—	—	45	225	—	0.8-1.0	300	—	—	10	10	10	45
2N2919	—	—	—	60	100	—	0.9-1.0	150	—	—	5	5	2	45
2N2920	—	—	—	60	225	—	0.9-1.0	300	—	—	5	5	2	45
2N3521	2N3522	2N3523	2N3524	45	155(1)	500	0.8-1.0(1)	200	600(2)	0.8-1.0	5	10	10	45
4JD12X084A See outline drawing No. 36				Network package (Matched 2N914 pellets @ I_C=1 ma. & 10 ma. h_{FE} ± 20%, V_{BE} ± 5mv.)										

NOTES: (1) At I_C=10 μa. (2) At I_C=10 ma. (3) At 0.1 ma.